

FEATURES

Low long-term drift

0.5ppm/year, typical (after first 3000 hours)

Low Zener reference noise: 0.14 ppm p-p (0.9 μ V p-p)

6.62 V typical Zener reference voltage

On-chip heater with temperature sensor

Specified for -40°C to $+125^{\circ}\text{C}$ operation

Industry-standard, 8-pin TO-99 package

APPLICATIONS

High accuracy instrumentation

Multimeters

Weigh scales

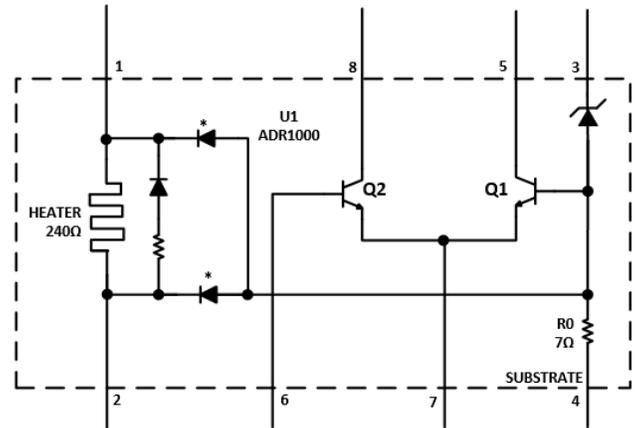
Electric balance

Automatic test equipment

Metrology equipment

Standard cells

Calibrators



* SUBSTRATE to NEPI Diode

NOTES:

1. PIN 4 IS THE SUBSTRATE AND IS CONNECTED TO THE CASE

Figure 1.

FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The ADR1000 has a 6.62 V output highly stable, oven-controlled, buried Zener reference component built on an Analog Devices, Inc., proprietary bipolar process and is a pin-compatible replacement for the [LTZ1000](#). Included on the chip is a buried Zener reference, a heater resistor for temperature stabilization, and a temperature sensing transistor. External circuitry is used to set the operating currents and to stabilize the temperature of the reference, allowing the maximum flexibility to achieve maximum long-term stability and minimum noise.

The ADR1000 application circuit can achieve a temperature coefficient of <0.2 ppm/ $^{\circ}\text{C}$ and a long term drift of 0.5 ppm per year (typical) after the first 3000 hours when properly implemented with the recommended external circuitry shown in 8 and with the recommended layout.

The low long-term drift of the ADR1000 is well suited for any application that must maintain accuracy over long calibration intervals or product lifetimes. The low thermal drift ensures the output is constant with temperature variations because the on-chip heater of the ADR1000

maintains a constant temperature above the expected ambient variations.

The ADR1000 is specified for operation over the extended industrial temperature range of -40°C to $+125^{\circ}\text{C}$. To get the best thermal drift performance, the temperature set point of the heater needs to be 10°C higher than the maximum ambient temperature to provide optimum stability of the buried Zener reference.

The ADR1000 comes packaged in an industry-standard, 8-pin TO-99 metal can package that is hermetically sealed to resist the effects of humidity.

Table 1. Related Products

Model	Output Voltage (V)	Initial Accuracy (mV)
ADR1000	6.62	± 50
LTZ1000	7.2	$-200, +300$
LM399	6.95	$-200, +350$

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REVISION HISTORY

5/2021— Rev. 1.0 to Rev. 1.1

Finalized BVCEO in Abs Max table on Q1 and Q2	4
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5/2021— Rev. SpA to Rev. 1.0

Changes to Figure 1 Conceptual Schematic.....	1
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Added Figure 7: Min Supply Voltage vs. Required Trise.....	8
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5/2019—Rev. Sp0 to Rev. SpA

Changes to Features Section and General Description Section	1
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Added Figure 4: Renumbered Sequentially	6
Changes to Theory of Operation Section	7
Changes to Heater Headroom Considerations Section	8
Changes to Figure 7	8

8/2018—Revision Sp0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
ZENER REFERENCE VOLTAGE ($V_{BZ1} + V_{BEQ1}$) ¹	V_{REF}	Zener current (I_{BZ1}) = 5 mA, I_{CQ1} current (I_{CQ1}) = 100 μA	6.57	6.62	6.67	V
		$I_{BZ1} = 1 \text{ mA}$, $I_{CQ1} = 100 \mu\text{A}$	6.54	6.59	6.64	V
ZENER LEAKAGE CURRENT	I_Z	Zener voltage (V_Z) = 5 V		1	1.5	μA
ZENER REFERENCE NOISE ($V_Z + V_{BEQ1}$)	$e_{N \text{ p-p}}$	$I_{BZ1} = 5 \text{ mA}$, $I_{CQ1} = 100 \mu\text{A}$, $0.1 \text{ Hz} < f < 10 \text{ Hz}$		0.14		ppm p-p
					0.9	$\mu\text{V p-p}$
	e_N	$I_{BZ1} = 5 \text{ mA}$, $I_{CQ1} = 100 \mu\text{A}$ $f = 0.1 \text{ Hz}$ $f = 10 \text{ Hz}$ $f = 1 \text{ kHz}$		300		nV/ $\sqrt{\text{Hz}}$
				30		nV/ $\sqrt{\text{Hz}}$
			24		nV/ $\sqrt{\text{Hz}}$	
HEATER RESISTANCE	R_{HTR}	Heater current (I_{HEATER}) = 1 mA	230	242	255	Ω
BREAKDOWN VOLTAGE		Heater				V
		Transistor Q1				
		Transistor Q2				
	BV_{HTR}	$I_{HEATER} < 10 \mu\text{A}$ to Pin 4 (I_{ZSET})	70	80		V
	BV_{CEO}	$I_{CQ1} < 10 \mu\text{A}$	5	30		V
	BV_{CEO}	I_{CQ2} current (I_{CQ2}) < 10 μA	25	55		V
CURRENT GAIN						A/A
Q1	h_{FE_Q1}	$I_{CQ1} = 100 \mu\text{A}$, $V_{CE} = 600 \text{ mV}$	280	400	520	A/A
Q2	h_{FE_Q2}	$I_{CQ1} = 100 \mu\text{A}$, $V_{CE} = 600 \text{ mV}$	190	300	410	A/A
TEMPERATURE COEFFICIENT	TCV_{REF}	Using the circuit shown in Figure 8 with the recommended layout		<0.2		ppm/ $^\circ\text{C}$
THERMAL HYSTERESIS	ΔV_{REF_TH}	$I_{BZ1} = 5 \text{ mA}$, $I_{CQ1} = 100 \mu\text{A}$, $\Delta T_A = 100^\circ\text{C}$		1		ppm
				6.62		μV
THERMAL RESISTANCE	θ_{JA}	Time = 5 minutes		216		$^\circ\text{C/W}$
LONG-TERM DRIFT	ΔV_{REF_LTD}	$I_{BZ1} = 5 \text{ mA}$, $I_{CQ1} = 100 \mu\text{A}$, $T_A = 25^\circ\text{C}$, chip set temperature (T_{SET}) = 75°C 200 hours (early life drift)		8.9		ppm
				7.7		ppm
				6.6		ppm
				6.2		ppm
				0.5		ppm

¹ V_{BZ1} is the buried Zener diode voltage, and V_{BEQ1} is the base emitter voltage of the temperature compensating transistor.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Heater to Substrate (Pin 4)	40 V
Q1 Collector to Emitter	15 V
Q2 Collector to Emitter	28 V
Emitter to Base Reverse Bias (Q1 and Q2)	2 V
Substrate Forward Bias	0.1 V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature, Soldering (10 sec)	300°C
Electrostatic Discharge (ESD) Rating	
Human Body Model (HBM)	2 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied.

Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Table 4. Thermal Resistance¹

Package Type	θ_{JA}	θ_{JC}	Unit
H-08			
1-Layer JEDEC Board	N/A ¹	N/A ¹	°C/W
2-Layer JEDEC Board	216	N/A ¹	°C/W

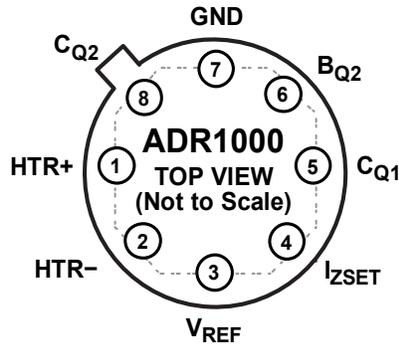
¹ N/A means not applicable.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. PIN 4 IS CONNECTED TO THE CASE.

16534-002

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	HTR+	Heater Positive. HTR+ must have a higher positive value than HTR- (Pin 2) and IZSET (Pin 4).
2	HTR-	Heater Negative. HTR- must have a higher positive value than IZSET (Pin 4) and must have equal or lower potential than HTR+ (Pin 1).
3	VREF	Zener Positive. VREF must have a higher positive value than IZSET (Pin 4).
4	IZSET	Substrate and Zener Negative. IZSET must have a higher positive value than GND (Pin 7).
5	CQ1	Temperature Compensating Transistor Collector (Q1).
6	BQ2	Temperature Sensing Transistor Base (Q2).
7	GND	Emitter of Sensing and Compensating Transistors.
8	CQ2	Collector of Sensing Transistor (Q2).

TYPICAL PERFORMANCE CHARACTERISTICS

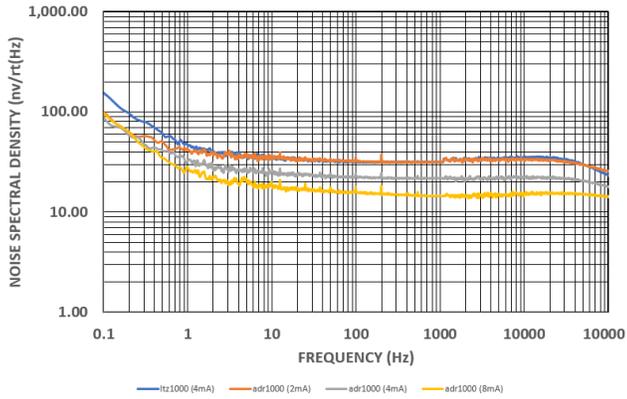


Figure 3. Noise Spectral Density vs. Frequency for Various I_{BZ1} with $I_{CQ1} = 100 \mu A$ (Heater Inactive)

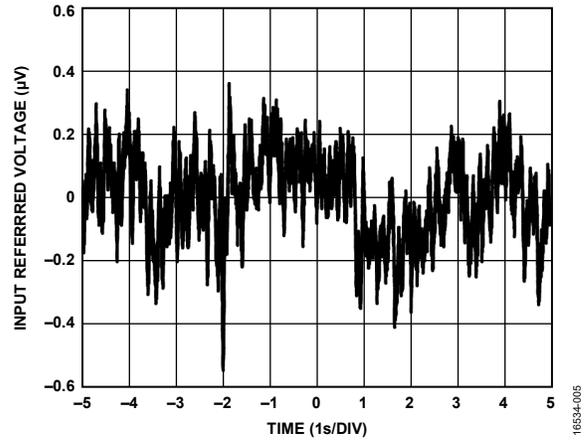


Figure 5. 0.1 Hz to 10 Hz Noise Peak to Peak, $I_{CQ1} = 100 \mu A$ and $I_{BZ1} = 5 mA$

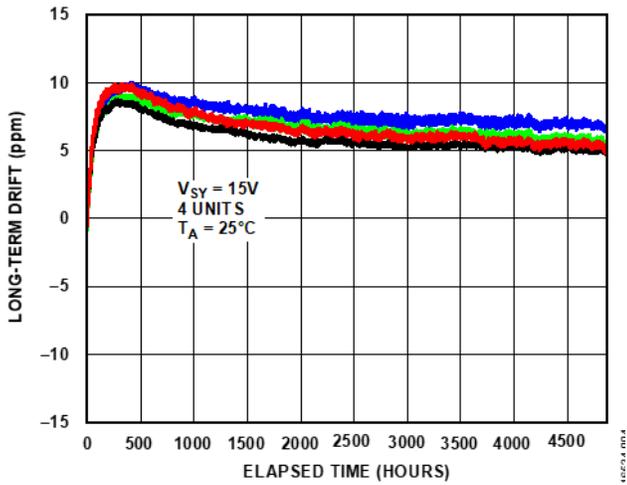


Figure 4. Long-Term Drift vs. Elapsed Time, $T_{SET} = 75^\circ C$

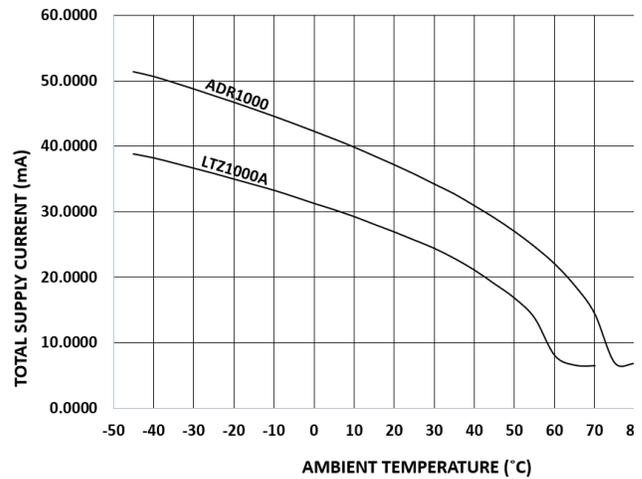


Figure 6. Total Supply Current vs. Ambient Temperature, $T_{SET} = 75^\circ C$

THEORY OF OPERATION

The ADR1000 consists of a buried Zener diode, a temperature compensating transistor, a temperature sensing transistor, and a heater resistor. The output reference voltage (V_{REF}) is formed by summing the buried Zener diode voltage (V_{BZ1}) and a temperature compensating transistor base emitter voltage (V_{BEQ1}), where the Zener diode temperature coefficient is approximately $+2 \text{ mV}/^\circ\text{C}$, and the transistor V_{BE} temperature coefficient is approximately $-2 \text{ mV}/^\circ\text{C}$. Referring to Figure 8, an external op amp (U3), in combination with an external resistor (R1), is used to set the Zener operating current as follows:

$$R1 = \frac{0.658V - 0.0022 * T}{I_z} - 7\Omega$$

T = heated chip temperature

I_z = desired Zener current

0.658V = Q1 vbe at 0°C

7Ω = bulk resistance to zener anode

With T = 70°C , and $I_z = 4\text{mA}$:

$$R1 = \frac{0.658V - 0.002 * 70}{I_z} - 7\Omega = 129.5\Omega$$

Note that because the 7Ω bulk resistance (R0 in Figure 1) schematically appears under Q1 base, it must be included in the calculation of I_z . The primary performance implication of the buried Zener operating current is output voltage noise. The ADR1000 can achieve a total output noise of 0.14 ppm (0.9 μV p-p) in the 0.1-10Hz frequency band when $I_{BZ1} = 5 \text{ mA}$ and $I_{CQ1} = 100 \mu\text{A}$, with the dominant noise source being the Zener diode. Increasing the current in the Zener (I_{BZ1}) reduces the reference noise by the inverse square root of Zener current. Zener bias current above 8mA is not very practical as power dissipation limits maximum ambient temperature. The ADR1000 applications circuit output noise spectral density has been measured over a range of Zener set currents (see Figure 3). The ADR1000 LTD is characterized at a Zener current of $I_{BZ1} = 5 \text{ mA}$ and a Q1 current of $I_{CQ1} = 100 \mu\text{A}$, and results are shown in Figure 4.

SETTING THE OPERATING TEMPERATURE

The ADR1000 can regulate chip operating temperature to within a few millidegrees over a 100°C ambient temperature change. This means if the unheated reference

temperature coefficient is $20 \text{ ppm}/^\circ\text{C}$ then the theoretical heated temperature coefficient is well below $0.1 \text{ ppm}/^\circ\text{C}$. Refer to the "Avoiding Thermocouple Errors" section to see why this performance is difficult to achieve in a practical circuit. The V_{BE} of Q2 is compared to a divided down copy of the 6.62 V reference voltage (see Figure 8). The 13 k Ω :1 k Ω divider sets the V_{BE} of the Q2 at around 474 mV. At room temperature, a V_{BE} of 474 mV does not provide enough collector current to satisfy the condition that the input terminals of U2 must be equal to within a few hundred microvolts, and thus, the noninverting input of U2 is pulled up until its inputs clamp or until its noninverting terminal hits V_{REF} . The voltage difference between the two inputs of U2 causes the output of U2 to pull up, raising the power dissipated in the on-chip heater. Because the transistor base emitter voltage has a negative temperature coefficient, the collector current of Q2 increases as the chip temperature rises, causing the op amp inputs to move closer together until the voltage drop across R3 satisfies the loop. The temperature at which the thermal loop is satisfied is the chip set temperature (T_{SET}).

Figure 6 shows the ADR1000 and LTZ1000A total supply current vs. the ambient temperature. Notice that the heater current has a square root dependence on the difference between the ambient temperature and the set temperature because the power dissipated in the heater is proportional to the square of the current. When the ambient temperature reaches the set temperature, the current in the heater goes to zero, and the chip temperature is no longer regulated.

With the values shown in Figure 8, a set temperature of 75°C is programmed. Set temperature is relatively easy to change in accordance with the maximum expected ambient temperature, plus 15°C of margin. Table 6 shows a list of recommended values used to vary the set temperature in 5°C increments.

THERMAL RESISTANCE

The ADR1000 uses a specialized epoxy die attachment to maximize the thermal isolation that reduces the power consumption required to achieve a given set temperature. At an ambient temperature of 10°C , the heater power consumption is approximately $35 \text{ mA}^2 \times 242 \Omega = 300 \text{ mW}$, assuming that the heater supply current is the total supply current minus 5 mA for the Zener current and other components on the PCB (see Figure 6). For 300 mW dissipation in the heater, the internal temperature of the ADR1000 is elevated by 65°C , yielding a $216^\circ\text{C}/\text{W}$ junction to ambient thermal impedance (θ_{JA}).

Table 6. Recommended Values for Varying the Set Temperature in 5° Increments

Estimate Set Temperature (°C)	R4 (Ω)	R5 (kΩ)	V _{BEQ2} (mV)
80	13 k + 316	1	464
75	13 k	1	474
70	13 k – 316	1	484
65	13 k – 632	1	494

HEATER HEADROOM CONSIDERATIONS

When colder ambient temperatures are combined with higher set temperatures, ensure that the heater drive NPN transistor (Q_{HTR}) does not approach the manufacturer specified V_{CE (SAT)}. V_{CE (SAT)} is the minimum collector emitter voltage for which a transistor base and collector terminals can sustain a large impedance. For example, at –40°C, the heater current is approximately 45 mA, which when multiplied by the 242 Ω heater resistance raises Pin 1 (HTR+) to 10.9 V. When the positive supply voltage (V+) is set at 15 V, this leaves 4.1 V headroom for Q_{HTR}. If characterization shows a marked increase in the temperature coefficient of the ADR1000 at lower ambient temperatures, the most likely culprit is not enough headroom for Q_{HTR}. This issue can be solved by either increasing V+ or by choosing a lower chip set temperature to reduce Trise. The following formula can be used to estimate minimum heater supply voltage:

$$V_{min} = \sqrt{Trise / (R_{TH} * R_H)} * R_H + V_{BEQ_{HTR}} + I_{BQ_{HTR}} * 1k\Omega + ADA4084(V_{out})$$

$$Trise = T_{chip} - T_{ambient}$$

$$R_{TH} = \text{Package Thermal Resistance } (216^\circ/W)$$

$$R_H = 240\Omega$$

$$V_{BEQ_{HTR}} = 900mV^1$$

$$I_{BQ_{HTR}} * 1k\Omega = (\sqrt{Trise / (R_{TH} * R_H)}) / \beta * 1k\Omega$$

$$ADA4084(V_{out}) = \text{Positive Headroom Limitation} = 1V$$

Fig 7 shows a plot of V_{min} vs. Required TRISE.

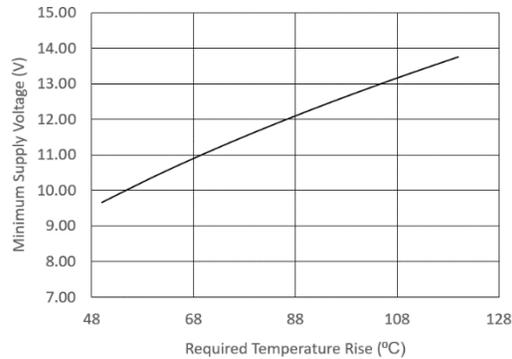


Figure 7: Minimum Supply Voltage vs. Required Trise

CHOOSING EXTERNAL OPAMPS

The ADR4084 dual opamp is used with the ADR1000 evaluation board because it has a common mode range that includes ground on a single supply, and because the output swings rail-to-rail. Ground sensing inputs ensure proper startup when input signals are both close to zero volts. Post startup, the ADA4084 common mode sits at around 480mV. Rail-to-rail output swing ensures the heater voltage can be driven from zero to within one volt of the positive supply. One additional requirement is that the opamp not swing to exactly zero volts during startup, which creates a stable operating point of zero volts on the reference output. Because the ADA4084 is a bipolar amplifier, its negative output swing is limited by the typical Vol specification of 50mV, preventing the amplifier output from reaching true ground.

A common question is: “how do opamp parameters like offset and noise effect performance of the ADR1000 applications circuit?” Other than proper startup, most opamps have little to no effect on the ADR1000 reference specification. Referring to Figure 8, Q1 runs at a gain of approximately 230, which looks like an additional gain stage in between the zener reference and the amplifier. This stage effectively attenuates any noise or offset contribution by 230:1.

¹ Parameter is discrete transistor dependent.

CHOOSING EXTERNAL RESISTORS

Although the ADR1000 schematic reduces the external resistance sensitivity by 200 or more, care must be taken in selecting certain components. For example, if a resistor exhibited 200ppm long term drift, that would affect the reference output by only 1ppm- in absolute terms a small

value but significant compared to the relative stability of the ADR1000. Resistors R1, R2, R4 and R5 should be metal foil, wire wound, or precision thin film to minimize noise, long term stability, and temperature drift. Table 7 shows the ratio of resistor change to reference voltage change.

Table 7. Application Circuit Resistor Attenuation Factors

Component	Attenuation Factor
R1	340:1
R2	230:1
R3	3900:1 @ unheated TC=20ppm/°C (Iz=5mA)
R4, R5	208:1 @ unheated TC=20ppm/°C (Iz=5mA)

For example, if R1 has a tempco of 10ppm/°C, it will cause the Vref tempco to vary by $10/340 = 0.03\text{ppm}/^\circ\text{C}$. Also, if R1 exhibits a long term drift of 40ppm, it will cause $40/340 = 0.12\text{ppm}$ change in reference voltage.

The note on R4 and R5 is because they thermostatically control IC temperature, so the unheated drift of the reference loop is material. As much as possible, R4 and R5 tempcos should track to prevent any dependence of the die set temperature on ambient temperature.

APPLICATIONS INFORMATION

BASIC CONNECTION

Figure 8 shows the recommend typical connection diagram for using the ADR1000. In addition, this is the circuit configuration used during the evaluation of the ADR1000. Resistors R4 and R5 are precision resistors.

AVOIDING THERMOCOUPLE ERRORS

Thermocouples are voltage offsets that occur whenever two dissimilar metals form a junction. For example, the TO-99 package leads are made of Kovar and must be soldered to a copper trace in a PCB design. Kovar copper junctions are known to cause thermocouple errors of $35 \mu\text{V}/^\circ\text{C}$, which is 50 times the theoretical temperature coefficient of the ADR1000. Thermocouple errors can be avoided by ensuring that critical pins always see the same temperature. In Figure 8, the reference voltage is taken from Pin 7 (GND) and Pin 3 (V_{REF}) of the ADR1000. Therefore, ensure that there are no extraneous heat sources to cause a thermal gradient between these two pins. It is also recommended to use air caps over the ADR1000, as well as the temperature set resistors, R4 and R5, to prevent air currents from disturbing these leads. Because the TO-99 package is a through-hole package, even the portion of the leads that protrudes to the underside of the board must be capped for optimal stability over time and temperature. Board cutouts can isolate unwanted heat sources from the ADR1000. It is also recommended that the temperature set divider resistors, R4 and R5, are wire wound or metal film to minimize temperature drift and thermocouple errors. Table 8 shows the effect of thermal EMF in component leads, with the attenuation factor calculated for each, and overall reference

drift in $\text{ppm}/^\circ\text{C}$. Note that the most sensitive component is the ADR1000 itself, followed by R5 and R1. The $10 \mu\text{V}/^\circ\text{C}$ number assumed is a conservative worst case value. Metal foil resistors will have much lower thermal EMF.

Table 8: External Component Thermocouple Attenuation Factors

Component	Attenuation Factor	Sensitivity (μV)	Sensitivity (ppm)
ADR1000	$10 \mu\text{V}/^\circ\text{C} * 1$	$35 \mu\text{V}/^\circ\text{C}$	$5.3 \text{ppm}/^\circ\text{C}$
R1	$10 \mu\text{V}/^\circ\text{C} * 0.033$	$0.33 \mu\text{V}/^\circ\text{C}$	$0.05 \text{ppm}/^\circ\text{C}$
R2	$10 \mu\text{V}/^\circ\text{C} * 0.005$	$0.05 \mu\text{V}/^\circ\text{C}$	$0.008 \text{ppm}/^\circ\text{C}$
R3	$10 \mu\text{V}/^\circ\text{C} * 0.001$	$0.01 \mu\text{V}/^\circ\text{C}$	$0.002 \text{ppm}/^\circ\text{C}$
R4	$10 \mu\text{V}/^\circ\text{C} * 0.01$	$0.1 \mu\text{V}/^\circ\text{C}$	$0.015 \text{ppm}/^\circ\text{C}$
R5	$10 \mu\text{V}/^\circ\text{C} * 0.15$	$1.5 \mu\text{V}/^\circ\text{C}$	$0.23 \text{ppm}/^\circ\text{C}$
R8	$10 \mu\text{V}/^\circ\text{C} * 0.001$	$0.01 \mu\text{V}/^\circ\text{C}$	$0.002 \text{ppm}/^\circ\text{C}$

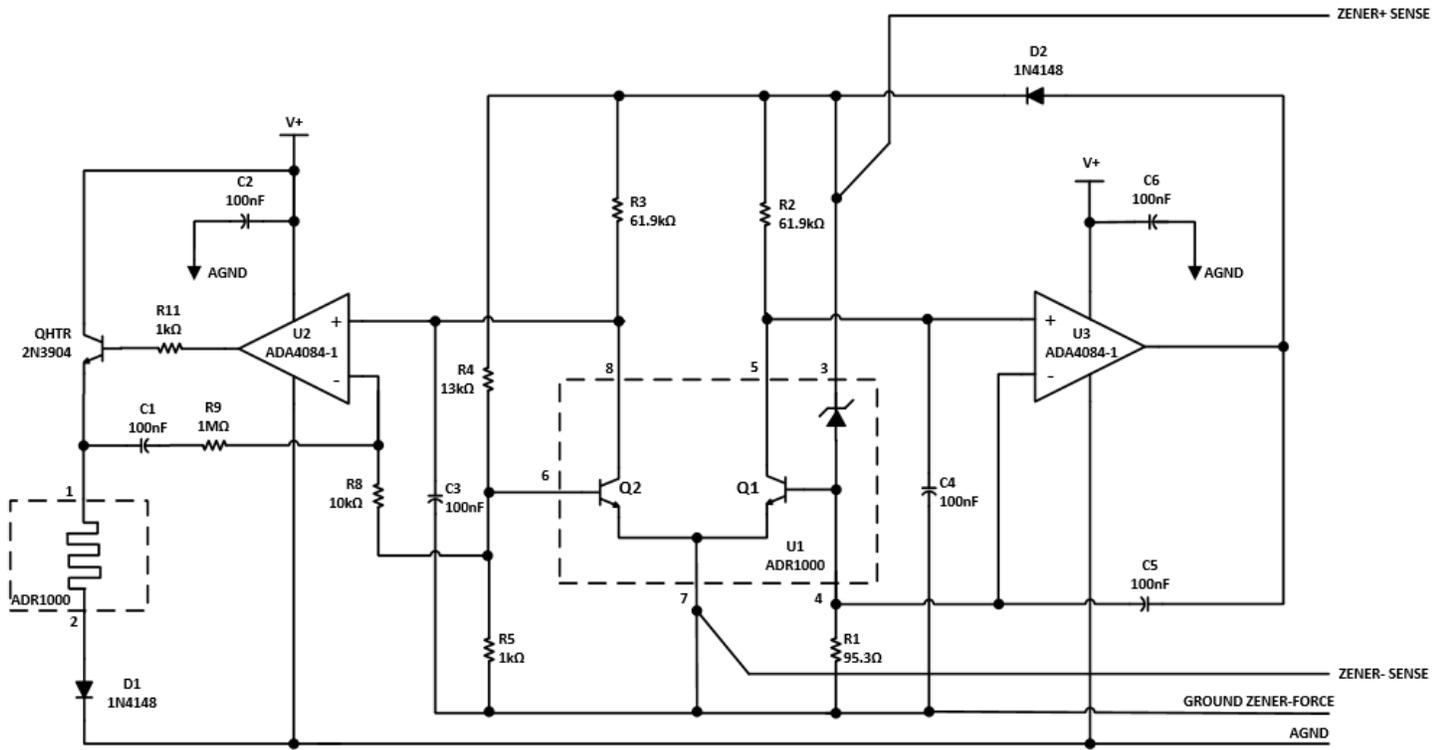
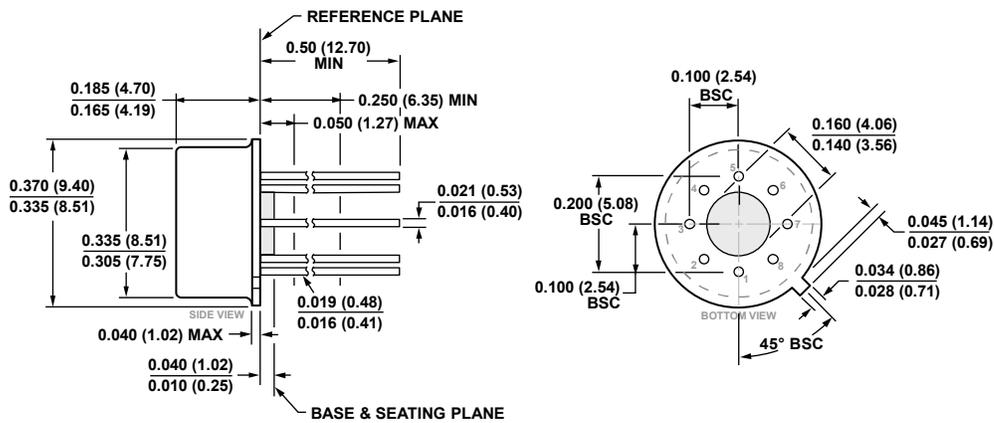


Figure 8. Typical Connection Diagram

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-002-AK
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

01-15-2015-B

Figure 9. 8-Pin Metal Header Package [TO-99]
 (H-08)

Dimensions shown in inches (millimeters)

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Ordering Quantity
ADR1000AHZ	-40°C to +125°C	8-Pin Metal Header Package [TO-99]	H-08	100

¹ Z = RoHS Compliant Part.

owners.

D16534-0-5/19(Rev. 1)