Setup of the 22-bit Delta-Sigma converter, v. 10.1

Objective

The Delta-Sigma 22 bits, a third order modulator originally developed by John Pett, needs a few starting up adjustments, ageing and setup. It is only carried out once and the procedure is fully explained here. Further adjustments should not be necessary, but are replaced by a digital calibration explained elsewhere

Tools required

This procedure requires a 10 Volts reference (Metron PBC), an oscilloscope, a DVM (8.5 digits type HP 3458), a frequency/counter device, a soldering iron (SMD) and a set of precision resistors (E24 / 1206, SMD) from 1 to 30 Ohms. Normal lab tools will help, like screwdrivers and a pot-trimmer. A PC with SLAP running an FGC is necessary for the evaluation of the 500 kHz/1 MHz output data stream.

Description of the subsystems

There are two PCBs inside the module, the power supply card and the modulator card. The power supply provides +/-15V for the analog part, +5V for the digital control and +/-4Vfor the Peltier element. The ±5V reference voltages for the ADC are generated internally from the 7.1 V primary reference on the modulator card. The power supply card includes a MOSFET power amplifier for the Peltier element, located under the modulator card. It also contains an optical fibre output driver for the data.

The modulator card includes a temperature regulated Al-block that covers all the sensitive components e.g. the voltage reference, resistor networks and the first integrator. The control logic is implemented in an FPGA with a quartz clock at 8/16 MHz. The temperature regulation circuits are also placed on this card. There are four potentiometers to be adjusted and one resistor to be installed in this setup procedure.

First check

The power supply card should be delivered mounted to the front panel and the modulator should be separate in its thermal insulation box and heat sink. Do not connect the modulator yet to the power supply card. Connect the mains supply and check that all LEDs on the front are green. Measure all the front panel voltages. Connect the modulator and verify again the supply voltages.

Time for Burn-in

The internal reference, LTZ1000A, should normally be burned in previously in a special setup in an oven. If this has not been done, and only for the units that have not been burnt in, it must be done now. To do this, mount R32, 3.3 kΩ, and leave the unit under power for at least 3 weeks. After this period remove R32.

Programming the FPGA

Unplug the modulator power supply connector and remove the modulator cover carefully. The FPGA can now be programmed via the JTAG connector J1. When programmed and re-powered, the red modulator LED fibre driver must be lit.

ID chip

The modulator and the power supply are equipped with Dallas ID chips for unique identification. Read them with an FGC and enter the values in the FGC database, otherwise the test software will not run.

Adjustments

- *Temperature control*

The temperature should be set to 25 °C. Connect the DVM between **TP10** and the **TP3 (GND)**. Adjust **P1** to reach 1.49 V (which corresponds to 25 °C). Remove the jumper **SW1** (open loop mode) and the regulation will saturate. Connect the scope probe or a DVM to **TP9** (error w.r.t. nominal value), put back the jumper **SW1** and watch the regulation working. The final value should be zero with a noise of approximately 10 mV_{p-p} (1 V corresponds to 1 °C).

- *±5V Reference voltage check*

Connect the DVM to **TP8** using TP13 as GND sense. It must read 7.1 V (±0.1 V). Check the stability.
Verify that the ±5 V reference voltages for the switches (± 1 bit DAC), **TP2** (+5 V) and **TP11** (-5 V) are stable.

- *Adjusting the dither*

The triangle-wave generator is adjusted by **P3** for the amplitude and **P2** for the frequency. Verify at **TP6** wrt **TP1**. The excursion must be adjusted to roughly the amplitude at **TP7**, 1.3 V and the frequency to 480 kHz. The modulator is now operational and data can be used, but there will be an offset at zero.

- *Offset setup and fine adjustment*

The three branches of a 'T' are providing the equilibrium for the zero in the charge balance system. R60 is initially 0 Ω, and R48 and R49 (also 0 Ω), which balance the switch resistance for the +5V reference resistors. The range of the potentiometer P4 (22 turns) is affecteded by these resistors and is centered by changing their values. It is only

carried out once at the setup.
Connect a short-circuit to the input and read the digital raw value through the FGC. First, turn P4 fully counterclockwise (CCW) and read the value. Then turn it clockwise (CW) to the end and read the new value. The difference should be about 100 (ppm of 10 V). Calculate the mid value and set the potentiometer to that point. If the read value is negative and greater than 90, divide the number by 88 to get the resistance value and replace the R60 resistor. The final value should be less than +/- 20ppm. As the potentiometer is in the middle scale, adjust now the reading for 420 digital (~ +15 ppm) to avoid idle tones at zero.

Last check and closing the box

Closing the box and putting the covers on could affect the offset value a few ppm. It should be re-checked after a few hours/days of stabilization. Calibrate it with available calibration software in SLAP and run a noise and stability evaluation.

The unit is now ready to use. Leave it under power for the longest possible time to improve stability. After a power cut or failure, wait several hours for re-stabilization and re-check offset and gain errors by renewed calibration.