

Design & Evaluation of a Metrology Class, Delta-Sigma Analogue to Digital Converter for the LHC project at CERN.

Allan Belcher¹, John Pett² & John Pickering³

¹Signal Conversion Ltd, Swansea, UK ²SL Group, CERN, Geneva, Switzerland

³Metron Designs Ltd, Norwich, UK

1 Introduction

The new LHC (Large Hadron Collider) particle accelerator, currently under construction at CERN, Geneva, will employ some 1700 converters powering cryogenic magnets to steer twin beams around the 27km ring. The critical positioning of the beams is dynamically controlled by adjusting the magnet current from near zero to some 13kAmps to track a pre-determined current profile to within a few parts per million (ppm).

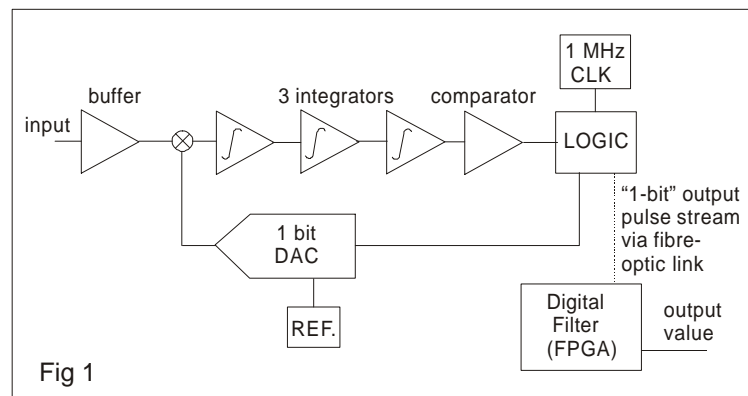
The control is performed in a digital loop requiring A-D conversion capable of sub ppm performance at real independent data rates up to the kHz region. Since no commercial product was available to meet this requirement, especially in the anticipated working environment, one of us (John Pett) designed and developed an a-d converter using Delta-Sigma technology. When prototypes became available, CERN sought independent verification of its performance, by asking the other two of us, as “industry experts” to perform rigorous evaluation of its operation and key parameters.

This paper outlines the CERN requirement as it relates to the A-D and describes at a functional level its operational characteristics and shows how simulation can verify its time domain characteristics. DC and Dynamic testing methods are described, along with the very difficult measurement source requirements. Finally an outline of the results is presented revealing that this converter technology, more often associated with digital audio, is quite capable of meeting very stringent metrology requirements.

2 Basic A-D Delta-Sigma Design

The ADC employed in the digital regulation loops for LHC is described in [1]. The choice of Delta-Sigma as the conversion technology was, as far as was known at that time, the first time it had been utilised for very high performance DC & LF metrology application. Such applications had previously turned exclusively to DVM-like methods but in this case would not achieve the necessary resolution-bandwidth product to be useable in the LHC’s proposed magnet current digital control loops.

The basic structure chosen is shown in Fig. 1. After a number of prototype realisations were made, based on an initial optimisation of parameters obtained via simulation, a third order integrator and 4th order digital filter were selected as having the required performance with limited complexity. Furthermore a 1MHz clock was chosen and each of the “sync 4” digital filter registers selected to be of 250 elements in length. This means that the filter completely flushes through in 4X250 clocks or, in this case, 1 millisecond giving a true complete conversion rate of 1kHz.



3 Evaluating the Suitability and Capability of the Design

For a converter of this nature, intended to work to the required performance over a wide range of measurement stimuli and conditions, it is virtually impossible to perform 100% testing and it is therefore necessary to interpolate between sample measurements and therefore to have knowledge of the converter’s characteristics in order to validate the interpolations. Traditionally, charge balance A-Ds have been the technology of choice for very high resolution DC measurements and are used in most high end DVMs. At first sight one would assume that Delta-Sigma is a version of charge balance and would have the same speed:resolution characteristics, but if

it is viewed in that way it is clear that with a 1MHz clock and only 1000 1 bit samples the resolution cannot be better than .1% (10 bits) where actual performance was expected to be around 22 bits. Delta-Sigma analysis in

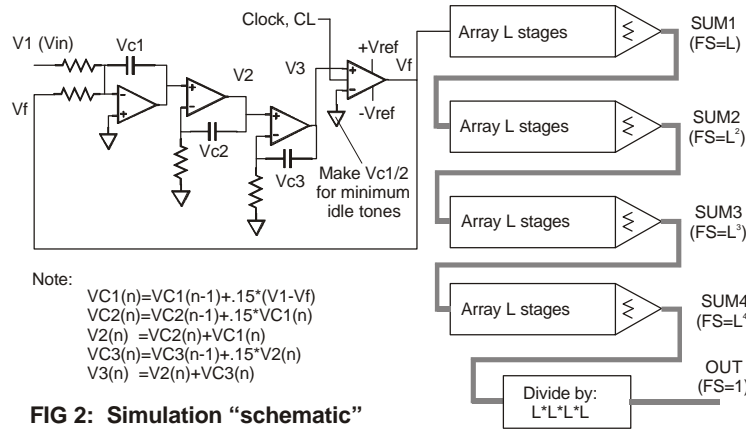


FIG 2: Simulation “schematic”

balance, for example dual slope, it would only have been able to achieve 0.5% resolution. The results of a simple simulation are shown in Fig 3 where the outputs of the Sum2, Sum3 and Sum4 are plotted against clock increment from the start of the measurement of an arbitrary value, in this case .765432 of Full Scale. Quite clearly the output (sum4) is settled and within about .005% of the input after only 200 clocks. To those familiar with charge balance this is quite extraordinary and indicates that at the end of the measurement period the net Reference charge entering the first integrator does NOT equal the net Signal charge.

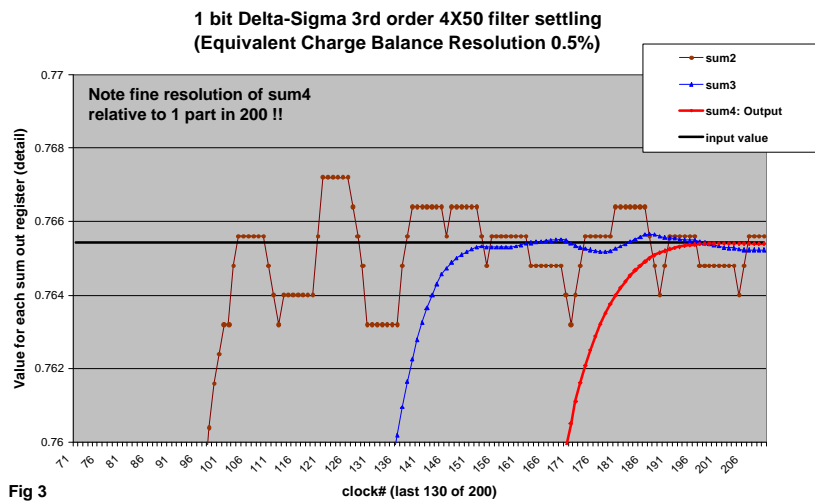


Fig 3

However, the third order integrator output responds to the second and third differentials of the signal and reference waveforms giving it the necessary information for the digital filter to interpolate to the correct output value. For a rigid analysis (in the frequency domain) see [2].

4 Test Overview

DC testing and circuit design analysis were performed to ensure linearity, stability, and overload requirements were met. Since there was not an application need to cope with high slew rates the dynamic testing was performed in the frequency domain using 10Hz-34Hz very pure sine wave signals whilst taking very long data records at the converter’s 1kHz output rate. This data was analysed in special purpose “SATs” software [3] in order that the A-D converter’s dynamic performance could be presented in commonly used specification parameters such as Effective Number of Bits (ENOB). SATS uses algorithms that conform to present IEC standards and also incorporate recommendations of emerging IEC standards [IEEE1241 and DYNAD].

Whilst adequate DC calibration equipment exists to reach these performance levels there is a significant problem for AC testing in finding sources with low enough distortion to be distinguished from that generated by the Device Under Test (DUT). We wanted something greater than -120dB for harmonics of a 34 Hz fundamental and excellent frequency stability over long data acquisition periods. In the event we chose a simple digital function generator, the HP33120A which for 30Hz signals had 2nd and 3rd harmonics -80dB and -84db respectively and we filtered its

the frequency domain can explain this conundrum but in this time domain application we felt it was necessary to gain confidence in the actual characteristics through analysis and operation of a number of simulation models.

Fig. 2 shows one of our simple models, a simulation schematic that was implemented in Excel. In order to more easily see what is happening within its integrators and registers it was designed to fully convert in only 200 clocks (L=50 in fig. 1) such that with true charge

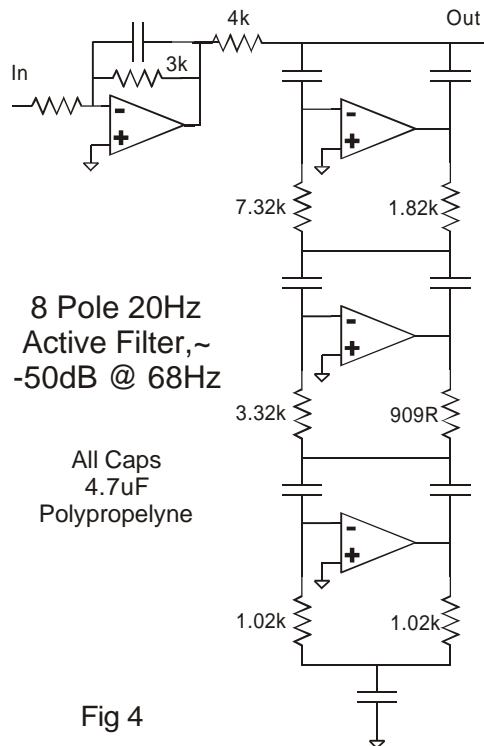


Fig 4

output with an 8 pole modified Bessel filter increasing the purity to better than the required level. Unfortunately the generator also produced some sidebands at about -80dB which interfered with the sampling and hence the FFT analysis which in turn complicated the assessment of results. However, the application only needed to meet dynamic performance to low amplitudes, less than 10% of Full Scale, so the filter was only operated at low signal levels in order to minimise its own distortion. The sidebands could be identified and were not a major contribution at low levels.

One of the most significant problems encountered was observed as strange results in the FFT output which turned out to be due to missing samples in the captured sample records. Both DOS and Windows operation of PCs can cause this and care has to be taken to inspect the sample record to ensure that all expected samples are present and have been acquired regularly.

5 DC tests and performance

The measurements made for DC included environmental tests such as Temperature Coefficient (TC) and a review of the circuits indicated that the stability of components was easily adequate. The remaining tests were essentially functional and the remarkably good results for linearity, measured against a Datron 4800, are shown in Fig 5 and Fig 6. In Fig 5 the input to the A-D is taken from -10 to +10 Volts and the error relative to a best fit straight line plotted as the Y axis, revealing about ± 0.5 ppm. Fig 6 shows detail close to zero indicating that there are no discontinuities. In both cases the error bars represent the estimated uncertainty of measurement due, primarily, to noise. Other DC tests included Common Mode and Power Supply Rejection Ratio, overload recovery, and power-up warm-up time.

Fig 5. Nominal linearity_ppmFS

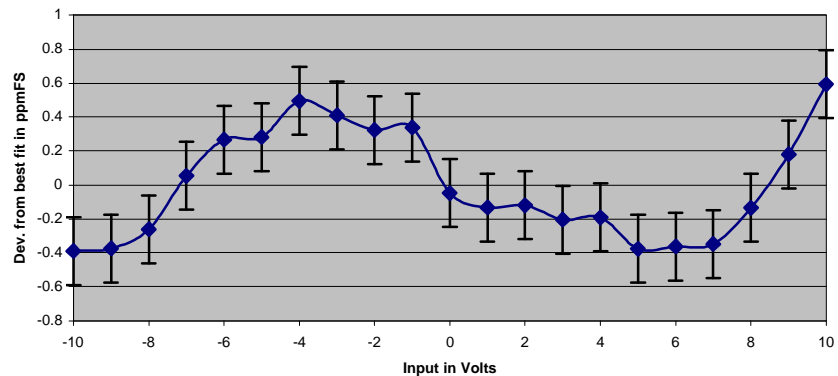
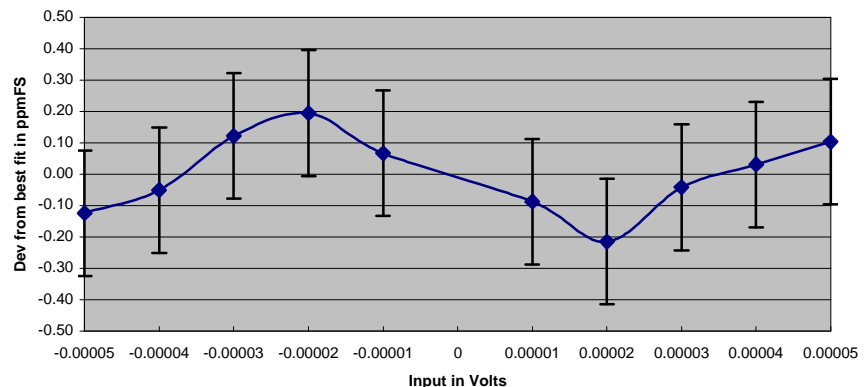


Fig 6 Nominal linearity_ppmFS, detail near zero



6 Dynamic Tests

Extensive dynamic testing was also performed for three basic reasons:

- Dynamic tests can easily and very thoroughly exercise the full range of operation of the A-D
- CERN had requirements for satisfactory operation to about 10Hz
- Low Frequency Dynamic tests, when analysed suitably, give an excellent insight to DC & LF performance and noise.

Many of the dynamic tests were made in the frequency domain, that is, long output records (>1M points) were analysed in the "SATs" software. This had the capability of presenting the measured output as a spectrum (FFT), without the need to synchronise sampling frequency and test frequency, and furthermore to calculate from this data many common A-D parameters such as SINAD (Signal to Noise and Distortion) and ENOB (Effective Number of Bits). It should be remembered that both of these are a function of input signal amplitude and frequency so most of the runs were performed over a number of input amplitudes but we chose to perform most at 34Hz because it gave a good margin over CERN's requirements and we were able to generate the source waveform, through the special filter, particularly cleanly.

One of the observations we made was that the combination of this A-D and the SATs software, with its custom FFT window with -300dB sidelobes, allows a remarkable FFT spectrum analyser to be made with a noise floor more than 140dB down on Full Scale input. Whilst this is only capable of operation to a few tens of Hertz the dynamic range compares very well with commercial units which typically give no better than 80dB .

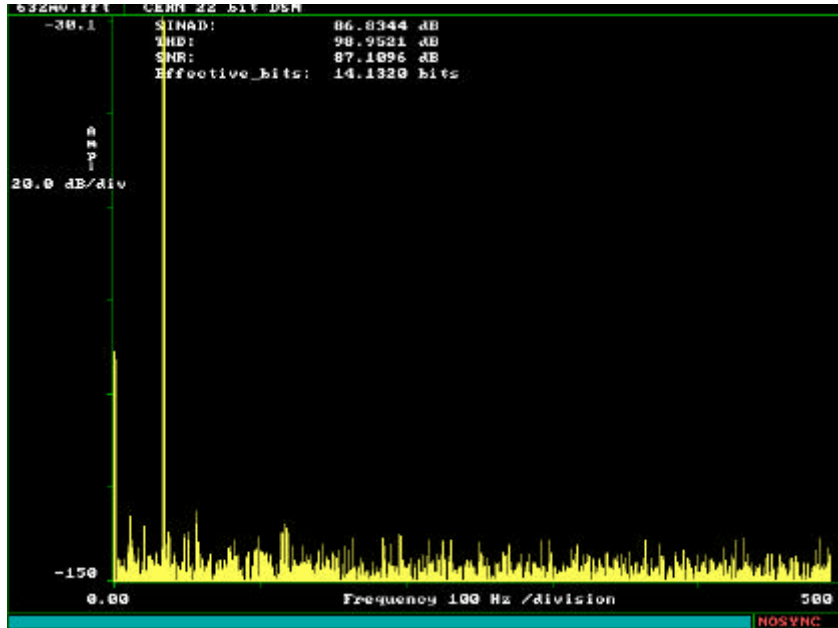


Fig 7
Fig 8

We also performed settling tests from zero to full amplitude by utilising a mercury wetted relay connected to the output of the DC calibrator. One of the settling time results for a zero to 10V step is shown in Fig 9 where it can be seen that settling is fast, circa 30ms to $\ll 10\text{ppm}$, clean and stable.

7 Conclusions

The CERN Delta Sigma Modulator ADC demonstrated an AC performance better than an equivalent ideal 21 bit analogue to digital converter. DC linearity at constant temperature was within $\pm 0.6\text{ ppm}$ of Full Scale input, ie better than $6\mu\text{V}$ in 10V . This is almost as low as the observed noise levels. From this work, aimed at satisfying CERN's particular requirement, it is also evident that this marriage of Sigma-Delta technology with precision circuit techniques has tremendous potential in many metrology applications and also in low-frequency spectrum analysis applications when used with FFT software of sufficiently low window leakage.

8 References

- [1], J G Pett "high accuracy 22 bit sigma-delta etc." adda conf. Glasgow july 99 iee pub 466 p46
- [2], Candy, J., and Temes, G., 1992 "Oversampling Delta-Sigma Converters". IEEE Press New York, USA.
- [3], "WINSATS: a windows based signal analysis and test system software suite", commercially available from: <http://www.signalconversion.com/>

An example of an FFT output is shown in Fig 7 which is a direct screen capture of the SATs software. The input is a 34 Hz sine wave -30dB down on the converter's Full Scale. The displayed ENOB is relative to signal input and so refers to ~ 20 bits referred to Full Scale

Fig 8 shows a summary of many such results indicating the converter's calculated ENOB at different input amplitudes. Since this was performed at 34 Hz one would expect the higher amplitude results to be some 10dB ($1\frac{1}{2}$ to 2 bits) better at the application maximum of 10Hz .

Fig 9

