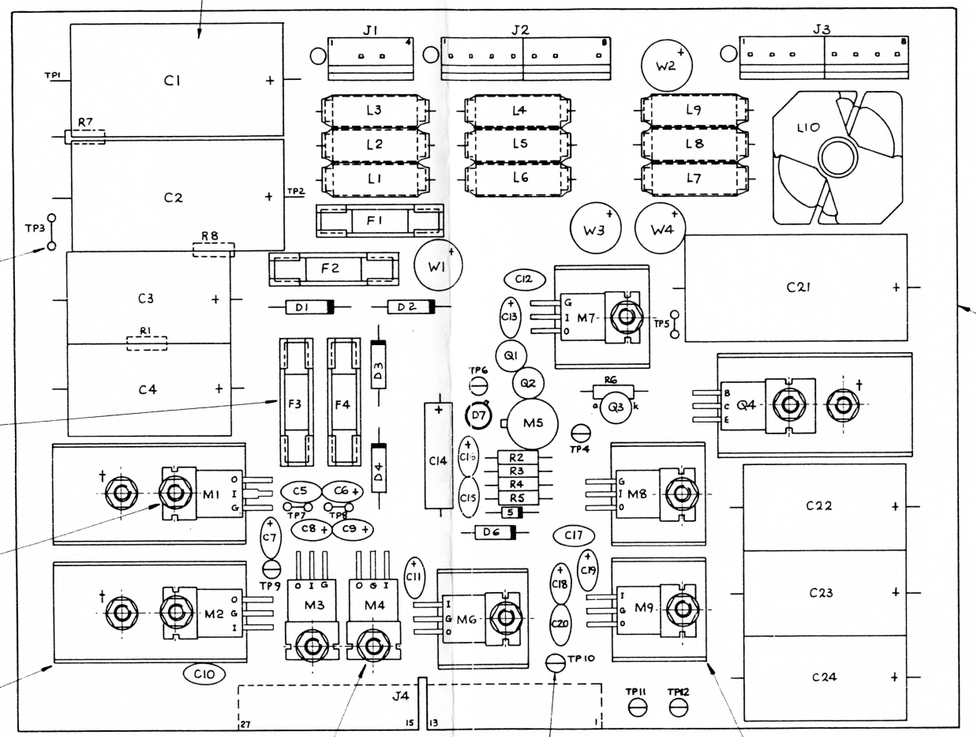
DRAWING No. 400451

ISS.	CHANGES
1	RELEASED 9-3-82
2	ECO 1325 DG WAS 16V JR 13.5.82
3	ECO 1585 D1, D2, D3 AND D4 WERE Z00010 PCB WAS IS JR 15.9.

BED C1 TO C4 AND C21 TO C24 IN SILICONE RUBBER (900004)



MAKE ALL TEST POINT LOOPS FROM 22 SWG BTC WIRE 54.0002

4 OFF FUSE HOLDER 920126
2 OFF FUSE (4A S/B) 920128 — F1, F6
2 OFF FUSE (2A S/B) 920127 — F3, F4

M1, M2 † Q4 FIXINGS
- 3 OFF SCREW M3X 8 mm POZIPAN 611016
- 3 OFF NUT M3 FULL HEX 615002
- 3 OFF WASHER M3 SHAKEPROOF 613005

† HEATSINK — PCB FIXING
- 3 OFF HEATSINK (TO 220 × 2) 920090
- 3 OFF SCREW M3 × 8mm POZIPAN 611016
- 3 OFF NUT M3 FULL HEX 615002
- 3 OFF WASHER M3 SHAKEPROOF 613005

2 OFF SCREW M3x8mm POZIPAN 611016
2 OFF NUT M3 FULL HEX 615002
2 OFF WASHER M3 SHAKEPROOF 613005

TEST POINT TERMINAL 620007 6 OFF.

4 OFF HEATSINK (TO 220) 920089
4 OFF SCREW M3 × 8 POZIPAN 611016
4 OFF NUT M3 FULL HEX 615002
4 OFF WASHER M3 SHAKEPROOF 613005.

PCB 410160-6A

NOTE: USE HEATSINK COMPOUND (900003) BETWEEN MATING SURFACES OF Q4, M1-M2, M6-M9 AND THE RESPECTIVE HEATSINKS. A TORQUE OF 0·5Nm SHOULD BE APPLIED TO TIGHTEN COMPONENT FIXINGS.

DRAWN IL	DATE 3.3.82	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± 4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400451	TITLE: 4000 IN-GUARD POWER SUPPLY PCB ASSY.
CHECKED MJD	DATE 9.3.82.	SCALE 2:1	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM 430451	DRAWING No. 400451
APPR. D Hume	DATE 17-3-82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460451 CHECK LIST 470451	SHEET 1 OF 5

datron ELECTRONICS LIMITED NORWICH

E.B.W.

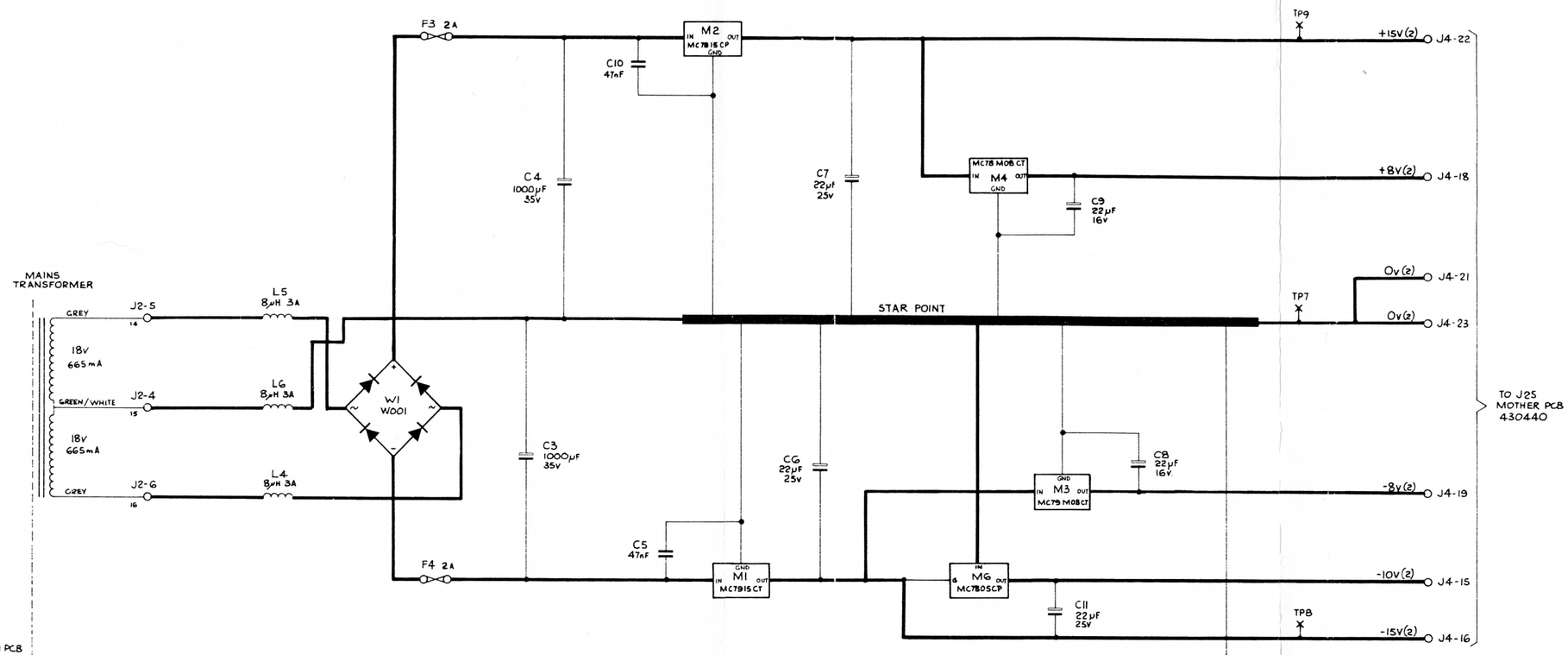
4951MT

218

DRAWING No. 430451

IN GUARD COMMON 2 SUPPLIES

ISS	CHANGES
1	RELEASED 9.3.82
2	ECO 1325 D6 WAS 18V JR 13.5.82



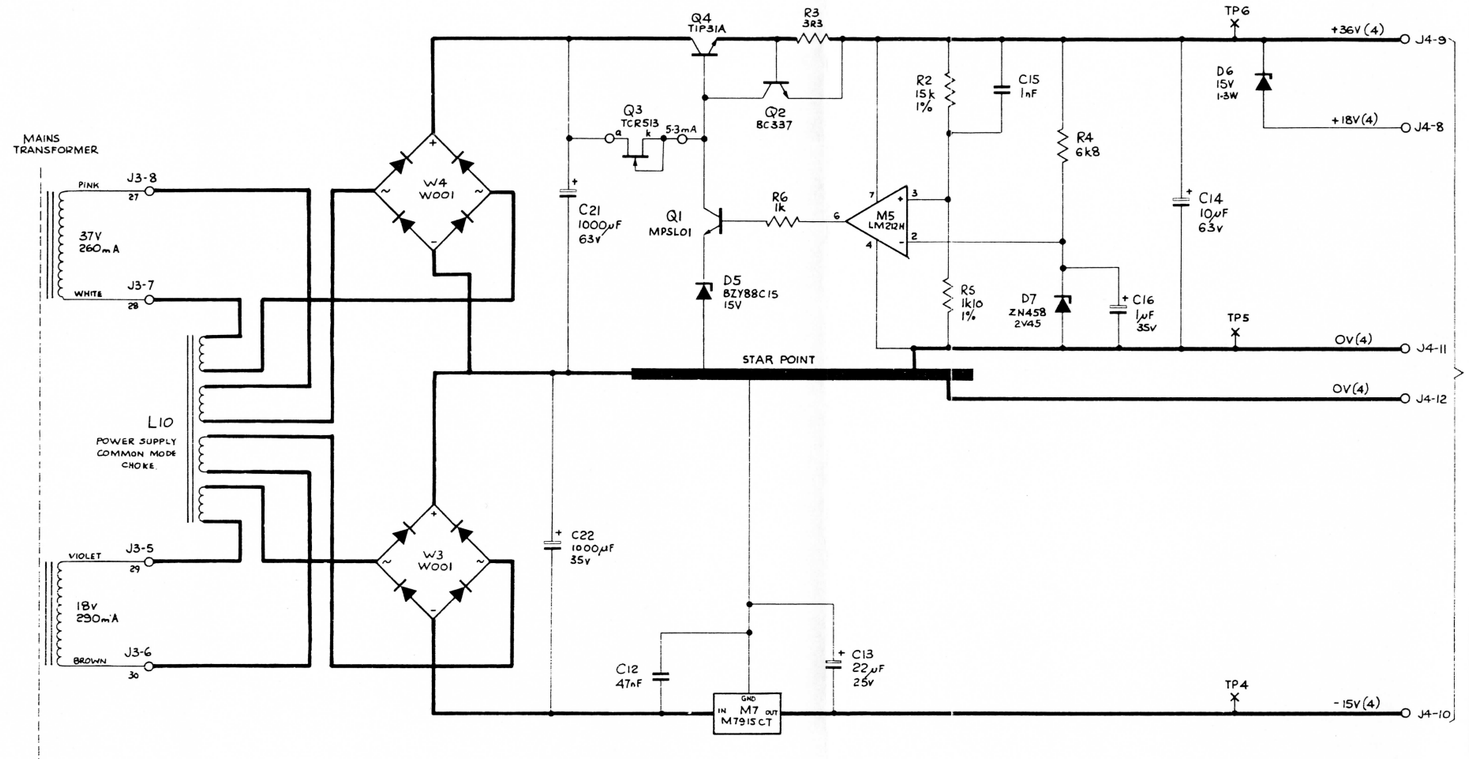
DRAWN JL	DATE 3.3.82.	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± 2mm; WHOLE DIMENSIONS ± 4mm; ANGULAR ± ½°	MATERIAL —	ASSY DRG & PARTS LIST 400451	TITLE 4000 POWER SUPPLY IN-GUARD	DRAWING No. 430451
CHECKED R.K. COGGAN	DATE 9-3-82	SCALE —	UNLESS OTHERWISE STATED	FINISH —	CIRCUIT DIAGRAM 430451		
APPR. B Jeune	DATE 17-3-82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460451; CHECK LIST 470451		SHEET 1 OF 2

datron ELECTRONICS LIMITED NORWICH

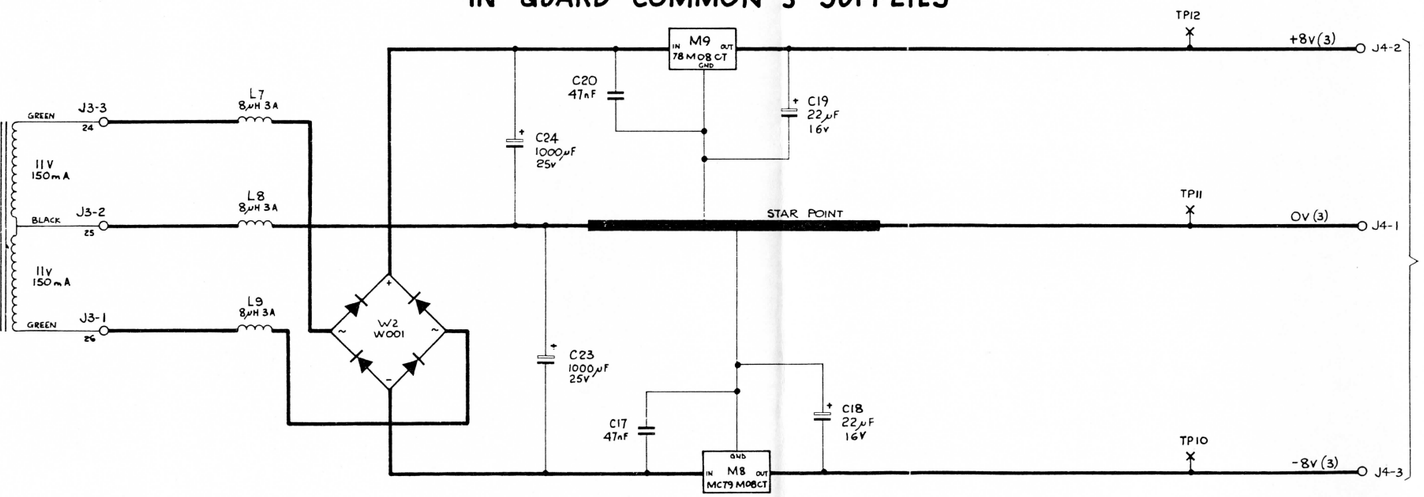
E.B.W. 4951MT

DRAWING No. 430451

REFERENCE DIVIDER COMMON 4 SUPPLIES



IN GUARD COMMON 3 SUPPLIES



ISS.	CHANGES
1	RELEASED 9-3-82
2	ECO 1325 DG WAS 18V JR 13 5 82

DRAWN IL	DATE 3.3.82.	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± 1mm; DECIMAL TO 1 PLACE ± 2mm; WHOLE DIMENSIONS ± 4mm; ANGULAR ± ½°	MATERIAL ———	ASSY DRG &	400451	TITLE 4000 POWER SUPPLY IN-GUARD
CHECKED R.K. COGGAN	DATE 9-3-82	SCALE ———	UNLESS OTHERWISE STATED	FINISH ———	PARTS LIST		
APPR. B Vane	DATE 17-3-82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CIRCUIT DIAGRAM	430451	
					CHECK PROCEDURE	460451	
					CHECK LIST	470451	

datron ELECTRONICS LIMITED NORWICH

DRAWING No. 430451

SHEET 2 OF 2

E.B.W.

4951MT

DRAWING No. 400449

RELAY PIN Nº	WIRE LENGTH
1	30mm
4	20mm
5	50mm
6	60mm
7	90mm
8	90mm
9	100mm
10	60mm

SLEEVE ALL WIRE CONNECTIONS BEFORE SOLDERING- USING SLEEVE 590001 (X½)

ALL RELAY LEADS MADE FROM 7/·2 PTFE INSULATED (WHITE) WIRE CUT + STRIP EACH END 5mm BEFORE SLEEVING + SOLDERING.

PIN 10, PIN 6, PIN 7, To PIN 8, To PIN 9, To PIN 5, To PIN 4, To PIN 1, RL3

WIRE LINK (X20mm) 540002

(VIOLET) CIRCUIT BOARD EJECTOR 2 OFF. 630123.

FUSE HOLDER (F1, F2 + F3) 920126

MOUNT R23, R24, R36, R49 + R115 ON CERAMIC BEADS. 630024 10 OFF.

FIT L1-L3 + L6 TO PCB AFTER 'FLOW-SOLDERING' BOARD.

PCB 410203-4A

HEATSINK (TO220 VERT) 920091 4 OFF
SCREW M3×8mm POZI-PAN 611016 4 OFF
WASHER M3 FLAT PLAIN. 613007 4 OFF
WASHER M3 SHAKEPROOF 613005 4 OFF
NUT M3 HEX FULL 615002 4 OFF

HEATSINK (TO202 HORIZ) 920105 2 OFF
SCREW M3×8mm POZI-PAN 611016 2 OFF
WASHER M3 SHAKEPROOF 613005 2 OFF
NUT M3 HEX FULL 615002 2 OFF

SOLDER TERMINAL 15 OFF 620003

REMOVE 5 PINS SHOWN THUS ::

J1, J2, J3, J4, J5, J6, J9, S1, D37, L6, R65, R77, R78, R79, R80, R81, R82, R115, RL1, RL2, RL3, F1, F2, F3, L1, L2, L3, L4, L5, L7, L8, L9, L10, L11, L12, R1, D1, D2, D12, D13, D15, D16, C3, C10, C15, C25, C26, C28, C32, C34, C48, C53, C56, C58, C59, C60, C66, C67, M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, Q22, Q23, Q24, Q25, Q41, Q42, TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP32, TP33, TP34, TP35, TLA, TLB, TLC, TLD, TLE, TLF, TLG, TLH, TLJ, HV ENBL, DISBL, PIN 1, PIN 2, PIN 3

SLEEVE LEADS OF R145/R146 BEFORE SOLDERING. USE PTFE SLEEVE 590004. FIT CERAMIC BEAD. 630036 (2 OFF) UNDER BODY OF RESISTOR.

MOUNT D15 + D16 ON MOUNTING PAD 618004 2 OFF

CUT TRACK AT POSITION MARKED * (NEXT C73). CUT TRACK BETWEEN C72 + C73. TOP SIDE OF PCB. LINK CAPS AS SHOWN TO M2 ON UNDERSIDE OF PCB. SLEEVE WIRE BEFORE SOLDERING. 540002/590004.

LACING CORD 590007 2 POSITIONS

TEST POINT TERMINAL 620007 30 OFF.

TEST POINT LOOPS MADE FROM 22 SWG BTC WIRE 540002.

FIT R147 + R148 THUS.

NOTE: USE HEATSINK COMPOUND BETWEEN MATING SURFACES OF Q22, Q23, Q24, Q25, Q41 + Q42 AND THE RESPECTIVE HEATSINKS 900003 A TORQUE OF 0·5 Nm. SHOULD BE APPLIED TO TIGHTEN COMPONENT FIXING.

WIRE LEAD BETWEEN SOLDER TERMINALS A + K, B + C ETC., 7/·2 PTFE COVERED WIRE (WHITE) 540008 SLEEVE TERMINATIONS WITH SLEEVE 590001 (X½)

WIRE LENGTH	
A TO K	100mm
B TO C	240mm
D TO E	220mm
F TO G	220mm

RELAY BRACKET 459112 1 OFF
RELAY NUT 3-48 UNC 615005 1 OFF
SCREW M3×8mm POZI-PAN 611016 1 OFF
WASHER M3 SHAKEPROOF 613005 1 OFF
NUT M3 HEX FULL 615002 1 OFF
WASHER M2·5 SHAKEPROOF 613014 1 OFF (RELAY)

'CONSTANT CURRENT' PLUG-IN PCB ASSY 400472 MOUNT ON CERAMIC BEAD 630036 3 OFF

I.C. MOUNTING			
Nº WAYS	PART Nº	Nº OFF	USED TO MOUNT
8	605059/A	6	M1-M5, M11
14	605060/A	1	M10
16	605061/A	2	M7, M8
6	605066/A	1	M9

ISS.	CHANGES
1	RELEASED 16.4.82
2	ECO 1331 C41 WAS 4·n7 500V CER. DISC. C8, 16, 14, 26, 40 AND 4·7 WERE 4·7n 63V POLYESTER. JR 17.5.82
3	ECO 1353, 15 R115 NOW MOUNTED ON CERAMIC BEAD. M6 SOCKET REMOVED PLUS PARTS LIST CHANGE. JR 5.7.82
4	ECO 1364, 1366, 1368, 1375, 1381, 1382. R65 WAS 20k POT. R36/R66 KIT WAS 155.1. C4/C9 DELETED. C72/C73 ADDED. D7/D8 DELETED. R145/R146 ADDED. R23, R24, R36 + R49 NOW MOUNTED ON CER. BEADS 630024. R145, R146 MOUNTED ON CER. BEAD 630036. R37/R43 WERE 22k. 23.8.82
5	ECO 1458. RQ WAS 6KQ. 8·4·83. BJ. Cont...
6	ECO 1518 R147 AND R148 ADDED JR 16·8·83
7	ECO 1529 D1, 2, 12 AND 13 WERE 200010 PCB WAS 155.4 JR 15·9·83

DRAWN IL	DATE 1.3.82	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± 1mm; DECIMAL TO 1 PLACE ± 2mm; WHOLE DIMENSIONS ± 4mm; ANGULAR + ½°	MATERIAL	ASSY DRG & PARTS LIST 400449	TITLE 4000 POWER AMP (D.C) PCB. ASSY.	datron ELECTRONICS LIMITED NORWICH
CHECKED MJ	DATE 16.4.82	SCALE 2:1	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM 430449		DRAWING No. 400449
APPR. B Thorne	DATE 23.4.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460449 CHECK LIST 470449		SHEET 1 OF 21

E.B.W.

4651MT

207

DRAWING No. 430449

ISS	CHANGES
1	RELEASED 16.4.82
2	ECO 1331 SEE SHT 5. MD
3	SEE SHT 2. MD
4	SEE SHTS. 2 + 5 MD
5	SEE SHEET 2. MD
6	ECO 1518 R147 AND R148 ADDED. JPR 12.8.83 MD

DC STABILISATION

POWER AMPLIFIER

OUTPUT CLAMP

FROM C36 SHT. 4 — PA DRIVE

FROM R133 SHT. 3 — I LIM

FROM M2 PIN 6 SHT. 4 — PA 1kV

FROM M1 PIN 5 SHT. 2 — -2.5V REF

FROM M1 PIN 2 SHT. 2 — +2.5V REF

PA OFF 8

FROM Q43 SHT. 4

TO RL2 PINS 7 + 10 SHT. 3.

PA OUTPUT

POSITIVE HEATSINK ASSY 400454

NEGATIVE HEATSINK ASSY 400461

SET BIAS

DRAWN IL	DATE 17.3.82	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± 1mm; DECIMAL TO 1 PLACE ± 2mm; WHOLE DIMENSIONS ± 4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400449
CHECKED F.B.S.	DATE 23.4.82	SCALE —	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM
APPR. D Hume	DATE 23.4.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460449; CHECK LIST 470449

TITLE: 4000. POWER AMP (D.C.) D.C. POWER AMPLIFIER

datron ELECTRONICS LIMITED NORWICH

DRAWING No. 430449

SHEET 1 OF 5

E.B.W.

4951MT

208

DRAWING No. 430449

+50V CURRENT LIMIT

+50V REGULATOR

±50V POWER SUPPLY SHUTDOWN

−50V REGULATOR

−50V CURRENT LIMIT

ISS.	CHANGES
1	RELEASED 16.4.82
2	ECO 1331 SEE SHT 5
3	ECO 1356 R37 AND R43 WERE 12K. D21 AND D24 WERE 30V. JR 5.7.82.
4	ECO 1368 C4/C9 DELETED C72/C73 ADDED R37 R43 WERE 22k IL 23.8.82
5	ECO 1456 RG WAS 5K6. B.4.83
6	ECO 1518 SEE SHEET 1.

DRAWN IL	DATE 17.3.82	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± 1mm; DECIMAL TO 1 PLACE ± 2mm; WHOLE DIMENSIONS ± 4mm; ANGULAR ± ½° UNLESS OTHERWISE STATED
CHECKED D.B.S.	DATE 23.4.82	SCALE ——	MATERIAL ——
APPR. B Howe	DATE 23.4.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION; FINISH ——

ASSY DRG & PARTS LIST	400449
CIRCUIT DIAGRAM	
CHECK PROCEDURE	460449
CHECK LIST	470449

TITLE: 4000 POWER AMP (DC) ±50V POWER SUPPLY

datron ELECTRONICS LIMITED NORWICH

DRAWING No. 430449

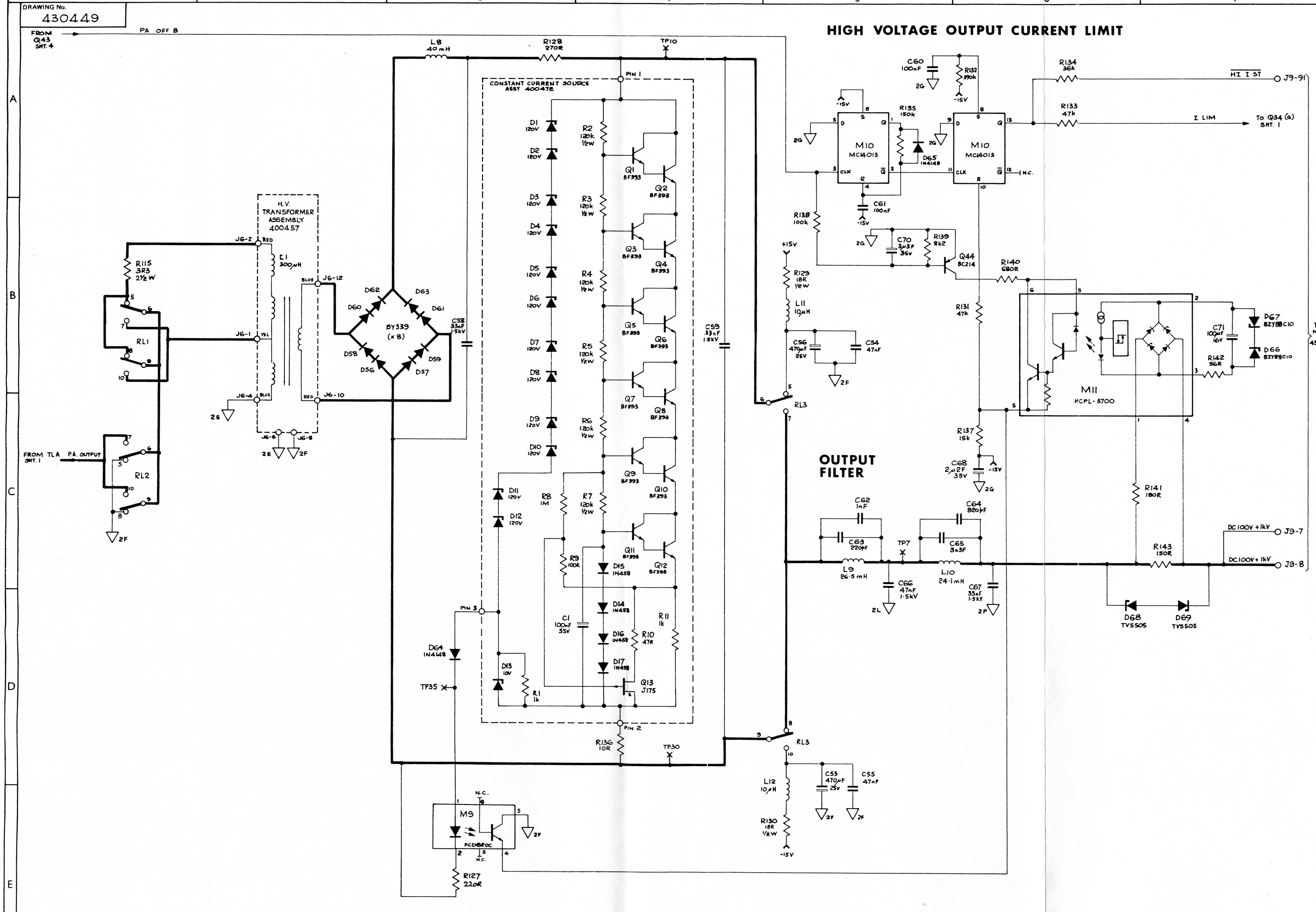
SHEET 2 OF 5

E.B.W.

DRAWING No. 430449

ISS.	CHANGES
1	RELEASED 16.4.82
2	ECO 1331 SEE SHT 5.
3	SEE SHT 2.
4	SEE SHTS. 2 4 +5
5	SEE SHT 2
6	ECO 1518 SEE SHEET 1.

HIGH VOLTAGE OUTPUT CURRENT LIMIT



DRAWN	DATE 17.3.82	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400449	TITLE: 4000. POWER AMP (DC) HIGH VOLTAGE OUTPUT.
CHECKED	DATE 23.4.82	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM	
APPR.	DATE 27.4.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460449	
					CHECK LIST 470449	

datron ELECTRONICS LIMITED NORWICH

DRAWING No. 430449

SHEET 3 OF 5

DRAWING No. 430449

ISS.	CHANGES
1	RELEASED 16.4.82
2	ECO 1331 SEE SHEET 5.
3	SEE SHT 2
4	ECO 1364. R65 WAS 20k POT. IL 23.8.82
5	SEE SHEET 2.
6	ECO 1518 SEE SHEET 1.

VOLTAGE CONTROLLED AMPLIFIER

16kHz SQUARE TO SINE FILTER

* N.B. Q26 & R66 = KIT 239051 (237R, 267R, 301R, 340R)

J9-86 16kHz (IG) — R122 47k — M8 — C38 330pF — C39 1nS — R64 4k75 1% — L7 10mH — R60 392R 1% — TP16 — R62 100R 1% — C32 10nF — R61 681R 1% — 2H

D48 IN4148

C27 1nSF — C30 47pF — R59 10k 1% — M3 NE5534N — TP15 — Q26 U1897 — R67 4k75 1% — M4 NE5534N — C31 47nF — C33 47pF — R66 1% — C28 220µF 40V — TP19 — C36 220nF — PA DRIVE — TO R87 SHT. 1

+15V — R56 2R2 — C37 47nF — R57 2R2 — -15V

J9-83 VCA CTRL — C29 22µF 25V — D36 6V8 — TP24 — TLC — R63 4k75 1% — Q28 TCR509 2·5mA — R65 100k — TLB — C34 100µF 40V — R68 100R — -15V

D40 HSCH1001

MAKE TLB, BREAK TLC FOR MANUAL CONTROL.

DECODING LOGIC

J9-95 +15V(2) — L4 10µH — +15V

TO D47 SHT. 1 + R38 SHT. 3 — PA OFF B

J9-94 OFF — TLH — TLJ — J9-89 PA OFF — TO J9 MOTHER PCB 430440

R124 1M — 2G — M8 — R121 22k — Q43 BC214 — -15V

RL3 — RL1 — S1a — HIGH VOLTAGE DISABLE — RL2 — S1b — R77 1k5 — D37 521-9165 — 2G

+15V

J9-48 POSITIVE — J9-47 HV ENBL — R125 1M — R126 1M — -15V

M7 XR2202 — N.C. — N.C.

J9-55 DC ST — R98 15k — -15V

J9-53 BARK — R123 4k7 — 2G

D55 TVS15 — C57 47nF — M8 4050 — M10 4013 — 2G

J9-96 -15V(2) — L5 10µH — -15V

PA 1KV — To R72 SHT. 1

COMMON INTERCONNECTIONS

POWER SUPPLY CAPACITORS (MOTHER BOARD) — STAR POINT — 2N

MAINS TRANSFORMER

50 VOLT POWER SUPPLY — 2M — 2D — 2C

DC POWER AMPLIFIER — 2A — 2B

HV TRANSFORMER PRIMARY — 2E

HV TRANSFORMER SECONDARY — 2F

LOGIC — 2G

VCA — 2H

HIGH VOLTAGE OUTPUT FILTER — 2P — 2L

STAR POINT — TP27

0V(2) — J9-97, J9-98, J9-99, J9-100, J9-101, J9-102

0V(2) — J9-105

0V(2) — J9-107

0V(2) — J9-81

0V(2) — J9-85

TO J9 MOTHER PCB 430440

DRAWN	DATE 18.5.82	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± 1mm; DECIMAL TO 1 PLACE ± 2mm; WHOLE DIMENSIONS ± 4mm; ANGULAR ± ½°
CHECKED T.B.S.	DATE 23.4.82	SCALE — NOT TO BE SCALED	UNLESS OTHERWISE STATED: FIRST ANGLE PROJECTION
APPR.	DATE 23.4.82		MATERIAL — FINISH —

ASSY DRG & PARTS LIST	400449
CIRCUIT DIAGRAM	
CHECK PROCEDURE	460449
CHECK LIST	470449

TITLE: 4000 POWER AMP (DC) FILTER, VCA AND DECODING LOGIC

datron ELECTRONICS LIMITED NORWICH

DRAWING No. 430449

SHEET 4 OF 5

211

DRAWING No.	FIRST USED ON
430449	

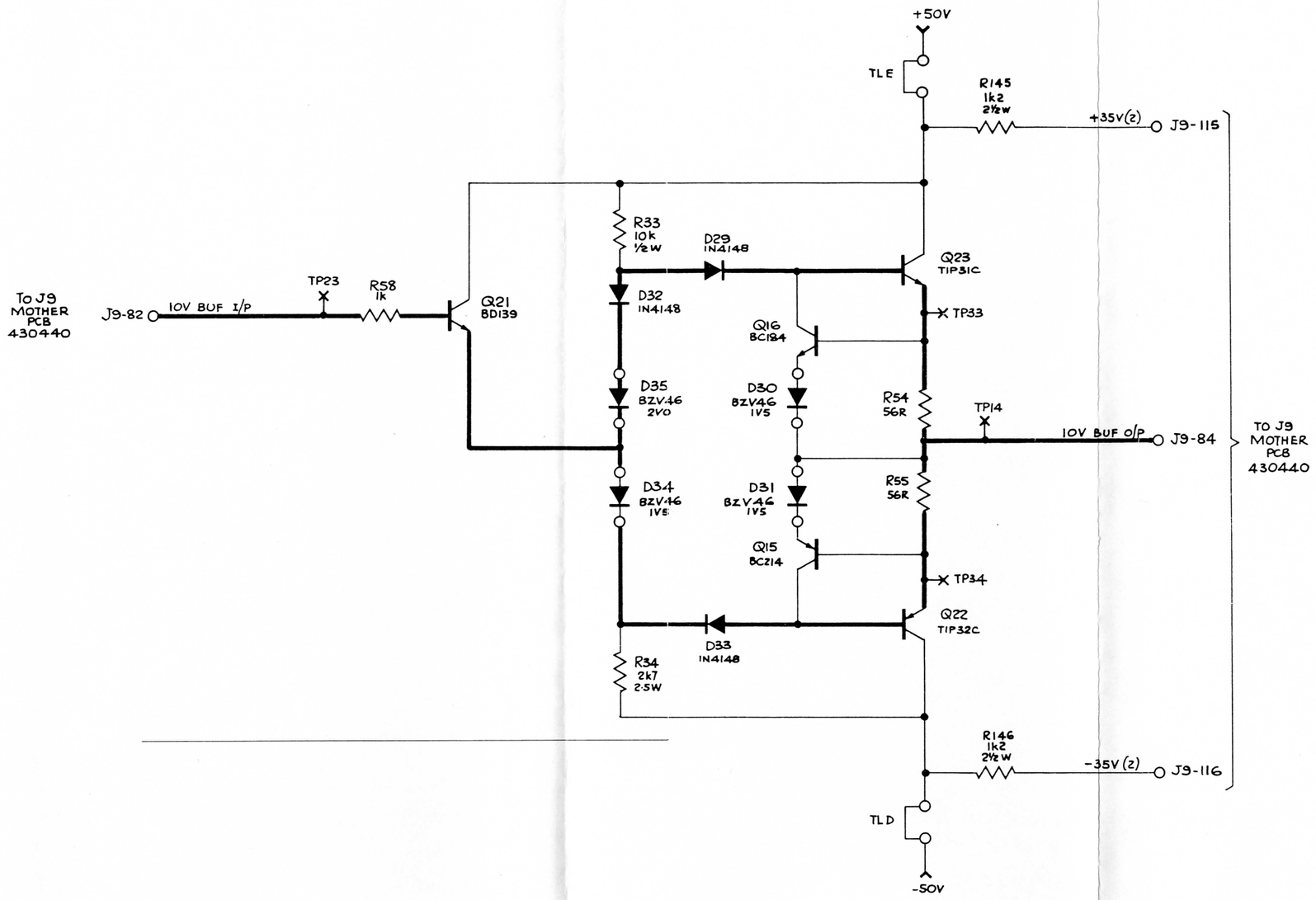
THIRD ANGLE PROJECTION

DRAWN IN ACCORDANCE WITH BS 308

ALL BURRS TO BE REMOVED

NOTES

ISS.	CHANGES
1	RELEASED 16.4.82
2	ECO 1331 D7 AND D8 WERE BZY88C-15V JR 17.5.82
3	SEE SHT 2.
4	ECO. 1375 D7/D8 DELETED R145/R146 ADDED IL. 23.8.82
5	SEE SHEET 2.
6	ECO 1518 SEE SHEET 1



DRAWN IL.	DATE 18.3.82	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR ± ½°	MATERIAL ——	ASSY DRG & PARTS LIST 400449	TITLE 4000. POWER AMP (DC) 10V DC BUFFER AMP	DRAWING No. 430449
CHECKED J.B.S.	DATE 23·4·82	SCALE ——	UNLESS OTHERWISE STATED	FINISH ——	CIRCUIT DIAGRAM		
APPR. B Hume	DATE 23·4·82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460449; CHECK LIST 470449		SHEET 5 OF 5

datron ELECTRONICS LIMITED NORWICH

4951MT

221

DRAWING No. 400470

ISS.	CHANGES
1	RELEASED 17.3.82
2	ECO 1314. 1324 C1 DELETED R5 AND R6 CHANGE VALUE. R20, C9 AND C10 ADDED. JR 14-5-82
3	ECO 1447. BJ TP8 & TP9 ADDED. 14th FEB 83.
4	ECO 1498. D MOUNTED ON C BEADS. BJ. 8-4-83. ECO 1478. C9 VALUE CHANGE WAS 1000n.
5	ECO 1504 R13 WAS CR25. JR 12-8-83.
6	ECO 1529 D1 AND D2 WERE 200010. PCB WAS ISSUE 3. JR 15.12.83

BED C5 & C7 ON P.C.B WITH SILICONE RUBBER COMPOUND 900004.

LINKS TO BE MADE FROM TINNED COPPER WIRE SLEEVED WITH PTFE SLEEVING 590004

2 OFF 4 WAY .156" LOCKING RAMP 604042 MOUNT ON UNDERSIDE.

2 OFF 2 x TO220 HEATSINKS 920090
2 OFF M3 X 6mm POZIPAN SCREW 611004
2 OFF M3 X 10mm POZIPAN SCREW 611006
4 OFF M3 SHAKEPROOF WASHER 613005
4 OFF M3 HEX NUT 615002
2 OFF M3 FLAT STEEL WASHER 613007
USE M3 X 10mm ON Q3 AND Q4 WITH A FLAT AND SHAKEPROOF WASHER UNDER NUT

TEST POINTS TO BE MADE FROM 22 SWG TINNED COPPER WIRE 540002 (TP5 & TP6).

1 OFF 4A FUSE 20mm 920128
1 OFF PCB MT FUSE HOLDER 920126

1 OFF M3 X 6mm POZIPAN SCREW 611004
1 OFF M3 SHAKEPROOF WASHER 613005
1 OFF M3 HEX NUT 615002

1 OFF 8 WAY DIL SOCKET 605059

MOUNT R7 ON STEATITE BEADS 630024 4 OFF

MOUNT C4 FLAT TO THE P.C.B AS SHOWN.

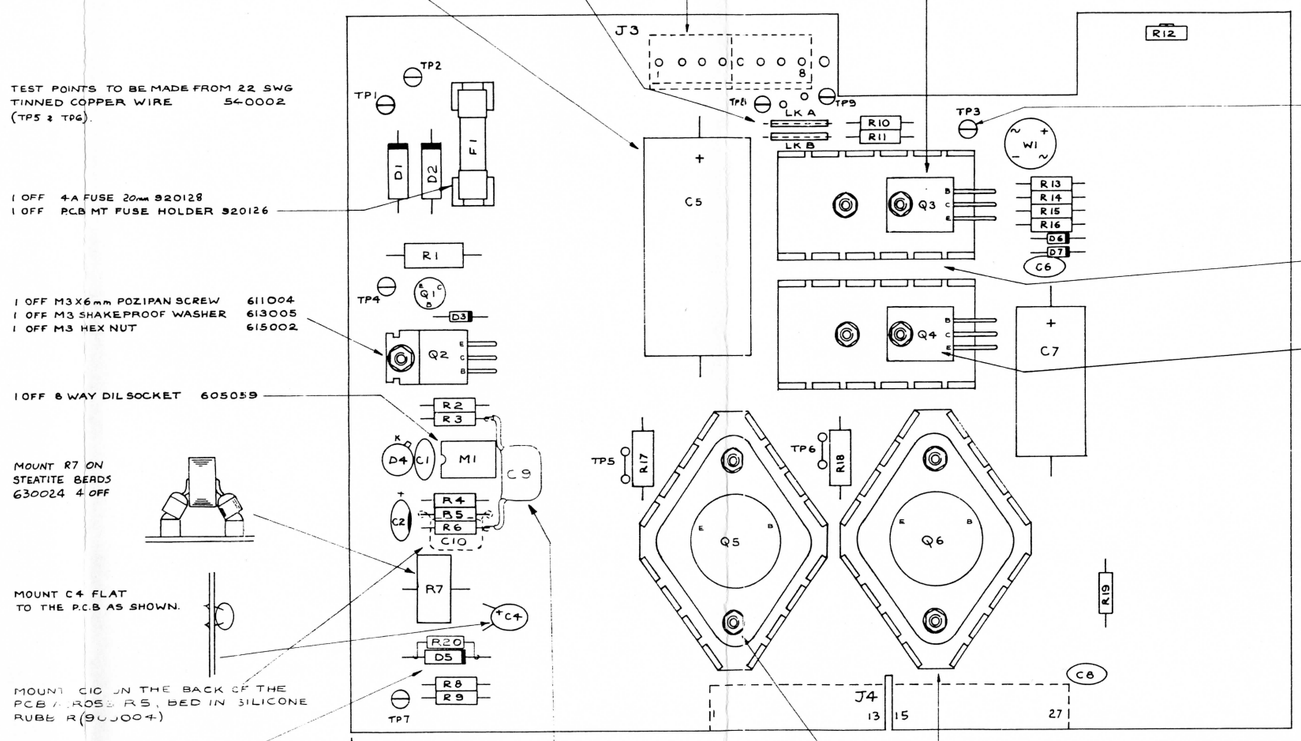
MOUNT C10 ON THE BACK OF THE PCB ACROSS R5, BED IN SILICONE RUBBER (900004)

MOUNT D5 ON STEATITE BEADS 630024 2 OFF.

TEST POINT TERMINAL 620007 7 OFF.

ENSURE THAT THERE IS A GAP OF AT LEAST 5mm BETWEEN HEATSINKS.

FIT Q3 AND Q4 WITH GOLD SIDE TO HEATSINK



PCB 410179-3A

SLEEVE LEADS OF C9 (590004) AND BED IN SILICONE RUBBER (900004)

NOTE USE HEATSINK COMPOUND BETWEEN MATING SURACES OF Q3,4,5 & 6 AND THE HEATSINKS, THEN USING A TORQUE SCREW DRIVER TIGHTEN TO TORQUE OF 0.5 Nm. (HEATSINK COMPOUND 920003)

2 OFF TO3 HEATSINK 920088
4 OFF M3 X 10mm POZIPAN SCREW 611006
4 OFF M3 SHAKEPROOF WASHER 613005
4 OFF M3 HEX NUT 615002
1 OFF M3 FLAT STEEL WASHER 613007
USE FLAT STEEL WASHER UNDER SCREW HEAD ON BACK OF PCB.

DRAWN JR	DATE 13-11-81	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± 1mm; DECIMAL TO 1 PLACE ± 2mm; WHOLE DIMENSIONS ± 4mm; ANGULAR ± ½°	MATERIAL ——	ASSY DRG & PARTS LIST 400470	TITLE 4000 OUT GUARD POWER SUPPLY ASSY	DRAWING No. 400470
CHECKED MJD	DATE 18.3.82	SCALE 2:1	UNLESS OTHERWISE STATED	FINISH ——	CIRCUIT DIAGRAM 430470		
APPR. B Hume	DATE 22-3-82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460470		SHEET 1 OF 5
					CHECK LIST 470470		

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4951MT

220

DRAWING No. 430470

ISS.	CHANGES
1	RELEASED 17.3.82
2	ECO 1314, 1324. C1 DELETED R5 WAS 1K24 R6 WAS 1K18 R20, C9 AND C10 ADDED. UPA 14.582. MC
3	ECO 1447. 14-5-85. TP8 & TP9 ADDED. BA

DIGITAL MAIN SUPPLY

MAINS TRANSFORMER

BLUE — J3-1 — 6 — D1 3051 3A
8·8v 1·5A
VIOLET — J3-3 — 7
8·8v 1·5A
BLUE — J3-2 — 8 — D2 3051 3A

F1 4A

R1 0R27 2½W — TP4
R17 0R27 ½W — TP5 — Q5 MJ2955
R18 0R27 ½W — TP6 — Q6 MJ2955
Q1 BC327

C5 4700µF 16v

Q2 TIP31A
R3 1K0
M1 CA3140
C9 100nF C280
C10 47n C280
R9 47R
R5 39K2 1%
R4 1K8
R6 37K4 1%
R8 47R
R2 33R
D3 2V7 BZY88
D4 2V45 ZN458
C2 1µF 35v
C4 100nF 16v
R20 220R
D5 5v TVS505

TP1 — +8v(UNREG) — J4-12
TP7 — +5v — J4-15, J4-16
+5v SENSE — J4-10
DIG COM SENSE — J4-9
TP2 — DIG COM — J4-1; DIG COM — J4-2; LED COM — J4-3
EARTH — J4-23

STAR POINT

R7 VA8650

J3-4 — EARTH

TO J20 MOTHER P.C.B 430440 (J4-23 ALSO GOES TO REAR PANEL EARTH SCREW)

PRIMARIES SHOWN ON INTERCONNECTION P.C.B. 430439

DISPLAY SUPPLY

ORANGE — J3-6 — 9
180v 44 mA
YELLOW — J3-7 — 10

W1 W006

C7 10µF 350v

R13 180K
D6 6V8 BZY88
R16 220R
Q3 MJE340
D7 180v IN5279B
R15 1K0
R14 1K0
Q4 MJE340
C6 10nF
TP3

+5v(LED) — J4-21
-175v — J4-19

COMMON MODE NULL (O.G.)

WHITE — J3-5 — 11 — TP8 — LKA
180v 5mA
PINK — J3-8 — 12 — TP9 — LKB

R10 100k 1%
R11 100k 1%
R12 2M
R19 100K
C8 100pF 4kV

GU — J4-27

TO J4-27 P5 (1G) P.C.B 430451

DRAWN JR	DATE 7·12·81	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± 1mm; DECIMAL TO 1 PLACE ± 2mm; WHOLE DIMENSIONS ± 4mm; ANGULAR ± 30; UNLESS OTHERWISE STATED	MATERIAL —	ASSY DRG & PARTS LIST	400470	TITLE 4000 POWER SUPPLY OUT GUARD
CHECKED RH·COGGAN	DATE 18-3-82	SCALE —		FINISH —	CIRCUIT DIAGRAM	430470	
APPR. B Vlems	DATE 22·3·82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE	460470	
					CHECK LIST	470470	

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DRAWING No. 430470

SHEET 1 OF 1

4951MT

DRAWING No. 430439

ISS.	CHANGES
B	5·8·81
1	29th MAR 82 RELEASED. BJ.
2	C1 ADDED. ECO 14666 BJ. 14th APRIL 82.

J1 TO J17
J2 TO J18
MOTHER PCB
430440

J1 - 13	DIO 1	J 27 - 1
J1 - 7	DIO 2	J 27 - 2
J1 - 6	DIO 3	J 27 - 3
J1 - 4	DIO 4	J 27 - 4
J2 - 10	EOI	J 27 - 5
J2 - 12	DAV	J 27 - 6
J1 - 16	NRFD	J 27 - 7
J1 - 3	NDAC	J 27 - 8
J1 - 2	IFC	J 27 - 9
J1 - 1	SRQ	J 27 - 10
J2 - 13	ATN	J 27 - 11
		J 27 - 12
J1 - 14	DIO 5	J 27 - 13
J1 - 8	DIO 6	J 27 - 14
J1 - 5	DIO 7	J 27 - 15
J2 - 9	DIO 8	J 27 - 16
J2 - 11	REN	J 27 - 17
J2 - 14	BUS COM	J 27 - 18
J2 - 15		J 27 - 19
		J 27 - 20
		J 27 - 21
		J 27 - 22
		J 27 - 23
		J 27 - 24

REAR PANEL IEEE 488 CONNECTOR

C1 0·01μF CER DISC

J2 - 1	+5V	J 3 - 1	ORANGE	CALIBRATION ENABLE
J1 - 12	CAL / $\overline{\text{RUN}}$	J 3 - 4	ORANGE	
		J 3 - 2 - J 3 - 3		NOT USED
J2 - 2	EXT FREQ HI	J 4 - 1	BROWN	J 53 - 1
J2 - 3	EXT FREQ LO	J 4 - 2	BLACK	J 53 - 2
J1 - 15	EXT RST	J 4 - 3	RED	J 53 - 3
		J 4 - 4	NOT USED	REAR PANEL CONNECTOR

J1 TO J17
J2 TO J18
MOTHER PCB
430440

IEEE 488 ADDRESS SELECTOR SWITCH

J2 - 16	ADD SW 1	S1
J2 - 8	ADD SW 2	
J2 - 7	ADD SW 3	
J2 - 6	ADD SW 4	
J2 - 5	ADD SW 5	
J2 - 4	LSTN ONLY	

+5V

J1 - 11	1 YEAR	1 yr	S2 CALIBRATION INTERVAL
	+5V	90 dy	
J1 - 10	24 HOURS	24 hr	
J1 - 9	EXT FREQ LOCK (OG)	OFF	
	+5V	ON	S3

POWER INPUT MODULE

F1
3A FOR 230V INPUT
6·25A FOR 115 V INPUT

FRONT PANEL POWER SWITCH

LIVE	L	BROWN	J5 - 1	J6 - 1	RED		YELLOW	J6 - 3	J5 - 3	YELLOW	B
EARTH		BRAID / GREEN	J5 - 9	J6 - 9	GRN/YW						
NEUTRAL	N	BLUE	J5 - 5	J6 - 5	BLUE		GREEN	J6 - 7	J5 - 7	RED	J

CHASSIS EARTH

J6 - 2	J6 - 10	
J6 - 4	J6 - 11	
J6 - 6	J6 - 12	
J6 - 8	J5 - 10	
J5 - 2	J5 - 11	
J5 - 4	J5 - 12	
J5 - 6		
J5 - 8		NOT USED

VOLTAGE SELECTOR PCB

100V / 115/120 V / 220 V / 230/240 V

A. BLACK	J7 - 6	J8 - 6	3	RED
			2	15 V
				BROWN
				100V
C. WHITE	J7 - 5	J8 - 5		BLACK
C. WHITE				
D. VIOLET	J7 - 1	J8 - 1	5	RED/WHITE
E. ORANGE	J7 - 8	J8 - 8	1	
E				115 V
F. GREY	J7 - 3	J8 - 3	4	BLACK/WHITE

MAINS TRANSFORMER

SECONDARIES SHOWN ON POWER SUPPLY PCB'S 430451 430470

EARTH SCREEN

ORANGE

FAN

J8 - 2	
J8 - 4	
J8 - 7	
J7 - 2	
J7 - 4	
J7 - 7	NOT USED

DRAWN	DATE 30·7·81	DIMENSIONS IN MILLIMETRES	TOLERANCES: DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± 4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400439	TITLE: 4000 INTERCONNECTION PCB
CHECKED J.B.	DATE 2·4·82	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM	
APPR. B Hume	DATE 2·4·82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460439	
					CHECK LIST 470439	

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DRAWING No. 430439

SHEET 1 OF 1

E.B.W.

4951MT

DRAWING No. 400439

FIRST USED ON 4000

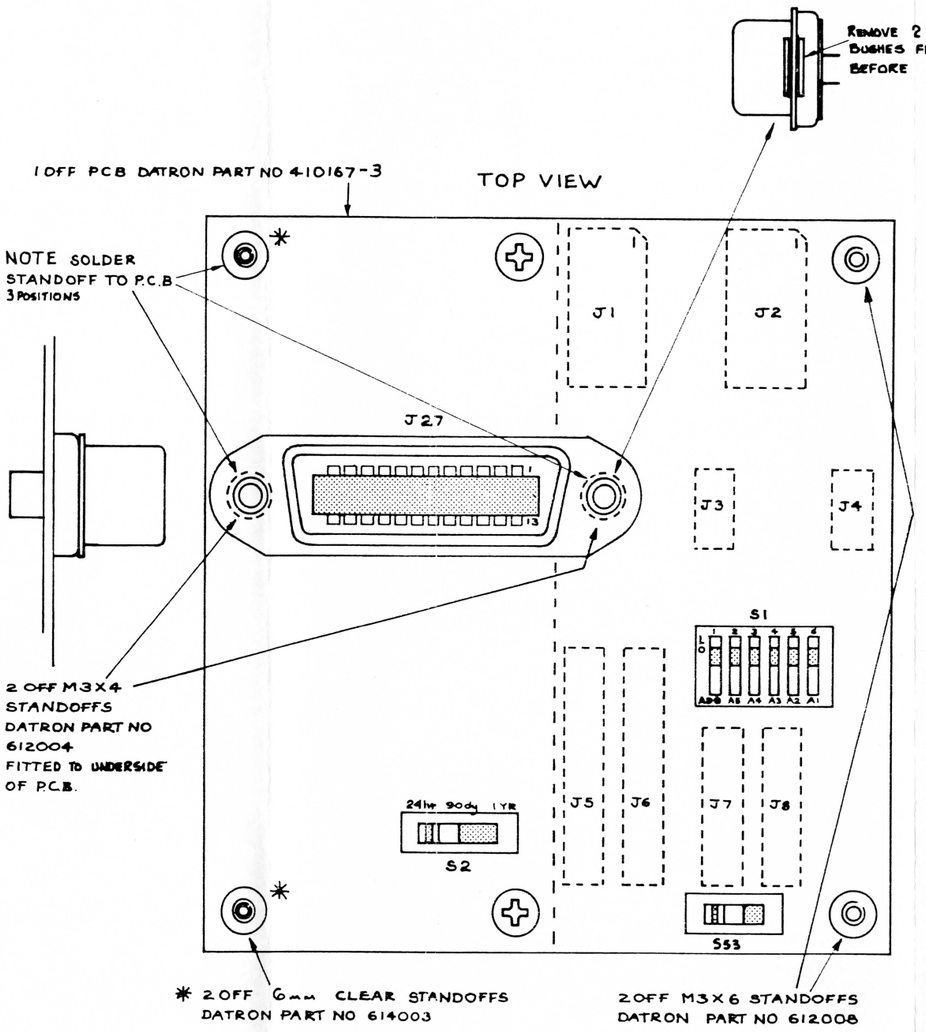
THIRD ANGLE PROJECTION

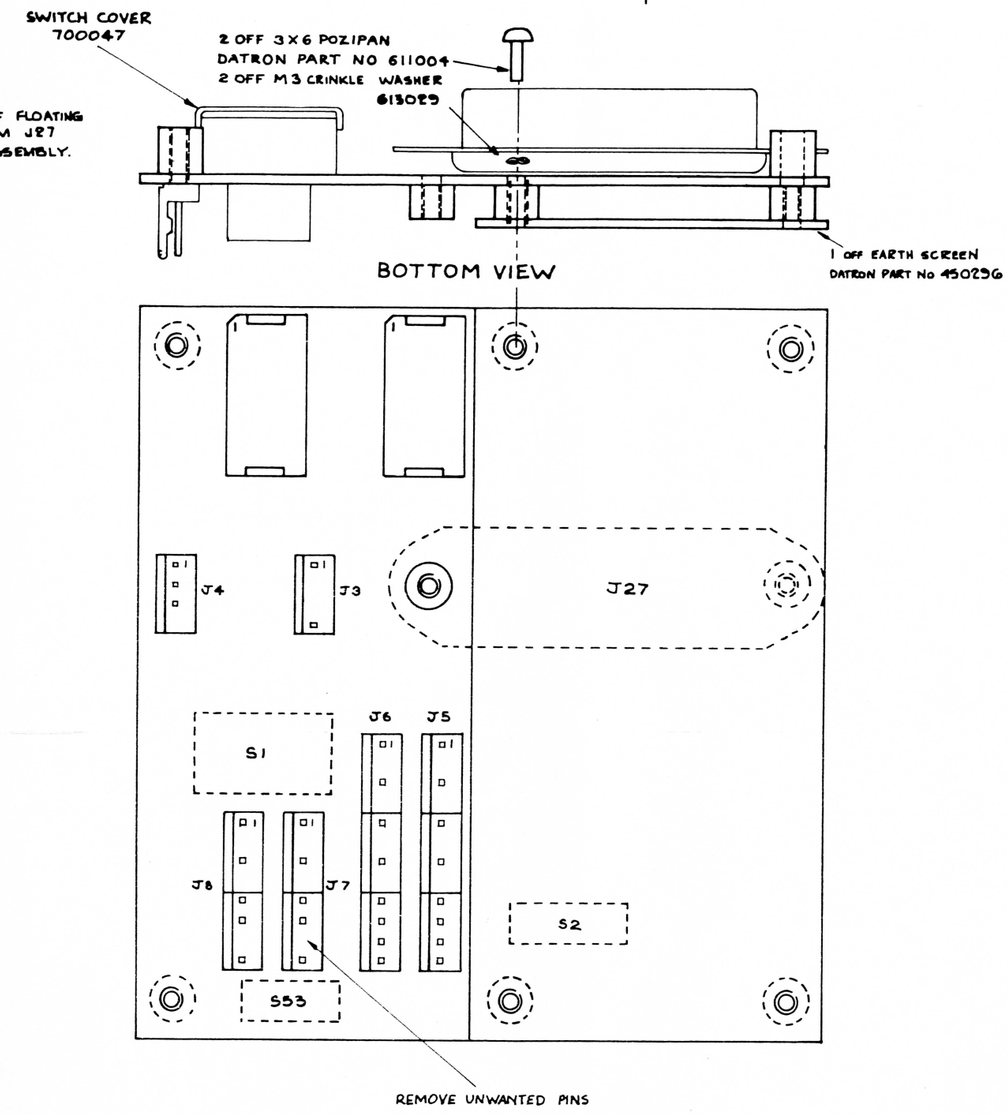
DRAWN IN ACCORDANCE WITH BS 308

ALL BURRS TO BE REMOVED

NOTES

ISS.	CHANGES
B	5-8-81.
1	29th MAR 82 RELEASED





DRAWN J.R.	DATE 24-7-81.	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± ·1mm; DECIMAL TO 1 PLACE ± ·2mm; WHOLE DIMENSIONS ± ·4mm; ANGULAR + ½°	MATERIAL —	ASSY DRG & PARTS LIST 400439	TITLE 4000 INTERCONNECTION PCB ASSY
CHECKED	DATE 29.3.82	SCALE 2:1	UNLESS OTHERWISE STATED	FINISH —	CIRCUIT DIAGRAM 430439	DRAWING No. 400439
APPR.	DATE 2.4.82	NOT TO BE SCALED	THIRD ANGLE PROJECTION		CHECK PROCEDURE 460439; CHECK LIST 470439	SHEET 1 OF 2

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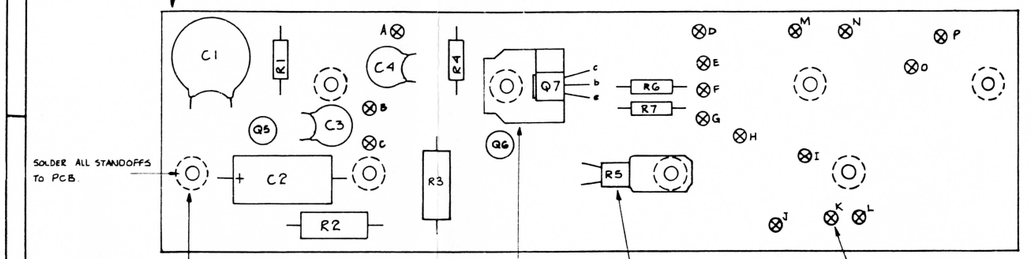
4951MT

DRAWING No. 400455

ISS.	CHANGES
C	13-8-81
1	RELEASED 19th APR 82

PROCEDURE
1) ASSEMBLE BOARD
ALIGN THE HOLES IN R5 AND Q7 HEATSINK WITH THE STANDOFFS CENTRES.

1 OFF PCB
DATRON PART NO 410166-4



SOLDER ALL STANDOFFS TO PCB.

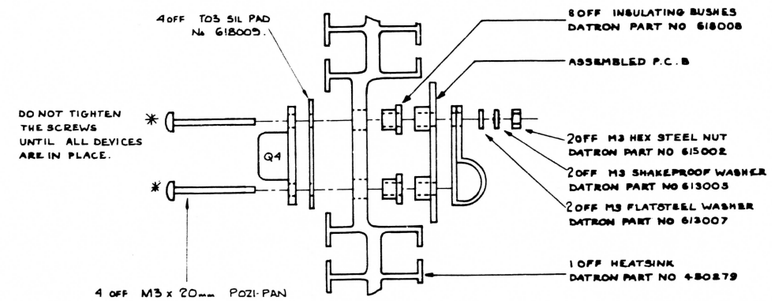
8 OFF M3 X 3 STANDOFF MOUNT ON UNDERSIDE OF P.C.B.
DATRON PART NO 612022

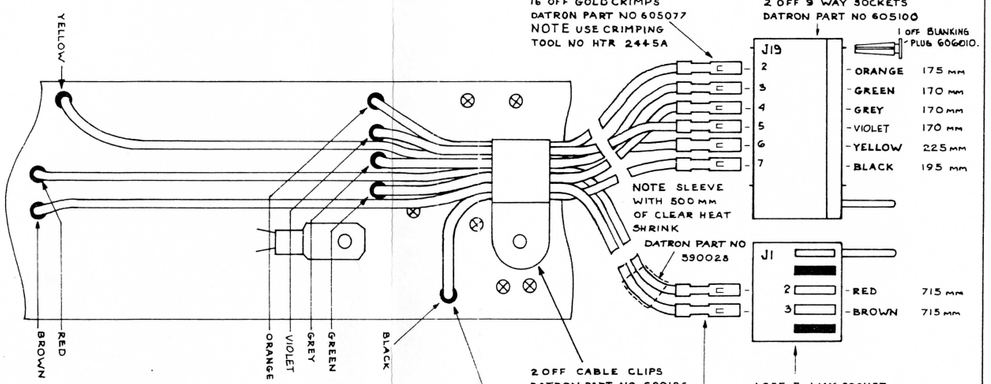
TRANSISTOR HEATSINK DATRON PART NO 920087

MOUNT WITH FLAT DOWN

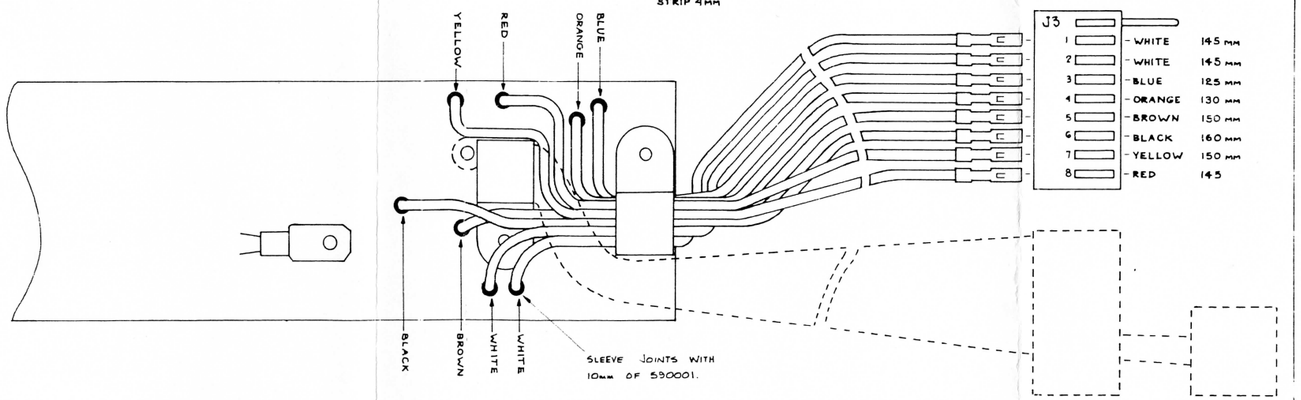
16 OFF HARWIN PINS DATRON PART NO 620003

POSITION ALL INSULATING BUSHES IN RESPECTIVE HOLES IN HEATSINK, THEN
3) PLACE PCB IN RECESS OF HEATSINK WITH CUT AWAY FLANGES. WITH BOARD FACING AS PROCEDURE 1). START AT RIGHTHAND END AND FIT Q4 TO REVERSE SIDE OF HEATSINK WITH SIL PAD AS SHOWN.
DONT SOLDER Q4 IN PLACE YET.

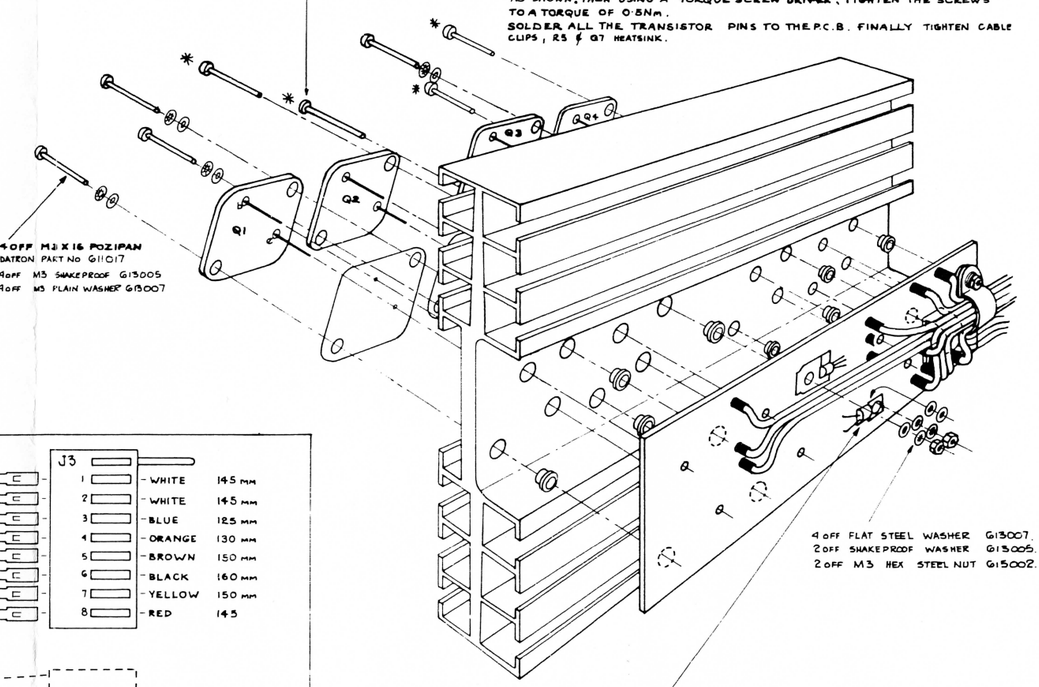




2) WIRE CABLE AS SHOWN
NOTE THE FIRST CABLE IS HELD IN POSITION BY THE SECOND.



4) WITH Q4 HOLDING THE BOARD IN POSITION, INSERT THE OTHER TRANSISTORS AS SHOWN, THEN USING A TORQUE SCREW DRIVER, TIGHTEN THE SCREWS TO A TORQUE OF 0·5Nm.
SOLDER ALL THE TRANSISTOR PINS TO THE P.C.B. FINALLY TIGHTEN CABLE CLIPS, R5 & Q7 HEATSINK.



DRAWN JK	DATE 7-7-81	DIMENSIONS IN MILLIMETRES	TOLERANCES DECIMAL TO 2 PLACES ± 1mm; DECIMAL TO 1 PLACE ± 2mm; WHOLE DIMENSIONS ± 4mm; ANGULAR ± ½°	MATERIAL	ASSY DRG & PARTS LIST 400455	TITLE 4000 POWER SUPPLY/ CURRENT HEATSINK ASSY	DRAWING No. 400455
CHECKED MJH	DATE 23.4.82.	SCALE	UNLESS OTHERWISE STATED	FINISH	CIRCUIT DIAGRAM 430445, 430448		
APPR. D Williams	DATE 29.4.82	NOT TO BE SCALED	FIRST ANGLE PROJECTION		CHECK PROCEDURE 460455		SHEET 1 OF 4
					CHECK LIST 470455		

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4.8 HIGH VOLTAGE

The circuits described in this section perform the following functions:

(1) Generate a 16kHz sine wave by band-pass filtering a 16kHz squarewave from the Reference Divider Assembly

(2) Control the amplitude of the 16kHz sine wave in a voltage-controlled amplifier, followed by power amplification to drive a step-up HV transformer.

(3) Rectify and filter the HV transformer secondary voltage to provide DC voltages to the I+ terminal:

-200V to +200V on 100V Range
-1200V to +1200V on 1000V Range

(4) Sense the voltages at the output terminals (or at the load in Remote Sense)

(5) Attenuate the sensed voltage and compare against the DC Reference Voltage in the Error Amplifier, using the error voltage as drive to the Voltage-Controlled Amplifier.

The circuits together form a negative-feedback loop which refers the output DC voltage to the value of the DC Reference Voltage, using AC drive transformation and DC sense attenuation as means of achieving the required high voltage outputs. This is illustrated in Fig. 4.33, which shows 100V Range selected, positive output in remote sense with output on.

In the main, the circuits are located on the Power Amplifier (DC) Assembly. The Error Amplifier, VCA drive circuitry, sense attenuator, overvoltage and overcurrent detectors and output switching are located on the DC PCB Assembly. Some of these circuits are common to the Low Voltage DC functions.

4.8.1 General (Fig. 4.33)

AC transformation is carried out at 16kHz, derived from M16 in the Analogue Interface 13-bit counter, and transferred into guard as a square wave through opto-coupler M3 on the Reference Divider pcb.

The square wave is filtered to provide a 16kHz sine wave. The filter has high selectivity at 16kHz to eliminate harmonic distortion.

The sine wave amplitude is controlled by the DC loop-error drive in a Voltage-Controlled Amplifier (VCA), and power-amplified to drive the step-up transformer primary. Range switching is achieved by changing the step-up ratio, both primary windings being connected in series on the 100V Range.

A constant-current source acts as a shunt to sustain the current drawn from the high-voltage secondary winding through the bridge rectifier, and polarity is switched with respect to common-2 via the LC-filtered ± 15V common-2 supplies. Positive polarity output is referred to -15V at zero output, to provide an overlap with Negative polarity output referred to +15V. The overlap allows digital calibration constants to be used to align zero voltage output in both polarities to the same calibrated zero.

The main output filter is placed in the output line. This is a low-pass filter with a high rejection at 16kHz, reducing the ripple voltage to within specification limits.

Shutdown of the high voltage power-circuitry occurs when an output current of 30 – 40mA is detected in the Current Limit circuitry. The output voltage is fed out through the Range switch on the DC pcb, where it is subject to Remote Sense and Output On/Off switching and over voltage detection, before being passed to the I+ terminal by the same route as for low voltage ranges. The external current is sunk into common-2 via the over-current detector, which warns the control processor when the output current exceeds approximately 28.5mA. On 100V and 1000V ranges the processor will switch the output off on receipt of the overcurrent signal from either the current limit circuit or the overcurrent detector.

The output voltage is sensed between the Hi and Lo terminals. Lo is referred to Sense attenuator Lo and DC Ref Lo. The Hi sense voltage is divided in the Sense Attenuators by 10 (100V Range) or 60 (1000V Range). The attenuated output is compared against DC Ref Hi in the Error Amplifier, and modifies its output to the 10V Buffer and VCA drive. The 10V Bootstrap, in addition to supplying the Error Amplifier, also buffers DC Ref Hi as reference for the VCA Drive circuit.

The error voltage between the buffered DC Ref Hi and the 10V buffer output is conditioned by the VCA drive to provide a suitable control signal for the VCA itself.

The Sense loop thus stabilises the High Voltage DC output to a value which on 100V range is 10 times the DC Ref voltage and on 1000V range is 60 times the DC Ref voltage. On 1000V range, the DC Ref voltage is scaled digitally so that Full Scale of 20V corresponds to 1200V on the OUTPUT display and at the output terminals.

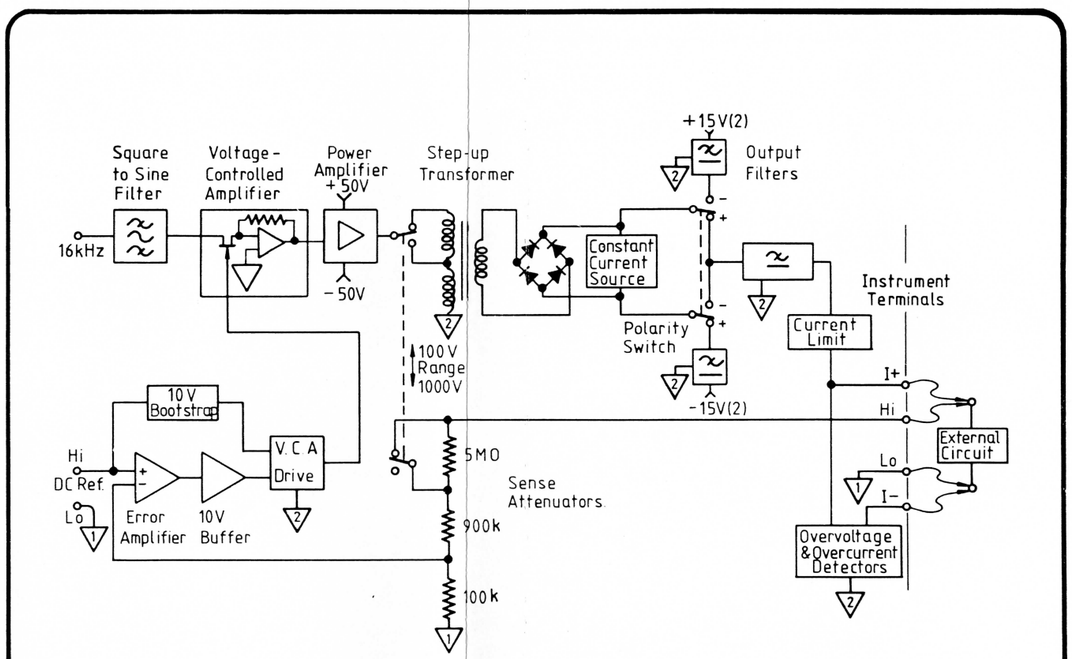

FIG. 4.33 100V AND 1000V RANGES – OUTPUT LOOPS

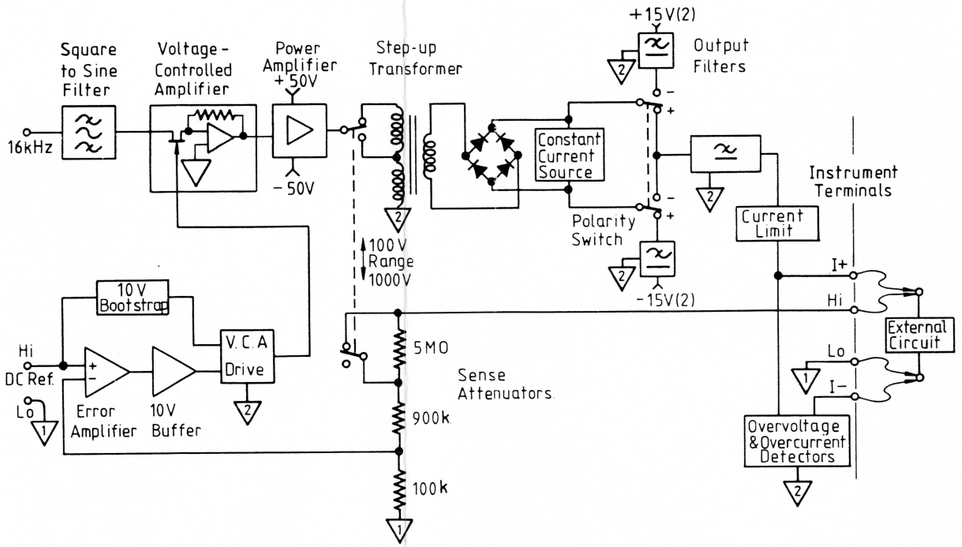

FIG. 4.33 100V AND 1000V RANGES – OUTPUT LOOPS

4.8.2 Square-Sine Filter (Circuit Diagram No. 430449 Sheet 4)

The 13-bit counter in the Analogue Interface generates 16kHz at M16-14 (Circuit Diagram 430443 Sheet 2), which is transferred into guard through opto-isolator M3 on the Reference Divider (Circuit Diagram 430444 Sheet 4). The 16kHz square wave, switching between logic-1 = 0V and logic-0 = −15V, enters the Power Amplifier pcb on J9-86.

M8 buffers apply the full 15V p-p squarewave to coupling capacitors C38 and C39. M3 input circuit is a 16kHz series-tuned filter. This, together with M3 active low-pass filter, produces a sine wave at TP15 of 0.6V to 0.8V pk-to-pk amplitude and approx 5% distortion.

4.8.3 Voltage Controlled Amplifier

The DC loop error voltage is applied from the VCA drive to Q26 to control the input resistance to M4. Q26 and R66 are matched to standardise the gain range (mid-range gain of approx 0.5). A manual gain adjustment (Q28, R68, R65) is provided for test purposes.

M4 output is AC-coupled as drive to the power amplifier.

4.8.4 Output Clamp (Circuit Diagram No. 430449 Sheet 1)

When the CPU switches the Power Amplifier on or off in 100V or 1000V ranges, it controls the 16kHz drive to the high voltage power amplifier. For both ranges, a signal PA OFF is provided at M15 pin 5 on the Reference Divider (Circuit Diagram No. 430444 Sheet 4) which is buffered by M8/Q43 on the Power Amplifier (Circuit Diagram No. 430449 Sheet 4), as PA OFF B signal.

With output off, the Output Clamp circuit is allowed to operate by D47 reverse bias. The ± 2.5V Reference from the 50V Power Supply is divided by R70/71/73/74 to provide ± 0.45V bias for M5 on 100V range. Q27 conducts only when the CPU has selected 1000V range, reducing M5 bias to ± 0.025V.

Example of clamp action

On 100V range, the bias on M5 pin 5 is −0.45V. If the PA output voltage is less negative than −5.95 volts, M5 pin 6 is more positive than pin 5 and D46 is non-conducting due to −15V at TP26. If the PA output is more negative than −5.95V, M5 pin 6 is more negative than −0.45V, TP26 rises to cause D46 conduction and Q33 starts to conduct. The 16kHz drive to the PA is reduced due to the extra volts drop across R87, which limits the negative half-cycles of the PA output at approx. −6V.

In similar fashion, D49 conducts on positive output half-cycles to start limiting at +6V and on 1000V range, positive and negative half-cycles start limiting at approx. 0.3V.

This limiting action ensures that when the 4000 output is off, the PA output to the step-up transformer is limited to less than 10V peak on 100V range, and less than 3V peak on 1000V range.

As the PA OFF B input is low (−15V) when output is on in 100V or 1000V range, Q33 is pinched off, and the PA output is not clamped.

Q34 in the PA drive line is pinched-off by $\overline{\text{I LIM}}$ at −15V when the output Current Limit is activated (see Section 4.8.9).

4.8.5 Power Amplifier (Circuit Diagram No. 430449 Sheet 1)

The Power Amplifier deals with AC and DC separately. The overall purpose is to stabilize the mean output level at zero DC, whilst driving the step-up transformer with a large enough voltage swing to provide DC output voltages at the I+ terminal of 200V (100V range) and 1200V (1kV range). The power delivered to the transformer is sufficient to provide output loading for each range of 25mA, with a little in reserve.

C46 is the only DC blocking capacitor in the whole amplifier, so Q36 and Q35 form the AC preamplifier as one half of an emitter-coupled cascode amplifier with Q38 and Q37. Q40 provides the constant current which reduces common mode disturbances at Q37 collector.

The DC path through the power amplifier passes through M6 and the Q38/Q37 half of the long-tailed pair. The DC loop is self-zeroing at input and output due to its three inversions in M6, Q38 and Q39. M6 is converted into an integrator by C48, so acts as a low-pass filter with unity gain at around 15Hz. Q32, Q39 and Q42 shift the DC level and provide high driver gain into the output Darlington amplifier. Q5 establishes the correct bias on Q24 to reduce crossover distortion, compensating four output V_{be} variations with temperature by being in thermal contact with the positive heat sink. Q41 provides constant current pull-down for the driver stage.

Q29 and Q30 current limiters prevent damage in the event of an output short circuit.

The d.c. output level is therefore referred to common-2 by R116 at M6 non-inverting input.

The AC loop also includes three inversions, so feedback controls both AC and DC to R96/(R87 + R88).

4.8.6 High Voltage Transformer and Rectifier (Circuit Diagram No. 430449 Sheet 3)

Relay RL2 is energised permanently when the watchdog BARK signal is low (−15V). The 16kHz PA output passes via RL2 pins 7 and 10 to RL1 contacts and to the High Voltage transformer.

When the watchdog BARK signal goes high (0V), the drive is removed and the transformer primary is shorted to common-2 as RL2 is de-energised.

RL1 is only energised on 1000V range with switch S1 ON (indicated by LED D37 lit on the PA (DC) Assembly. On 100V range it is set as shown on the circuit drawing, selecting both primaries in series for a step-up ratio of 9.2. For 1000V range, RL1 connects the PA output to only one primary winding (J6-1 to J6-4), a step up ratio of 49.2.

These ratios generate secondary voltage outputs sufficiently large to provide DC outputs from the instrument of 200V (100V range) and 1200V (1000V range).

The rectifier bridge uses to series diodes in each arm. Each diode is current-rated at 1A, with a p.i.v. of 1.5kV.

N.B. The transformer secondary, and bridge rectifier are not directly referred to any common. This allows the rectifier output to float so that it may be used for either polarity.

4.8.7 Constant-Current Source and Overvoltage Detector Assembly (400472)

4.8.7.1 Constant-Current Source

Q1-12 form a series Darlington chain, connected across the bridge rectifier output as a constant-current source, having two functions:

(1) It provides a discharge path which is a "constant" current at all output voltages, of approx 1.2mA above 120V, rising to 7mA at 0V.

(2) It maintains diode bridge D56-D63 conduction in no-load conditions. At higher voltages, D14-D17 limit Q11 base voltage to +2.4V, limiting the series current in R11 to 1.2mA, with Q13 pinched off. At lower voltages Q13 conducts, shunting R11 with 170-180 Ω (R10 plus Q13 'On' resistance which falls to approx 125Ω), and increasing the discharge current to approx 7mA.

Note that the minimum voltage applied across the constant-current source is 15V. Even at zero output voltage and current, the diode bridge generates 15V to back off the positive or negative 15V connected to RL3.

4.8.7.2 Overvoltage Detection

Zener diodes D1 – D13 form a series chain across the High Voltage supply. When the voltage exceeds 1440V this chain conducts, lifting D13 cathode and driving opto-isolator M9. M9 emitter rises, and provides a "Reset" logic-1 (0V) input to M10-10, resulting in a logic-0 (−15V) output from M10 – 13.

The operation of M10 and subsequent action is described in section 4.8.9.

4.8.8 Polarity Switching and Ouput Filter

Double-pole relay RL3 performs the polarity-reversal. With RL3 de-energised as shown the output filter is connected to rectifier negative, and +15V Common-2 supply is connected to rectifier positive. During zero calibration, the +15V is backed off to give a true zero output by an output from the rectifier.

When RL3 is energised by the POSITIVE signal from the serial data-link parallel output registers at logic-1 (0V), the output filter is connected to the rectifier positive rail, referred to −15V common-2 supply. Again, this −15V is backed off to zero when calibrated.

Filtering is accomplished in three stages:

(1) L8, R128, C58, C59 2-pole filter attenuates 16kHz by approx 30dB and 32kHz by approx 42dB.

(2) L9, L10 and associated capacitors form a 5-pole filter with elliptic characteristics, attenuating by at least 60dB above 16kHz.

(3) The final stage is formed by C1 on the Mother PCB (Refer to Circuit Diagram 430440 Sheet 1) and the output resistance (approx 500Ω) of the high voltage circuitry on the Power Amplifier PCB (Circuit Diagram 430449 sheet 3). This gives attenuations of approx. 30dB at 16kHz and 36dB at 32kHz.

4.8.9 High Voltage Output Current Limit Detector

Section 4.7.10 describes over-current sensing circuitry on the DC pcb Assembly, which provides LIM ST 1 signal when the output current exceeds approximately 28.5mA. It also generates HV STATUS signal when the output voltage exceeds 130V.

In addition to these signals; the two high voltage ranges are protected against over-voltage (see Section 4.8.7.2) and over-current on the Power Amplifier pcb itself.

4.8.9.1 Over-Current Detector

An output current of approx. 35mA will cause the output to be shutdown. Opto-isolator M11 is set to respond to a threshold level of approximately 5.25V across R143, causing conduction between pins 6 and 5.

4.8.9.2 Protection Logic

On Power-up, M10 settles into its stable state with Q (pin 2) and Q (pin 13) both at logic-1 (0V). Both sections have set and reset pins at logic-0 (−15V), and PA OFF B signal at logic-1. Q44 is cut off, as also are M9 and M11 output emitter-followers, holding M10 reset (pin 10) at −15V (logic-0).

By selecting Output On in 100 or 1000V range, PA OFF B goes to logic-0. M10 is not clocked by the negative edge, but Q44 is turned on, providing the supply to M11, which remains cut-off unless overcurrent is detected.

When an over-current is detected M11 Output stage conducts, lifting pin 5 from −15V to approximately −1V (logic-1 on M10 pin 10). The Q output of M10 (pin 13) is forced into reset state. $\overline{\text{HI I ST}}$ and $\overline{\text{I LIM}}$ fall to logic-0 (−15V).

The $\overline{\text{I LIM}}$ signal switches off Q34 at the input to the Power Amplifier (sheet 1), removing the 16kHz drive, and reducing the output voltage to zero, thus providing instantaneous shut-down. $\overline{\text{HI I ST}}$ signal is returned via the serial data link to the CPU, which presents "Error OL" on the MODE display and carries out the normal Output OFF routine, disconnecting the external load, reducing R143 current to zero, hence cutting off M11 Output stage. M10 pin 10 reverts to Logic-0, sensitising the flip-flop to any positive clock-edge on pin 11.

At the same time, the PA OFF B signal rises to Logic-1, cutting off Q44, and clocking the logic-1 on M10 pin 5 through to pin 1 (Q) so Q (pin 2) goes to logic-0.

Pin 4 rises on time constant C61 R135, and the monostable times out after 8mS by forcing Reset state. Pin 1 falls to logic-0 and rapidly sets pin 4 to logic-0, sensitising the monostable to any positive clock-edge on pin 3. Meanwhile, pin 2 has reverted to logic-1, clocking the logic-1 on pin 9 through to pin 13, and returning $\overline{\text{HI I ST}}$ and $\overline{\text{I LIM}}$ signals to their non-active logic-1 state. The detector remains in this state until output is again switched ON on 100V or 1000V range. The "Error OL" presentation is retained until the user makes a further Front Panel or Remote selection.

If the instrument is operating normally with Output ON in 100V or 1000V range, and Output OFF is selected, M10 monostable pin 2 again delivers its negative 8mS pulse to Pin 11 and the logic-1 at pin 9 is clocked in. But as pin 13 is already at logic-1 this does not disturb the $\overline{\text{HI I ST}}$ and $\overline{\text{I LIM}}$ signals.

4.8.10 Output Switching, Sense Attenuator and Guard (Circuit Diagram No. 340445)

The high voltage output is taken from the Power Amplifier to be Range-switched on the DC pcb (RL2 on Circuit Diagram No. 430445 Sheet 1). On 100V or 1000V the selected PHi voltage is Remote/Local and Output ON/OFF switched before passing to the instrument output I+ terminal. Any output current drawn by the external load is returned via the I− terminal and the over-current sensor to common-2 (Refer to section 4.7.10).

The external load Lo is connected directly to the Lo terminal and hence to common-1 in the DC pcb. Load Hi is returned via the Hi terminal to the head of a high-voltage attenuator (R10, R27, R48, R66, R89, R96, R99 of circuit drawing 430445 Sheet 1), which is also referred to common-1.

The attenuator is range-switched by RL3 between 1000V and 100V ranges. On 1000V range the attenuation is 60:1, reducing Full Scale load voltage of 1200V to 20V for comparison against the DC Ref Hi voltage. On 100V range; R89, R96 and R99 divide the voltage by 10. The attenuator and DC Ref Lo are both returned to common-1.

To guard the necessarily high-impedance attenuator each connection between resistors is shielded. The potential divider R8, R9, R25, R26, R46, R47, R64, R65, R88, R95 and R98 connected between the Power Amplifier output voltage and common-2 maintains each screen at the potential of the connection it is shielding, to reduce leakage. RL3 shorts part of the divider on 100V Range to equalise potentials.

4.8.10.1 Model 4000A – 100V/1000V Precision Sense Attenuator (Layout Drawing 400445 Sheet 1 and Circuit Diagram 430445 Sheet 1)

In the Model 4000A, the DC PCB is fitted with an uprated 100V/1000V attenuator, to hold the specification over a wider temperature range than the 4000:

(1) R10, R27, R46 and R48 (1M25) are replaced by five 1MO resistors.

(2) R89, R96 and R99 are replaced by one 900k/100k unit.

The whole attenuator set is referenced as part no. 090057/A.

4.8.11 VCA Drive and Control

The attenuated sense signal is applied to the inverting input of the Error Amplifier via RL11-10 and RL9-14. This bootstrapped, high-gain amplifier compares the sense signal with DC Ref Hi. When both are equal: the output from the 10V buffer at TP5 star-point, the bootstrap common BS2, DC Ref Hi and the sense signal are all at the same level. Therefore the differential input to M12 (VCA error amplifier) is zero at R42/R43.

The gain from M12-1 to I+ terminal is approx. x2000 on the 1000V Range and approx. x400 on the 100V Range. Components R97, C33 at the Error Amplifier input, and R33, C16 on M11 provide frequency compensation for the overall loop.

The second M12 stage acts as a polarity switch. With OUTPUT ON + LED lit, the POSITIVE control signal is at logic-1 (0V). Q2 conducts setting M12 non-inverting

input (pin 5) to zero volts, so the amplifier inverts the pin 6 input. If OUTPUT ON- LED is lit the POSITIVE signal is at logic-0 (-15V) cutting off Q2, M12 pin 5 follows the pin 1 voltage, so the amplifier acts as a voltage follower. The polarity switching is necessary to adapt the bi-polar action of the error amplifier to the unipolar sensitivity of the Voltage Controlled Amplifier.

4.8.11.1 VCA Action

If a user increases a positive OUTPUT display value, the positive DC REF Hi voltage will increase, (a demand to increase a positive output voltage). The polarity switch inverts the positive input from M12-1. So M12-7 feeds a negative output to M11. This is inverted and fed, via the Mother pcb, to D36 on the Power Amplifier Assembly as an error signal (Circuit Diagram No. 430449 Sheet 4).

On the Power Amplifier Assembly; as the VCA control signal becomes more positive the gain of M4 between TP15 and TP19 is increased, thus increasing the output at I+. The attenuated sense voltage rises to equallise the differential inputs to the error amplifier, and the I+ voltage stabilises at its new value.

M4 has a maximum gain of x12 when TP24 is at 0V and a minimum gain of x0.01 when TP24 is at -12V or lower.

4.8.12 Decoding Logic (Circuit Diagram 430499 Sheet 4)

4.8.12.1 "PA OFF"

The PA OFF signal is originated by the CPU and latched at M15 Q2 (pin 5) Serial/Parallel data converter on the Reference Divider pcb (Circuit Diagram No. 430444 Sheet 4); as logic-1 (0V) for PA OFF, and logic-0 (-15V) to provide the DC 100V/1kV drive from the Power Amplifier Assembly. Under normal use test link TLJ is made, but for test purposes link TLJ can be unsoldered, and TLH made. PA OFF is buffered by M8 and Q43 as PA OFF B, which has two functions:

(1) At logic-1 it allows the output clamp to operate but at logic-0 removes the clamp from the PA input. (Refer to Section 4.8.4).

(2) A 0-1 transition by PA OFFB clocks the over-voltage and over-current detector M10 to reset. (Refer to Section 4.8.9).

4.8.12.2 "POSITIVE"

The polarity of 100V and 1000V Range outputs is determined by the CPU. In addition to changing the polarity of the DC Ref Hi signal fed from the Reference Divider into the DC Error Amplifier, the POSITIVE signal performs polarity switching in the VCA drive (refer to sections 4.6.11 and 4.8.11). On the Power Amplifier pcb it energises RL3 when at logic-1 (0V), connecting the positive rectified voltage from the HV transformer to the Output Filter (Refer to Section 4.8.8). At logic-0 (-15V), RL3 is de-energised, and the drive to the output filter is negative.

The POSITIVE signal is latched at M31 Q1 (pin 4) on the Reference Divider pcb serial/parallel data converter. (Refer to Section 4.5.5).

4.8.12.3 "HV ENBL"

On 1000V Range, HV ENBL signal is at logic-1 (0V) to energise RL1, whose contacts apply the P.A. output to the single primary winding (J6-1 to J6-4) of the high voltage transformer. (Refer to Section 4.8.6). The Output Clamp circuit requires reduced reference voltages on this range, so HV ENBL is buffered as PA 1kV signal and applied to Q27 for this purpose (Refer to Section 4.8.4). Switch S1 on the PA pcb can be set to disable the 1kV Range output by releasing RL1 and shorting the 16kHz drive to the PA. When the switch is in the "Enable" position, LED D37 lights as a visible warning.

4.8.12.4 "DC ST"

The DC ST line returns to the Reference Divider pcb, (Circuit Diagram No. 430444 Sheet 4), and is connected there to M21 pin 5. An identical line from the DC pcb also connects to M21 pin 5. Each line is pulled down to -15V through a 15kΩ resistor. When both lines are correctly connected, M21 pin 7 (TP17) is at logic-0 (-15V), input to M22-13 Parallel/Serial data converter. The DC status bit is read out of the SSDA "Receive" register by the CPU on each data transfer. If at logic-0, DC function may be selected by a user. If at logic-1, the CPU inhibits selection. The same method is used for AC ST, but as AC is not fitted in the 4000, M22-4 will always be at logic-1.

4.8.12.5 "BARK"

The Safety Monitor (Watchdog) produces the BARK signal when the CPU or SSDA is functioning incorrectly, and the SAFETY message is presented on the MODE display. The BARK signal is normally at logic-0 (-15V) so that RL2 is energised, applying the PA output to the HV transformer. When a failure trips the watchdog, BARK goes to logic-1, de-energising RL2, which disconnects the PA output and shorts the HV primary to common-2, reducing the 4000 output voltage to zero. (Refer to Section 4.5.6 for information on the Safety Monitor).

4.8.13 50V Power Supply (Circuit Drawing No. 430449 Sheet 2)

The power supply on the PA pcb provides ± 50 volts regulated power for the Power Amplifier. It incorporates "Foldback" current limiting and "excess input voltage" limiting for both polarities. Overheating of the positive or negative heatsink (PA Output stages) generates a $\overline{\text{TEMP ST}}$ signal to the CPU via the serial data link. Overheating of the PS/I heatsink, failure of the ± 15V supply or ± 50V output undervoltage; generates a $\overline{\text{PS ST}}$ signal to the CPU.

In both cases the CPU sets 4000 Output Off and displays a FAIL message:

FAIL 1 – $\overline{\text{TEMP ST}}$ at Logic-0
FAIL 7 – $\overline{\text{PS ST}}$ at Logic-0

When the power supply is operating normally, both signals are at logic-1. The logic levels for these signals at TP3 and TP22 are Logic-0 = −15V, Logic-1 = 0V (common-2).

4.8.13.1 50V Supply Regulation

Power is input from the Line Transformer secondaries, both fused at 4A. R1 provides an adjustment to eliminate line frequency hum on the guard shields, in conjunction with R52/C4 on the Mother pcb. (For adjustment procedure refer to Section 5.7).

The secondaries are referred to common-2, and the rectified outputs are smoothed by reservoir capacitors C2 and C3 at the rear of the Mother pcb.

The series regulation elements Q3 and Q4 are mounted on the PS/I heatsink assembly. These Darlingtons are driven by Q10 and Q9.

NB. The following description refers only to the positive 50 Volt supply. The action in the negative supply is similar.

Q17 generates constant current of 3mA to activate D15 2.45V Zener diode. The +2.45V provides the positive reference supply for the Output Clamp circuit (Refer to Section 4.8.4.). It is also the reference for comparator M2-2. The output voltage is sensed on the +50V rail and divided down to Reference potential at M2-3. M2-1 output drives Q6 whose collector voltage at TP18 controls Q3 (PS/I Heatsink) conduction via Q10. If the +50V rail voltage falls due to loading, TP18 voltage rises, increasing the conduction of Q3 to restore the output rail voltage.

4.8.13.2 50V Current Limit (Positive 50V only described)

R24 is the series current detector, which drops 0.4V at 2.7A. Q19 generates a constant current of approximately 3mA which can be shared between Q12 and Q11. Q12 is saturated, generating approximately 200mV across R39. With little or no load current passing through R24, Q11 is off. When the current through R24 reaches approximately 2.7A, Q11 is switched on.

Q11 collector voltage rapidly falls below Q10 base voltage, D25 conducts and pulls Q10 base voltage down, reducing Q3 conduction. This reduces the current through R24, but with Q11 fully conducting, it is held on by the voltage across R39. As a result, Q3 conduction can fall to approximately 500mA, and with the overload still present, the 50V rail voltage can fall to approximately 12.5V. This is a stable condition which persists until the 4000 is powered-down. As the voltage falls below +43V the under-voltage detector is activated (Refer to Section 4.8.13.3).

4.8.13.3 Under-Voltage Detection

With the Power Supply operating normally, the positive rail voltage lies between +49.5V and +52.2V. M1-3 is held at approximately +2.85V, and as the +2.45V Reference is connected to M1-2, D11 is reverse-biassed by +15V at M1-1. (D11 anode is normally pulled to 0V by AN2 on the Reference Divider pcb – Refer to Circuit Drawing No. 430444 Sheet 4).

When the rail voltage falls below approximately +43V, M1-3 falls below +2.45V, and M1-1 changes polarity to −15V, forward-biassing D11, and setting $\overline{\text{PS ST}}$ to logic-0. This is detected by the CPU, which presents FAIL 7 on the MODE display and sets 4000 Output OFF.

4.8.13.4 50V Power Supply Shutdown

At normal operating temperatures, the PS/I heatsink thermal detector has high resistance (approximately 100kΩ). Q3 base is biassed by approximately +1V from the junction of R13/R9, so Q3 is saturated, holding approximately 150mV across R7 – R6, cutting Q1 off. The same 150mV holds p-channel FET Q4 On, which in turns holds Q2 cut off. D5 is unbiassed so $\overline{\text{PS ST}}$ is at logic-1 (0V).

If either the +15V or −15V supply fails, the voltage at Q3 base falls and cuts Q3 off. The clamp on Q1 base is removed, and it draws collector-current through R26, turning off the conduction in Q3 (PS/I heatsink). In the negative supply, Q4 is cut off, and Q2 turns off Q4 (PS/I heatsink) conduction. D5 is forward-biassed by −15V from the unregulated supply, clamped by D4, setting $\overline{\text{PS ST}}$ to logic-0 (−15V).

If the PS/I heatsink overheats, the temperature is detected by R3 (NTC thermistor). R3 resistance falls from 100kΩ to 100Ω (approximately) as its temperature rises from 80°C to 90°C, reducing Q3 V_{be} to approximately 200mV. Q3 cut-off initiates the power supply shutdown as for loss of ±15V supply.

4.8.13.5 PA Overheating

The Positive and Negative Heat Sink assemblies house the Power Amplifier output transistors. Each assembly is sensed by a NTC thermistor. These are connected in parallel, in series with R35 across the −15V supply. If either heatsink overheats, the $\overline{\text{TEMP ST}}$ signal changes from logic-1 to logic-0, the CPU presents FAIL 1 on the MODE display, and turns the 4000 Output OFF.