Keysight Technologies
15431A Filter Set for 81150A

Generates Random Jitter Profile for Testing
PCI Express® 2.0 Receivers

Data Sheet

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PCI Express® 2.0 Physical Layer Testing

Increasing speed rate for PCI Express Generation 2 is driving design to new dimensions. Validating and testing of PCI Express devices at the physical layer is getting more and more challenging for today's engineers.

PCIe ® 2.0 doubles the data rate from 2.5 Gbit/s to 5 GBit/s, improves point-to-point data transfer protocol and becomes more tolerant of jitter. Therefore the jitter tolerance and transfer measurement become more important.

Keysight's Offering

Keysight Technologies, Inc. offers serial and multi-lane RX testing.

J-BERT N4903A High-Performance Serial BERT

allows single-lane characterization of jitter tolerance from the device's input, checks compliance by emulating jitter conditions and has built-in mask tests and eye analysis tools to evaluate the PCIe 2.0 design.

ParBERT 81250A High-Performance Parallel Bit Error Ratio Tester

is a modular BERT platform for clock, data generation and data analysis that allows configuring of a solution with up to 64 output and input channels. Its jitter modulation capability via the delay control input, together with the PCIe multi-lane receiver compliance test suite make it an automated and highly accurate tool for multi-lane PCI Express receiver tolerance compliance and characterization testing.

The PCIe 2.0 specification defines a dedicated random jitter profile. The required control voltage for ParBERT's delay control input can be generated by the Keysight 81150A, a pulse function arbitrary noise generator.

The 81150A Pulse Function Arbitrary Noise Generator

provides white Gaussian noise with a selectable crest factor up to 7 (V_{peak} / V_{RMS}) or 14 ($V_{peak\,peak}$ / V_{RMS}). The long repetition rate of 26 days ensures real random noise. After 26 days the noise pattern starts from the beginning.

The Keysight 15431A noise filter is an instrument accessory that is intended to be used for jitter measurements on PCIe 2.0 with the 81150A as noise source and the N4903A or the 81250A as jitter tolerance tester.

The proper jitter spectrum is achieved by filtering the white noise with a PCIe 2.0-specific filter. The filter can serve two topologies: data driven and common clock.

Table 1. Two different clocking architectures

Two different clocking architectures	
Common reference clock	**Data clocked (embedded clock)**

– RX sampling on (multiplied) ref clk
– RX w /DLL only (no CDR/PLL)
– SSC off: no phase error induced
– SSC on:
  – Small error (femtoseconds) due to path delay difference (!) but
  – Significant residual phase error due to potentially different transfer functions (BW and peaking) of TX and RX clock multiplying PLLs (CMU)
	– Receiver with PLL-CDR (using ref clock only until locked)
	– SSC on or off:
	  – Common for TX and RX, both TX's use same ref clk

Test Setup of a J-BERT

Test setup of a J-BERT with the 81150A for LF noise; the filtered signal from the 81150A is used as delay control input for the J-BERT.

An equivalent setup is valid for the ParBERT 81250A.

The N5990A test automation software supports PCIe 2.0 compliance testing and characterization with J-BERT and ParBERT configurations.
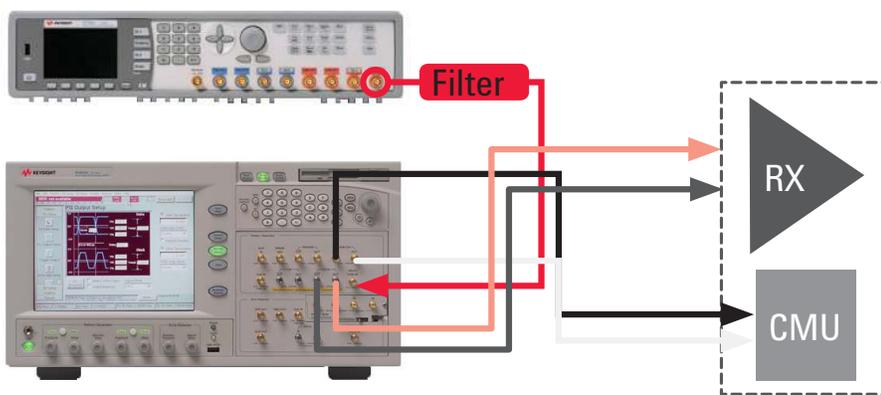
Figure 1. Test setup of a J-BERT with the 81150A for LF noise; the filtered signal from the 81150A is used as delay control input for the J-BERT. ISI and channel effects are merged into the signal path of the J-BERT by using the built-in trace 2.

The PCIe 2.0 Jitter Specification for Receiver Tests

Table 2. The PCIe 2.0 jitter specification for receiver tests

Specifications and characteristics	Common reference clock architecture	Data clocked architecture
Impedance	50 Ω	
Low frequency pass band	0.01 – 1.5 MHz	
High frequency pass band	1.5 – 100 MHz	
$\|\|LF\|\|_2$ / $\|\|HF\|\|_2$ [1,2]	4.2 / 3.8 ± 10%	8.0 / 4.2 ± 10%
Total insertion loss [2,3]	21.4 ± 1 dB	21.9 ± 1 dB
Max. input voltage	10 V_{pp}	
Input connector	BNC (female)	
Output connector	SMA (female)	
Operating temperature range	0 – 55 °C	
Mech. dimensions (L x W x H)	109 x 20 x 20 mm	
Weight	71 g	

1. Lp norm $\|\|X\|\|p$ yields rms value of X for p = 2

2. at +25 °C ± 5 °C ambient temperature

3. With 81150A as Gaussian noise source, crest factor = 7
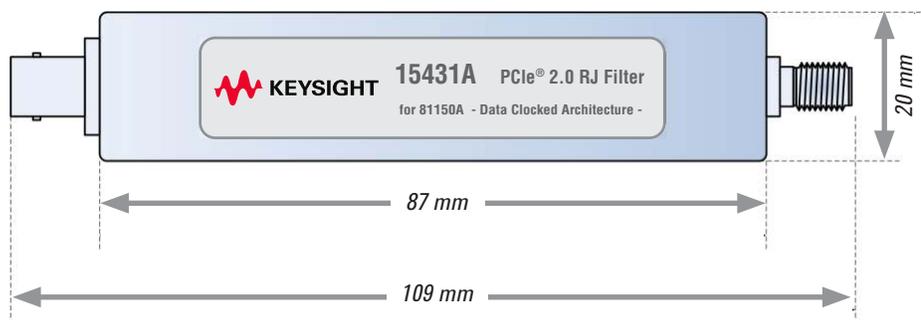

Figure 2. 15431A dimensions

Setting the correct output amplitude on the 81150A

For the reference clock filter the total rms jitter is $(4.2^2 + 3.4^2)^{1/2} = 5.4$ ps. The sensitivity of the J-BERT delay control input is specified with 400ps/V. Thus the filter's output voltage must be $5.4/400 = 0.0135$ V_{RMS} or 13.5 mV_{RMS}. With an insertion loss of 21.4 dB for the filter, the appropriate 81150A output voltage is 159 mVrms. The equivalent calculation for the data clocked filter with a total RMS jitter of 9 ps and 21.9 dB insertion loss yields 280 mV_{RMS}:

Jitter is separated into two bins:

LF: 0.01 - 1.5M Hz step BPF
LF-RJ$_{RMS}$ = 4.2 ps

HF: 1.5 MHz step HPF and 100 MHz edge filtering
HF-RJ$_{RMS}$ = 3.4 ps

15431 RCA-filter specification:
$|LF\text{-}RJ/HF\text{-}RJ|_{RMS}$ = 1.23 ± 10%
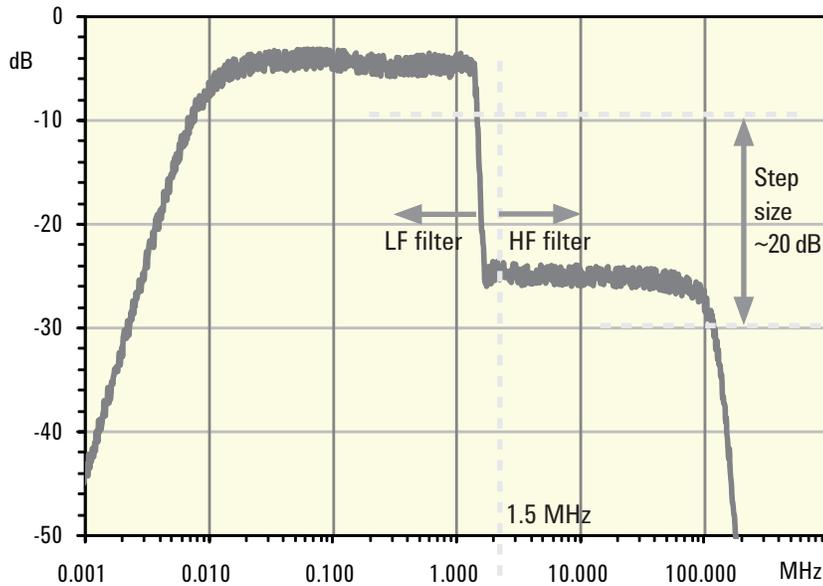Total insertion loss: 21.4 ±1 dB

Figure 3. RJ filter noise spectrum for common reference clock architecture with 81150A as noise source

Jitter is separated into two bins:

LF: 0.01 - 1.5 MHz step BPF
LF-RJ$_{RMS}$ = 8.0 ps

HF: 1.5 MHz step HPF and 100 MHz edge filtering
HF-RJ$_{RMS}$ = 4.2 ps

15431 DCA-filter specification:
$|LF\text{-}RJ/HF\text{-}RJ|_{RMS}$ = 1.9 ± 10%
Total insertion loss: 21.9 ±1 dB
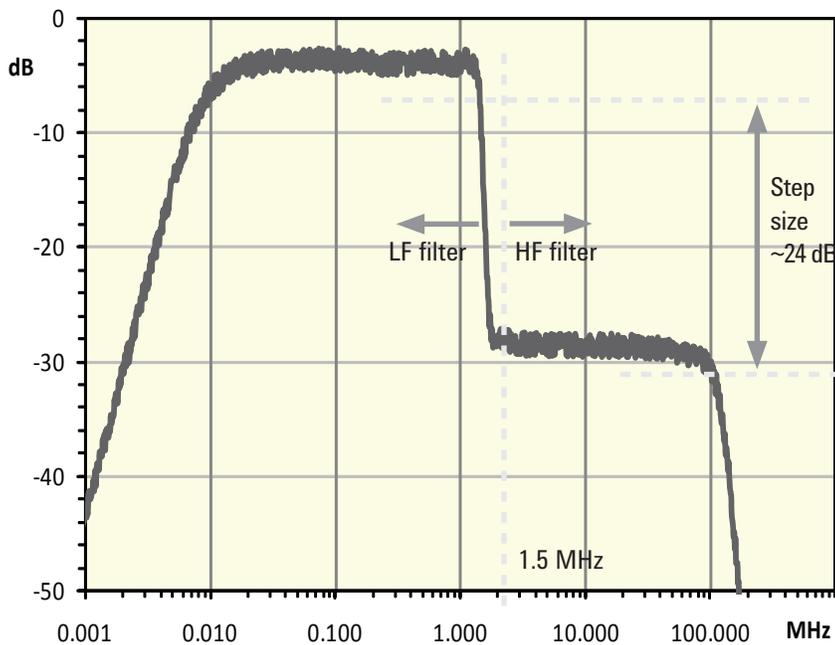
Figure 4. RJ-filter noise spectrum for data clocked architecture with 81150A

Related Keysight Literature

Table 3. Related literature

Publication title	Pub number
Keysight 81150A Pulse Function Arbitrary Noise Generator Data Sheet	5989-6433EN
Keysight J-BERT N4903A High-Performance Serial BERT	5989-2899EN
Test Automation Software Platform N5990A	5989-5483EN
Keysight ParBERT 81250, Parallel Bit Error Ratio Tester	5968-9188E

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