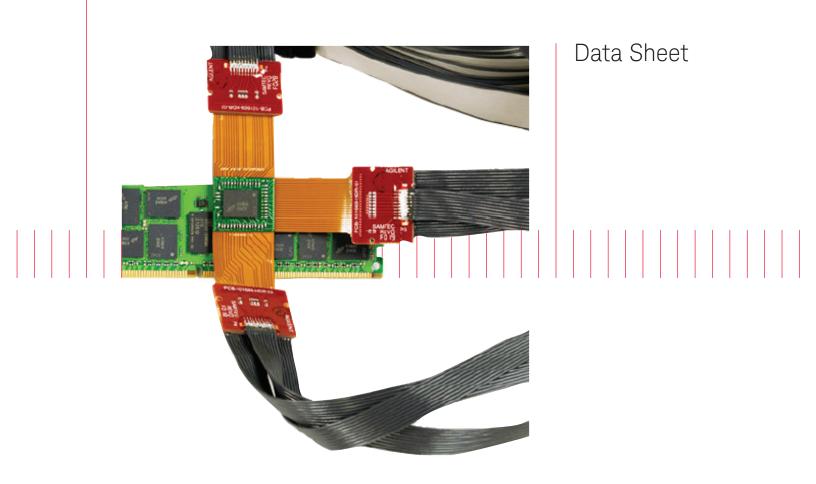
Keysight W4630A Series DDR4 BGA Interposers for Logic Analyzers





The W4630A series DDR4 BGA interposers enable probing of embedded memory DRAM directly at the ball grid array with Keysight Technologies, Inc. logic analyzers.

The Keysight W4630A series DDR4 BGA interposers for logic analyzers enable viewing of data traffic on industry standard DDR4 DRAMs with the Keysight U4154A logic analysis systems.

Features	Benefits	
Connects directly to the DDR4 BGA balls.	Eliminates reflections from mid-bus probing methods. Also eliminates design time, prototype builds, and trace routing required to design in alternative probing methods.	
Supports:	Get complete signal access to the DDR4 signals critical to your	
- Single die x4, x8 configuration	debug and validation effort.	
- Stacked/quad-die x4, x8 configuration	_	
- Operating transfer rate of 2400 Mb/s (validated)	Operate at full speed making measurements with a	
 Designed to achieve higher data rates once DDR4 DRAM technology achieves higher data rates (to be validated) 	Keysight U4154B or U4154A logic analyzer.	
 Using U4154A with APS (Advanced Probe Settings*) enables highest data rates 	-	
Supports either leaded or lead-free solder.	Easily works with all solder finishes. Designed to tolerate lead-free soldering temperature profiles.	
Contract manufactures available for those without the in-house expertise or facilities for soldering BGAs.	Eliminates the need to develop BGA soldering expertise.	
Flexible "wings" with ZIF connectors.	Ensures reliable connection to the ZIF probes. Enables placement of the probe cables around adjacent components. Minimizes the torque to the balls of the BGA.	
Attach to E5849A single-ended ZIF probes for connection to the logic analyzer.	Optimizes the use of logic analyzer channels by allowing assignment of channels to 4, 8 or 16 bits on each DRAM.	

The DDR4 BGA Interposer Advantage

* To enable Advanced Probe Settings refer to Tech brief # 5991-0799EN. Maximum transfer rates are subject to variables in the signal integrity of the system under test.

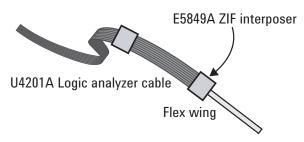
DDR4 BGA Interposer Connection to a Keysight Logic Analyzer

The W4633A DDR4 BGA interposer connects to two E5849A cables to provide connection to the logic analyzer for the x4/x8 probe system.



Figure 1. E5849A 46-ch single-ended ZIF probe for x4/x8 DRAM BGA interposer connects to 90-pin logic analyzer cables





W4630A Series BGA

Figure 2. Interposer and cable connection to the logic analyzer

DDR EyeFinder and EyeScan Software

The DDR EyeFinder and EyeScan software tool helps you position the sampling points for accurate read and write data capture. The software qualifies scans of valid read and write commands while your system executes memory tests, random read and write traffic, or stimulus program. The software will then display read and write data valid window as a result of the scan.

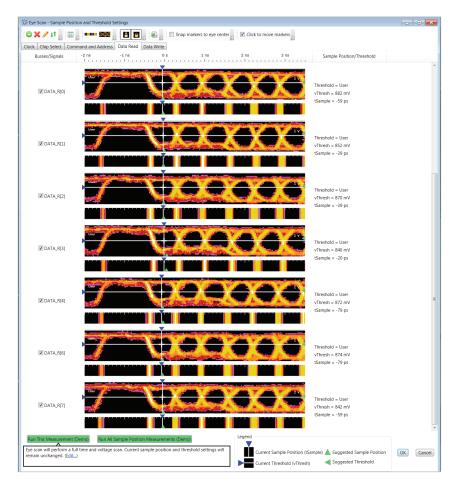


Figure 3. DDR EyeFinder and Eyescan software shows read and write data valid windows for accurate sampling position of data for protocol decode

Protocol Analysis

The W4630A series BGA interposer along with the B4621B memory bus decoder provides protocol decode of memory transactions using a Keysight logic analyzer as the analysis execution engine. Data is decoded and displayed at any level of detail from the protocol to binary. The B4621B protocol-decode software translates acquired signals into easily understood bus transactions, at the full bus speed. The Keysight logic analyzer provides extensive triggering and store qualification features. The DDR protocol-decode software executes in the logic analyzer and takes user input on system attributes such as Burst length, CAS and Additive Latency, as well as Chip Selects to decode the key DDR bus signals and present a display that lists the transaction type, address, data and command conditions. The software also supports user-defined symbols that can be easily added to the state listing display. The W4630 Series BGA interposer along with the B4622B compliance toolset provides memory bus triggering, debug and compliance verification measurements.

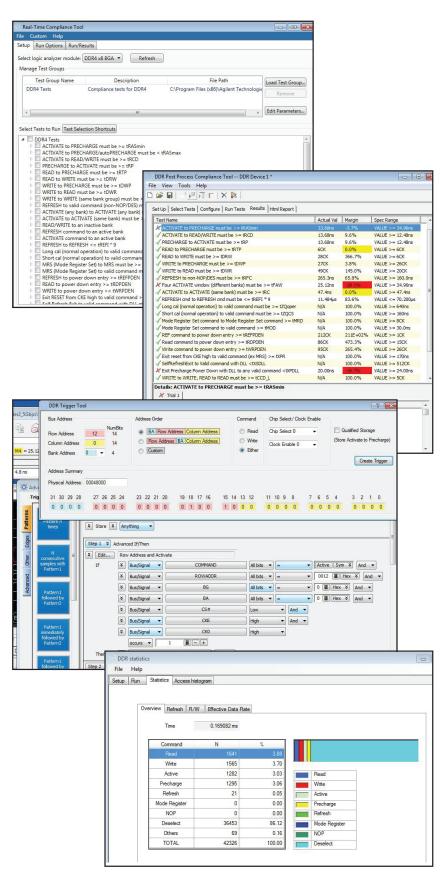


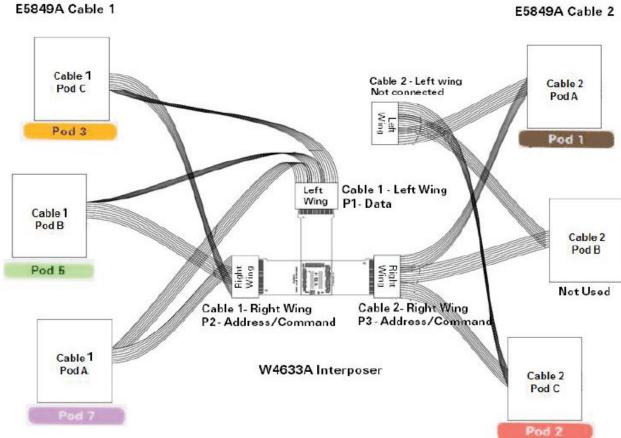
Figure 4. The B4622B compliance toolset used with the W4633A DDR4 interposer

Interposer Pin-Out to Logic Analyzer

The following signals are omitted from the Logic Analyzer connection for the x4/x8 interposer system:

Address signal group None Control and other signals group VREFCA, TEN, ZQ Data signal group None

For additional installation information, refer to the installation guide at http://literature.cdn.keysight.com/litweb/pdf/W4631-97000.pdf



E5849A Cable 2

Technical Specification

Keysight Technologies Rigid/Flex BGA interposers enable probing of embedded DDR4 DRAM (x4 and x8) directly at the ball grid array using Keysight logic analyzers.

Key performance features

- Probes a 78 ball DDR4 single channel x4 or x8 DRAM chip, JEDEC MO-207M footprint variation DT-z, with a maximum DRAM package size of 11 x14 mm*
- Access signals with two E5849A cables (sold separately)
- Measurement timing skews within ±25 psec achieved by matched trace lengths from DDR4 balls to test point
- Interposers are delivered with RC (resistor/capacitor) networks for logic analyzer probing installed on top of each DDR4 BGA interposer
- W4633A ships with a riser that is required to provide clearance for the bottom RC and surrounding devices
- DDR4 78-ball riser may be replaced with an optional grypper socket, sold separately (http://www. hsiotech.com/products/releasedproducts/engineering-products/ grypper-family)
- * Maximum of 11 mm x 14 mm DDR4 DRAM package can fit on top of DDR4 x4/x8 BGA interposer without an additional riser, optional grypper, or socket (not provided) to provide clearance for the RC components.

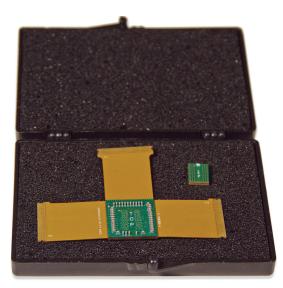
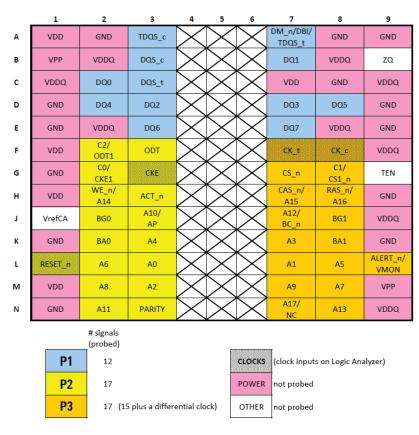


Figure 5.W4633A DDR4 x4/x8 BGA interposer with riser

Ball count:	78
Package size:	Maximum 11 mm x 14 mm*
Connectors:	3 zero-insertion force (ZIF) connectors

Signals to be probed

The BGA interposer provides access to the DDR4 signals highlighted below and passes all power and ground signals between the system and memory chip.



DDR4

Figure 6. Signals probed; Top View

Riser, interposer, and RAM stack up

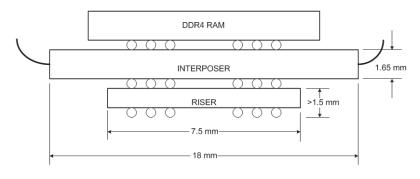


Figure 7. Dimensional diagram of Interposer/RAM stack-up. Can use riser or optional grypper socket (not included).

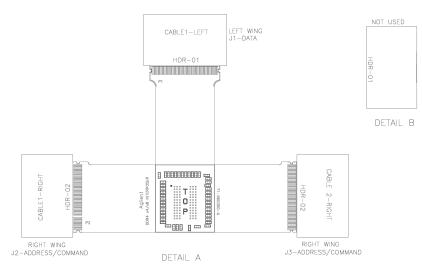


Figure 8. Dimensional top view of W4633A.

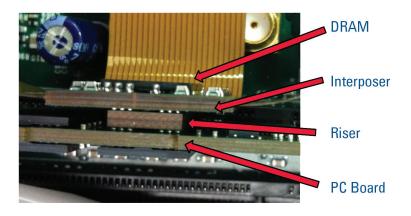


Figure 9. Example of stack-up using a riser and interposer. Riser provides clearance for bottom-side RC components on interposer and allows BGA interposer to clear surrounding DRAM.

Logic Analyzer Configuration Guide and Ordering Information

DRAM type	Data width	Access to	Probes	Cables	Logic analyzer modules	Order summary
x4	x4	Command, Address,	W4633A	E5849A (2)	U4154A	U4154B 1 U4201A 4
x8	x8	Control and Data	VV4033A	U4201A (4)	04104A	E5849A 2 W4631A 1

U4154A requires M9502A or M9505A AXIe chassis.

Product	Description
DDR3 BGA probes	
W4633A	DDR4 x4/x8 BGA command and data probe for logic analyzer
AXIe modular logic analyzers	
U4154B	136-channel, 4Gb/s state, 5 GHz timing, memory depth up to 200 M, AXIe-based logic analyzer module allowing three modules to merge into one time base
U4201A (4)	Logic analyzer probe cable
Logic analyzer ZIF probes ¹	
E5849A (2)	46-ch single-ended ZIF probe for x4/x8 DRAM BGA interposer connect to 90-pin logic analyzer cable
Software	
Logic and protocol analyzer software	Required - not licensed; acts as the base software platform
B4621B	DDR2/3/4 bus decoder (recommended)
B4622B	DDR2/3/4 and LPDDR/2/3 protocol compliance and analysis tool (recommended)
DDR Setup Assistant and DDR Eyefinder ²	Highly recommended

- 1. Used to connect W4630As Series DDR4 BGA interposers to 90 pin logic analyzer cables.
- 2. DDR Setup Assistant and Eyefinder software is available free of charge. DDR Setup Assistant provides a series of steps to simplify state mode measurement tuning with U4154A logic analyzer modules.

You can install the software components by downloading the required files from www.keysight.com/find/lasw-download

Related Literature

Publication title	Pub number
U4154B Logic analyzer module data sheet xxxx-xxxxEN	5990-7513EN
Keysight W4630A Series DDR4 DRAM BGA Interposer User's Guide Manual	
B4622B DDR2/3/4 and LPDDR/2/3 Protocol Compliance and Analysis Toolset - Data Sheet	5991-1063EN
A Time-Saving Method for Analyzing Signal Integrity in DDR Memory Buses - Application Note	5989-6664EN
Infiniium 90000-X Series Oscilloscopes - Data Sheet	5990-5271EN
B4621B for DDR2, DDR3, or DDR4 Debug and Validation - Data Sheet	5991-0802EN
Advanced Probe Settings Mode - Technical Brief	5991-0799EN

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