



DDR Memory Overview, Development Cycle, and Challenges

Tutorial

DDR Overview

Memory is everywhere – not just in servers, workstations and desktops, but also embedded in consumer electronics, automobiles and other system designs. With each generation of DDR SDRAM, short for Double Data Rate Synchronous Dynamic Random Access Memory, speeds increase, packages sizes decrease, and power consumption decreases (see Table 1). With these improvements comes the added challenge of decreased design margins, signal integrity, and interoperability.



DDR Interface

The Joint Electronic Devices Engineering Council (JEDEC) has also introduced a new DDR standard for low-power DDR (LPDDR) or mobile devices (mobile-DDR). As the name implies, this standard uses lower signal amplitude, improving power consumption. Currently the standard meets the specifications for DDR1. Engineers will not need to re-design the link or protocol layer of devices to take advantage of the lower power consumption, since little investment is required to adjust the voltage level in the system.

DDR standard	DDR	LPDDR or Mobile-DDR	DDR2	LPDDR2 or Mobile-DDR2	DDR3	LPDDR3 or Mobile-DDR3	DDR4
Specification	JESD79E	JESD209	JESD79-2E, JESD208	JESD209-2B	JESD79-3C	JESD209-3	JESD79-4
Operating voltage	1.5 - 3.3V	1.8V	1.8V	1.6B	1.5V	1.2V	1.2V
Clock frequency	100 - 200 MHz	100 - 200 MHz	200 - 400 MHz	100 - 533 MHz	400 - 800 MHz	667 - 800 MHz	800 - 1600 MHz
Data transfer rate	200 - 400 MT/s	200 - 400 MT/s	400 - 800 MT/s	200 - 1066 MT/s	800 - 1600 MT/s	1333 - 1600 MT/s	1600 - 3200 MT/s
Package type	This Small Outline Package (TSOP)	Fin Ball-Grid Array (FBGA)	Fin Ball-Grid Array (FBGA)	Fin Ball-Grid Array (FBGA)/POP	Fine Ball-Grid Array (FBGA)	POP	Fine Ball-Grid Array (FBGA)
Package size	x4, x8, x16, x32	x16, x32	x4, x8, x16	x16, x32	x4, x8, x16	x16, x32	x4, x8, x16
Backward compatibility	No	Yes, with DDR	No	Yes, with DDR2	No	No	No

Table 1. JEDEC defines the DDR specifications; however, JEDEC leaves the responsibility to designers or adopters to abide by the standards rather than enforcing compliance.

The DDR interface consists of signals for control, address, clock, strobe and data. As Figure 1 shows, clock, address and control signals are transmitted one way from the memory controller to the DDR chip; strobe and data signals are bi-directional. In a read operation, the strobe and data signals are transmitted from the DDR chip to the memory controller. In a write operation, the signals move in the opposite direction.

To improve signal performance as data transfer rates increase and signal amplitude decreases, the clock and strobe signals are differential, which cancels out common mode noise. The other signals still operate in single-ended mode, which makes them more susceptible to noise, crosstalk and interference.

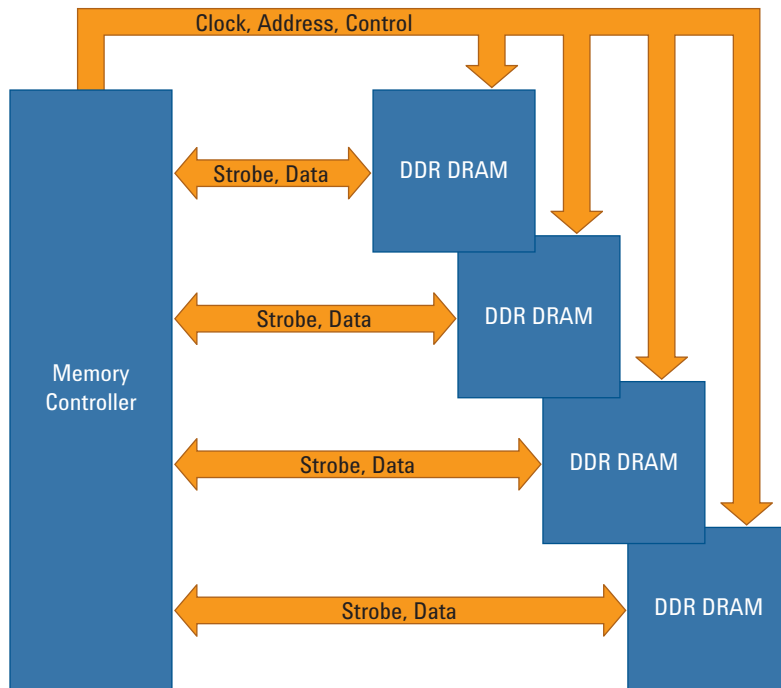


Figure 1. In the DDR Interface, clock, address and control signals move from the memory controller to the DDR chip, but strobe and data signals are bi-directional. Their direction depends on the operation being performed.

Common DDR Validation Challenges

DDR Memory Development Cycle

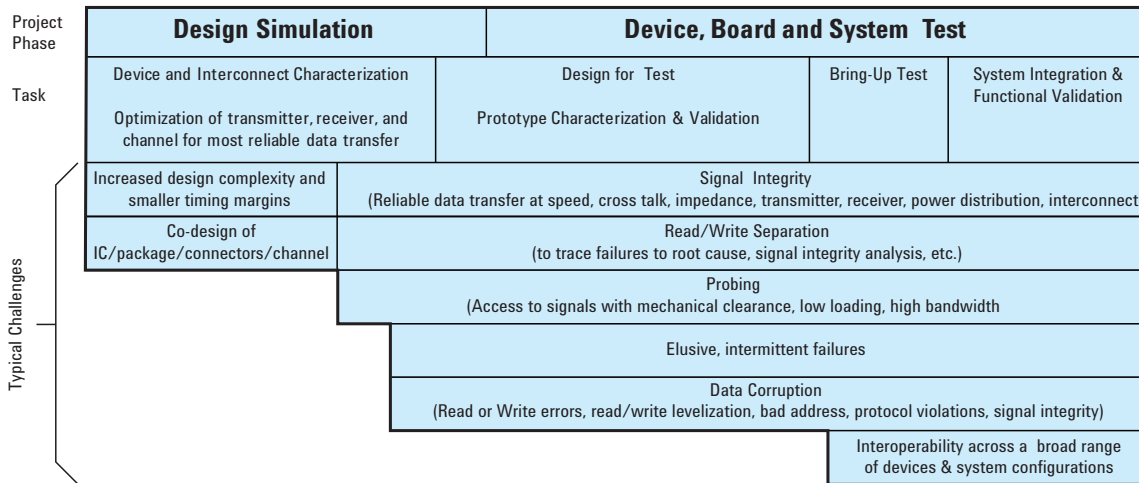


Figure 2. In the DDR memory development cycles the basic activities associated with each phase also present a number of typical challenges.

Although faster speeds offer significant benefits, they also present issues that complicate design and validation. The goal is to manage these issues and ensure good signal integrity. Doing so guarantees system interoperability, improves device performance and allows greater design margins. Figure 2 summarizes the DDR memory development cycle and outlines the typical DDR validation challenges that designers and engineers face. See the collection of DDR tutorial documents for techniques and tools to tackle each of these challenges:

- Simulating device and interconnect validation
- Probing for physical layer and functional testing
- Testing signal integrity and debugging DDR failures
- Finding and identifying causes of data corruption and elusive failures
- Separating read/write signals for DRAM and controller validation
- Ensuring DDR compliance and interoperability

Simulating device and interconnect validation

When designers need to analyze their driver and receiver prior to having the silicon available, it can be difficult to see the behavior of these devices. This process is further complicated by the difficulty of getting accurate packet analysis results. How do you fully characterize and optimize your DDR memory designs in a single, integrated design environment?

See *Simulating Device and Interconnect Validation*, tutorial 5990-3317EN for more information.

Probing for physical layer and functional testing

JEDEC defines the DDR specifications at the ballout of the DRAM Fine Ball-Grid Array (FBGA) package. The ballout is located beneath the FBGA package, which makes it difficult to probe the signals for true compliance. Engineers commonly probe signals at vias or termination resistors, but this usually compromises measurement results. Undesirable effects come into play, including signal reflection, distortion and skew. How do you probe in a way that ensures you accurately see your signal's behavior?

See *Probing for Physical Layer and Functional Validation*, Tutorial 5990-3182EN for more information.

Common DDR Validation Challenges (continued)

Testing signal integrity and debugging DDR failures

To troubleshoot DDR device failures, engineers need to conduct root cause analysis. This can prove to be a tough and tedious task. Various design issues and system sources can cause failures, so time spent identifying and troubleshooting problems can delay a project schedule and time to market. With the right tools, you can quickly find the root causes of failures and fix them. Additionally, designers can analyze a signal down to an expect bit error rate. What tools are available to effectively identify and troubleshoot signal integrity and debug failures?

See *Testing Signal Integrity in DDR Designs*, Tutorial 5990-3189EN.

See *Valid Data Window and Bit Error Rate testing for DDR Designs*, Tutorial 5991-1581EN.

Finding and identifying causes of data corruption and elusive failures

There are times when tracking infrequent errors or events can be challenging because they do not happen regularly. What if a glitch happens once every 5 minutes which can only be observed in infinite persistence display mode? Without the ability to track it, the condition when the glitch happens cannot be fully understood. Some other scenarios include signal overshoot due to crosstalk when the adjacent signal transition or ISI failure due to specific DQ pattern. How do you find and debug intermittent errors?

See *Identifying the Causes of Data Corruption and Elusive Failures*, Tutorial 5990-3183EN for more information.

Separating read/write signals for DRAM and controller validation

The main DDR operations are read and write – but both operations use the same strobe and data lines for signal transmission. To characterize these signals' electrical and timing parameters, you need to differentiate the complex traffic on the data bus for further analysis. The traffic consists of read data (output), write data (input) and high-impedance states (idle). Eight data buses constitute one data group which is source-synchronous to one strobe signal. To make things even more complicated, the write data is shifted 90 degrees from the read data with reference to the strobe signal edges, as Figure 3 shows. How can you easily and reliably separate the read and write cycles?

See *Separating Read/Write Signals for DRAM and Controller Validation*, Tutorial 5990-3187EN for more information.

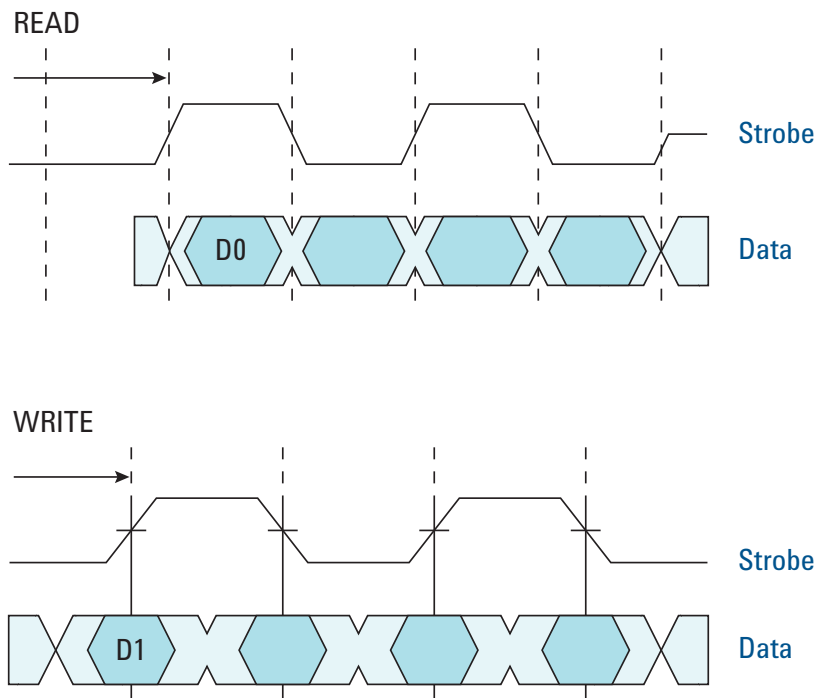


Figure 3. The strobe is active only during data bursts. The read signal aligns with the strobe edges; the write signal centers on the strobe edges.

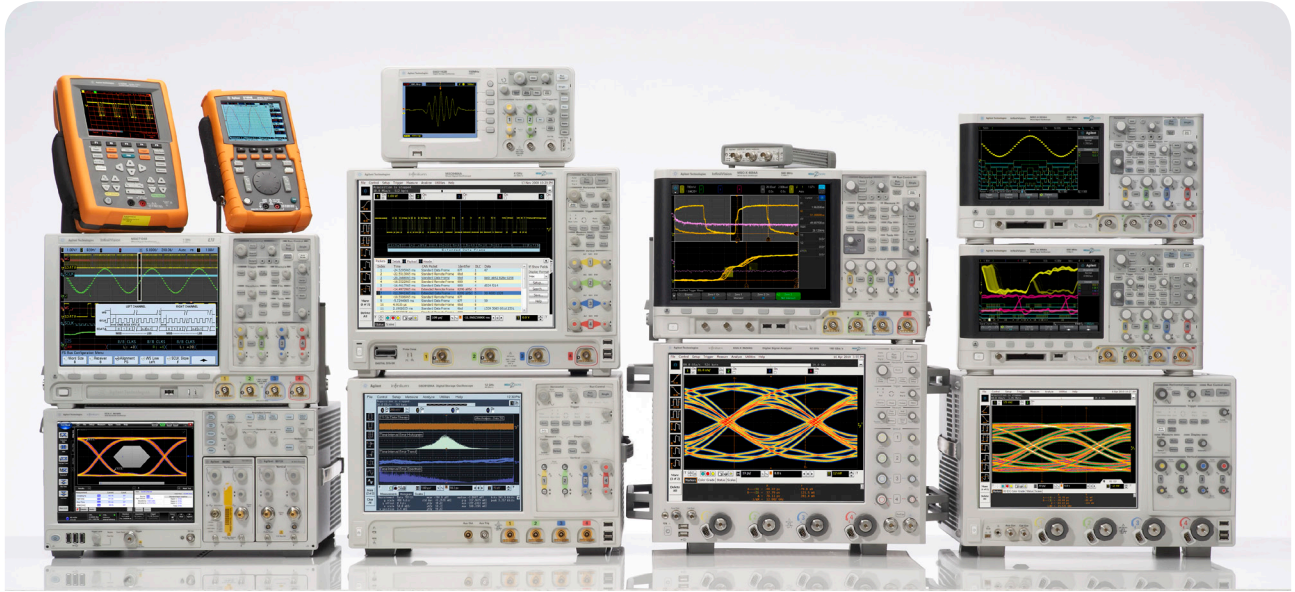
Ensuring DDR compliance and interoperability

The JEDEC specifications for DDR include a long list of measurements that must be carried out to ensure compliance. Engineers generally make the measurements manually, record the results and compare these with the specification to determine if the device is in compliance or not. Then the results need to be incorporated in a test report for sharing or archiving. This rigorous routine must be performed repeatedly for every revision or enhancement of the device. How can you reduce the time and effort required to ensure compliance and interoperability?

See *Ensuring Compliance and Interoperability in DDR Designs*, Tutorial 5990-3188EN for more information.

Find out how to overcome these challenges in DDR design and validation through this series of DDR tutorial documents. These tutorials further explain how the continual advancement in DDR technology and tools offers progressively improving solutions to your DDR memory challenges.

Publication title	Publication type	Publication number
<i>DDR Design and Verification through Simulation</i>	Tutorial	5990-3317EN
<i>DDR Probing for Physical Layer and Functional Testing</i>	Tutorial	5990-3182EN
<i>Debugging Signal Integrity and Protocol Layers on DDR Designs</i>	Tutorial	5990-3189EN
<i>Identifying the Causes of DDR Data Corruption and Elusive Failures</i>	Tutorial	5990-3183EN
<i>Separating Read/Write Signals for DDR DRAM and Controller Validation</i>	Tutorial	5990-3187EN
<i>Ensuring Compliance and Interoperability in DDR Designs</i>	Tutorial	5990-3188EN
<i>Agilent DDR Memory Solutions</i>	Tutorial	5990-3324EN
<i>Valid Data Window and Bit Error Rate Testing for DDR Designs</i>	Tutorial	5991-1581EN



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