

Agilent

N4971A Pattern Generator 13 Gb/s (PPG12500)

Data Sheet



Product highlights

- 24 Mb pattern memory supports virtually any pattern
- · Integrated two tap de-emphasis
- Fully programmable data and clock output parameters
- Transparent jitter pass-through
- Output calibrated near the point of use, not the front panel
- Single port remote control of all parameters through USB or GPIB
- GUI interface for multiple instrument control – N4980A application or LabVIEW[®] driver and GUI

Cost Effective Solution for Receiver Characterization

An affordable generator for characterization needs beyond PRBS patterns

The Agilent Technologies N4971A pattern generator 13 Gb/s (PPG12500) is a single channel generator capable of producing any serial data pattern up to 24 Mbits in length. An internal non-volatile pattern library comes preloaded with PRBS along with several common telecom and PC data bus test patterns. It can also store multiple user generated patterns. Output parameters of the data and clock outputs can be independently programmed, presets for common logic families simplify user set up. All outputs can supply differential or single ended signals.





Figure 1. Pattern generator 13 Gb/s plus clock synthesizer 16 GHz

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Pass-through jitter

Any calibrated jitter stress appearing on the clock input passes through to the data and clock outputs. Low intrinsic jitter contribution from the N4971A pattern generator 13 Gb/s (PPG12500) itself makes it ideal for receiver characterization using calibrated stress. The combination with the N4972A clock synthesizer 16 GHz (SCS16000J) results in a stressed programmable pattern generator priced less than half of competing serial BERT generator only versions.



or other test modes

· Transmitter emulation for general receiver characterization

equalization optimization such as 10 Gb/s Base-KR

Verification of tolerance to over and under applied pre-emphasis

Protocol simulation during development of systems employing closed loop

· Packet generation for initiating receiver loopback, internal BER counting,

Typical applications

Integrated de-emphasis

The N4971A pattern generator 13 Gb/s (PPG12500) includes integrated two tap de-emphasis signal conditioning. Commonly used in higher data rate systems to open eyes by counteracting high frequency loss in the channel, applying de-emphasis to the test signal is required for receiver testing. Other vendors' generators require additional dedicated external signal processors. The internal de-emphasis conditioning in the N4971A pattern generator 13 Gb/s (PPG12500) eliminates the expense of additional signal processors, as well as the associated signal degradation resulting from the extra cables used to connect them.

Figure 2. Integrated de-emphasis

Output calibration near the DUT

Most competitive pattern generators calibrate the output parameters at the output connector. As even the highest quality low loss cables create some frequency dependant loss, the user will generally need to adjust amplitude to de-embed cable loss effects in the system. The N4971A pattern generator 13 Gb/s (PPG12500) output parameters and waveshape are factory calibrated at the end of precision cables provided with the instrument, generally eliminating the need for de-embedding calibration.

Pattern editor

Pattern editor software included with the instrument provides a convenient tool for generation of user patterns in a PC running Microsoft Windows®. Familiar cut, copy and paste functions simplify the creation of repetitive portions of patterns. Data may be entered in hexadecimal or binary format. Integrated syntax checking screens for invalid characters before downloading patterns via USB interface into the N4971A pattern generator 13 Gb/s (PPG12500) library. The pattern editor software also allows for management of the user patterns in the N4971A pattern generator 13 Gb/s (PPG12500).

Eliminate downtime

User replaceable connector savers on the Data and Clock outputs eliminate down time. Should the output connectors be damaged through improper cable installation, simply replace the connector saver yourself without the need to send the instrument in for service.



Figure 4. Connector savers

Centralized control

Controlling multiple pattern generators or signal sources for characterizing multi-lane devices or cross talk is cumbersome and confusing. In addition to the need to address multiple instruments, the command syntax or user interface usually differs. The N4980A multi-instrument BERT software application provides customers the ability to control multiple instruments through a windows-based graphical user interface (GUI).

Set up is easy using N4980A multi-instrument BERT software application. For repetitive testing, setups can be stored and recalled at a later time.

The results view shows composite BER along with the performance of the individual lanes. Bar graphs give a quick indication of any lane specific problems without the need to look at the individual BER numbers.

Add Remove	• •	Gen Det Clk	P E N	12:1000 12:1010 4972A-C	(1100,0) (1100,1) J1:1222		Instant Accum	8.	0 343E-011	1e-1	5 1e-12 5 1e-12	1e-9 1e-9	1e-6	1e-3 1e-3	1e0 1e0	Data 💿 Sync 🍩 Error 🜑
Up Down	() 1	Gen Det Clk	P E N	12:1030 12:1010 14972A-0	(1100.2) (1100.1) J1:1222		Instant Accum	5.	0 420E-012	1e-1	5 1e-12 5 1e-12	 1e-9 1e-9	1 e -6 1 e -6	1e-3 1e-3	1e0	Data 💿 Sync 🥯 Error 🛢
	2 2	Gen Det Clk	P E N	12:1040 12:1010 4972A-0	(1100,3) (1100,1) ີ່ມ1:1222		Instant Accum		0	1e-1	5 1e-12 5 1e-12	 1e-9 1e-9	 1e-6 1e-6	1e-3	1e0	Data 🔘 Sync 🥌 Error 🛑
	() 3	Gen Det Clk	P E	12:1050 12:1010 N49	(1100,4) (1100,1) 71A:1000		Instant Accum	2 . 4.	759E-010 674E-011) 1e-1	5 1e-12 5 1e-12	1e-9 1e-9	1e-6	1e-3 1e-3	1e0	Data 💿 Sync 🥯 Error 🖨
Meas Setup — Parallel BE Duration		R — Inst B Accu	ER m BER		3.506E-01	0	1e-15 1	e-12 1	 e-9 1 e-9 1	 e-6 16 e-6 16		e0				
	6		9			Accu	m Bit Count	6	.846E+01	1	Accum E	Error Cou	unt 🤇	2.400	E+001	

Figure 5. Multi-instrument BERT software

Initialization TG1C1-4	A PPG12500	Qu 4	N4971A GUI v1.0
Data Output Output CUIST Logic Level 1.60 DC Offset (V) 0.00 Term (V) 0.00 De-emph (dB) 2.5 Crossover (%) 50	Pattern Selection Pattern CJPAT.FPT Pattern Invert Error Inject Errlnj Length Errlnj Rate Aux Errlnj	Clock Input Clock Mode Auto • Freq (GHz) 10.31266 Delay (UI) 0.21 Clock Output Logic Level ECL • Ampl (V-se) 0.90 DC Offset (V) 1.35 Term (V) 2.200	Trigger and Div Clock Trigger Mode Pattern • DirClock Modulus \$66 DirClk Ampl (V-se) \$0.60 Update GUI Reset PPG12500 Slot • Save Recall

Also available, LabVIEW[®] open source code drivers and stand alone GUI for the N4971A pattern generator 13 Gb/s (PPG12500). All of the operating parameters of the N4971A pattern generator 13 Gb/s (PPG12500) are displayed in a single window, allowing the user to instantly see the state of the entire system.

Figure 6. LabVIEW window

Specifications

Clock input	
Input clock frequency	1 to 13 GHz
Input clock amplitude	200 mV to 2 V p-p
Differential data outputs	
Signal configuration	Differential. Will operate in single ended mode
Data line coding	Non-return to zero (NRZ)
Output amplitude	200 mV to 1.6 V p-p, single ended
Output offset range	-2.0 V to +2.0 V
Termination voltage range	-2.0 V to +2.0 V
Cross-over adjustment range	25 to 75%
Rise & fall time	≤30 ps, 25 ps typical
Additive jitter	≤20 ps p-p, 10 ps p-p typical
Data delay range	±10 UI
De-emphasis	0 to 20 dB in 0.1dB steps
Error injection	Single or continuous at rates of 10 ⁻⁹ – 10 ⁻³ ,Burst length of 1, 2, 4, 8, 16, 32, 54, 128
Data patterns	2n-1 PRBS, where n=7,9,10,11,15,23,29,31
	2n PRBS, where n=7,10,11,13,15,23 with mark/space density of ½, ¼, ½, ¾, ½
	Selection of other common patterns e.g. CJPAT, CRPAT, K28-X, etc
Data connectors	2.92 mm, male
Differential clock outputs	
Signal configuration	Differential. Will operate in single ended mode
Output amplitude	200 mV to 1.8 V p-p, single ended
Output offset range	-2.0 V to +2.0 V
I ermination voltage range	-2.0 V to +2.0 V
Rise & fall time	≤40 ps
Additive jitter	≤3 ps rms, 1.5 ps rms typical
Clock connectors	2.92 mm, male
Differential divided clock outputs	
	Differential. Will operate in single ended mode
Clock output divider ratio	8 to 511 in steps of 1
	200 mV to 600 mV Vp-p, single ended
Rise & fall time	50 ps typical
UIVIAEd CIOCK CONNECTORS	Sivia temaie
Tuinney autout	
Output type	Cleak : 256 or pattern synahranized
Output type	400 mV n n contared around 1000 mV offect
	400 mV p-p, centered around +300 mV onset
Ingger connector	SINA lelliale
System	
Bemote control interface	USB2 0 and IEEE_088 (GPIR)
Power requirements	
Voltane	100 to 240 VAC autoranging
Frequency	50 to 60 Hz
Power consumption	170 W maximum
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Physical and environmental

Temperature, operating	+10° to +40 °C
Temperature, non-operating	-40° to +70 °C
Dimensions (height, width, and depth)	53 mm (2.1 in) x 425 mm (16.7 in) x 425 mm (16.7 in)
Mass	3.2 kg (7.0 lbs)

Regulatory standards

EMC	CISPR Pub 11 Group 1, clas	s A					
	AS/NZS CISPR 11						
	ICES/NMB-001						
	This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme a la norme NMB-001 du Canada.						
Safety	Complies with European Low Vol	tage Directive 2006/95/EC					
	 IEC/EN 61010-1, 2nd Edition Canada: CSA C22.2 No. 61010-1 						
	• USA: UL std no. 61010-1, 2nd Edition						
	German Acoustic statement						
	Acoustic noise emission	Geraeuschemission					
	LpA <70 dB	LpA <70 dB					
	Operator position	Am Arbeitsplatz					
	Normal position	Normaler Betrieb					
	Per ISO 7779	Nach DIN 45635 t.19					

Ordering information

Model	Description
N4971A (PPG12500)	Pattern generator 13 Gb/s
N4972A (SCS16000)	Clock synthesizer 16 GHz

Warranty and calibration service

For warranty and calibration service information, contact your local authorized Agilent Distributor or Agilent Sales Department.

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