

Keysight Technologies

x1149 Boundary Scan Analyzer

Data Sheet



Overview

Product description

The Keysight Technologies, Inc. x1149 boundary scan analyzer is a printed circuit board tester in compliance with the IEEE 1149.1 Standard test access port (TAP) and boundary scan architecture. The Keysight x1149 offers an easy to use software interface for development, debug and production runtime.

Industries and Applications

- Computational and server board test
- Network communication board test
- Aerospace and defense
- Automotive electronics test
- Industrial electronics test
- Medical device test

Process Outline
Guides user through test development and debug.

Project Explorer
Navigate to sections of the test at a click.

Click to select chain.

Generate Multi-Chain
Scan Path Linker combines chains at a click.

Configure/Reconfigure Chain
Automatically sets up chains using board's net information.

Graphical view of the selected chain.
Mouse over to retrieve the TAP information.

All information of the devices in the chain at a glance.

Chain Name	Type	Device Cou	Has OBI	TDI	TDO	TMS	TCK	TRST	GND	Header	TAP Por	Remarks
U19_U59	Single	3		TDL_RAPS	TDO_PRC	TMS_ALTERA	TCK_RAPS		GND	NA		
U24_U77	Single	8		TDL_S466	TDO_XG12	TMS_JTG1	TCK_S466	TRST_JTGL	GND	NA		
U31_U31	Single	1		JTG_TDI	ST_JTG_TDO	JTG_TMS	JTG_TCK	JTG_TRST	GND	NA		
U93_U101	Single	5		TDL_QDR1	TDO_RLD2	TMS_QDR	TCK_QDR1		GND	NA		

Pos	Name	Board Abbr	Part Number	BSDL	Package	OBI	TDI	TDO	TMS	TCK	TRST	Scan Type	Ignore
1	U24		BCM5466R_A0_S1	bcm5466r_a0.bsd	FBGA_256		TDL_S466	TDO_S466	TMS_JTG1	TCK_S466	TRST_JTGL	Full	
2	U57		BBK8483_SETUP	bbk8483.bsd	FCBGA		TDL_SPI	TDO_SPI	TMS_JTG1	TCK_SPI	TRST_JTGL	Full	
3	U56		BCM5482S_BGA1	bcm5482s_bga1.bsd	BGA_121		TDL_S482	TDO_S482	TMS_JTG1	TCK_S482	TRST_JTGL	Full	
4	U55		BCM8011_SETUP	bcm8011_bsd.bsd	FBGA_324		TDL_B011	TDO_B011	TMS_JTG1	TCK_B011	TRST_JTGL	Full	
5	U71		NP2_V4_SETUP	np2_v4.bsd	DW		TDL_EZ	TDO_EZ	TMS_JTG1	TCK_EZ	TRST_JTGL	Full	
6	U58		BCM5630XB1_SE1	bcm5630xb1.bsd	FCBGA_1156		TDL_S6303	TDO_S6303	TMS_JTG1	TCK_S6303	TRST_JTGL	Full	
7	U70		QT2032V7_SETUP	qt2032v7.bsd	CABGA15x15		TDL_XG11	TDO_XG11	TMS_JTG1	TCK_XG11	TRST_JTGL	Full	
8	U77		QT2032V7_SETUP	qt2032v7.bsd	CABGA15x15		TDL_XG12	TDO_XG12	TMS_JTG1	TCK_XG12	TRST_JTGL	Full	

Minimize **Process Outline** to increase viewable area.

Click to select view.

All information displayed for easy reference.

The screenshot shows the x1149 Boundary Scan Analyzer software interface. The main window is titled "x1149 Boundary Scan Analyzer (HelixM2~U4) (630-7327.v2)". The interface includes a menu bar (File, Debug, Tools, Report, Help), a toolbar with various icons, and a Project Explorer on the left. The Project Explorer shows a tree view with "Test" selected. The main area displays a table of test results and a table of nodes.

Test Results Table:

Chain Name	Test Name	Test Type	Device Tested	Marked	Permanent	Executable	Test Result	Remark	Created Time	Created
HelixM2~U1_HelixM2~U4	breg	BReg Length		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>			Jan-29-2013 01:07:13 PM	Engineer
HelixM2~U1_HelixM2~U4	ce_HelixM2~J3	Cover Extend	HelixM2~J3	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>			Jan-29-2013 01:07:12 PM	Engineer
HelixM2~U1_HelixM2~U4	ce_HelixM2~J9	Cover Extend	HelixM2~J9	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>			Jan-29-2013 01:07:12 PM	Engineer
HelixM2~U1_HelixM2~U4	disable	Disable		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>			Jan-29-2013 01:07:13 PM	Engineer
HelixM2~U1_HelixM2~U4	idcode	ID Code		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>			Jan-29-2013 01:07:13 PM	Engineer
HelixM2~U1_HelixM2~U4	integrity	Integrity		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>			Jan-29-2013 01:07:13 PM	Engineer
HelixM2~U1_HelixM2~U4	interconnect	Interconnect		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>			Jan-29-2013 01:07:13 PM	Engineer
HelixM2~U1_HelixM2~U4	interconnect_dot5	Interconnect Dot5		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>			Jan-29-2013 01:07:13 PM	Engineer
HelixM2~U1_HelixM2~U4	pullup_pulldown	Resistor Pull Up/Down		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>			Jan-29-2013 01:07:14 PM	Engineer
HelixM2~U1_HelixM2~U4	shorted_cap_dot5	Shorted Cap Dot5		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>			Jan-29-2013 01:07:14 PM	Engineer

All Nodes Table:

Name	Schematic Name	Board Abbrev	Monitor Voltage	Monitoring Upper Limit (Volt)	Monitoring Lower Limit (Volt)	Monitoring TAP Port	Monitoring Ground Node	Pin Count	Node Type
+3_3V_A	+3_3V_A	HelixM2	<input checked="" type="checkbox"/>	3.4	3.2			60	High
+3_3V_B	+3_3V_B	HelixM2	<input type="checkbox"/>	0	0			13	High
10PF_CAP1	10PF_CAP1	HelixM2	<input type="checkbox"/>	0	0			1	
10PF_CAP2	10PF_CAP2	HelixM2	<input type="checkbox"/>	0	0			1	
22PF_CAP1	22PF_CAP1	HelixM2	<input type="checkbox"/>	0	0			1	
22PF_CAP2	22PF_CAP2	HelixM2	<input type="checkbox"/>	0	0			1	

Output Window:

```

Project C:\Helix_Main\Helix_S1630-7327.v2
Project C:\Helix_Main\Helix_S1630-7327.v2
Error - Test (HelixM2~U106_HelixM2~U4)
Error - Test (HelixM2~U106_HelixM2~U4)
Error - Test (HelixM2~U106_HelixM2~U4)
    
```

On board voltage can be verified within an upper and lower limit.

Dock the selected window into your preferred location on the screen.

Output

Shows the results of all the tests for the chain(s).

Results of tests are highlighted in colors.

Test results can be sorted by clicking on the title tab.

The screenshot displays the Boundary Scan Analyzer interface. The main window shows a 'Test List' for 'Agilent x1149' with the following data:

Chain Name	Test Name	Test Type	Device Tested	Marked Permanent	Executable	Test Result	Remark	Created Time	Created By	Last Modified
U1_U4	integrity	Integrity			<input checked="" type="checkbox"/>	Passed		Jan-29-2013 05:54:43 PM	Engineer	Jan-29-2013
U1_U4	interconnect	Interconnect			<input checked="" type="checkbox"/>	Failed		Jan-29-2013 05:54:42 PM	Engineer	Jan-29-2013
U1_U4	interconnect_dot6	Interconnect Dot6			<input checked="" type="checkbox"/>			Jan-29-2013 05:54:42 PM	Engineer	Jan-29-2013
U1_U4	pullup_pulldown	Resistor Pull Up/Down			<input checked="" type="checkbox"/>			Jan-29-2013 05:54:44 PM	Engineer	Jan-29-2013

The 'Output' window shows the following log and summary tables:

```

Project C:\Program Files (x86)\Agilent\x1149\boards\Cherry-A-290113.absp opened successfully.
Jan-29-2013 05:58:38 PM: Test execution started...
Jan-29-2013 05:58:38 PM: Start executing test U1_U4:integrity ...
Jan-29-2013 05:58:38 PM: U1_U4-integrity test execution result: Passed.
Jan-29-2013 05:58:38 PM: Test execution finished.
Debug Test Summary (Jan-29-2013 05:58:38 PM):
| Test | Run Option | Total Run | Pass | Fail | Pass Rate |
|-----|-----|-----|-----|-----|-----|
| U1_U4-integrity | Run Once | 1 | 1 | 0 | 100.00 % |
Jan-29-2013 05:58:41 PM: Test execution started...
Jan-29-2013 05:58:42 PM: Start executing test U1_U4:interconnect ...
Jan-29-2013 05:58:42 PM: U1_U4-interconnect test execution result: Failed.
Jan-29-2013 05:58:42 PM: Test execution finished.
Debug Test Summary (Jan-29-2013 05:58:42 PM):
| Test | Run Option | Total Run | Pass | Fail | Pass Rate |
|-----|-----|-----|-----|-----|-----|
| U1_U4-interconnect | Run Once | 1 | 0 | 1 | 0.00 % |
    
```

The 'Repair Ticket' window provides a detailed analysis of the failed interconnect test:

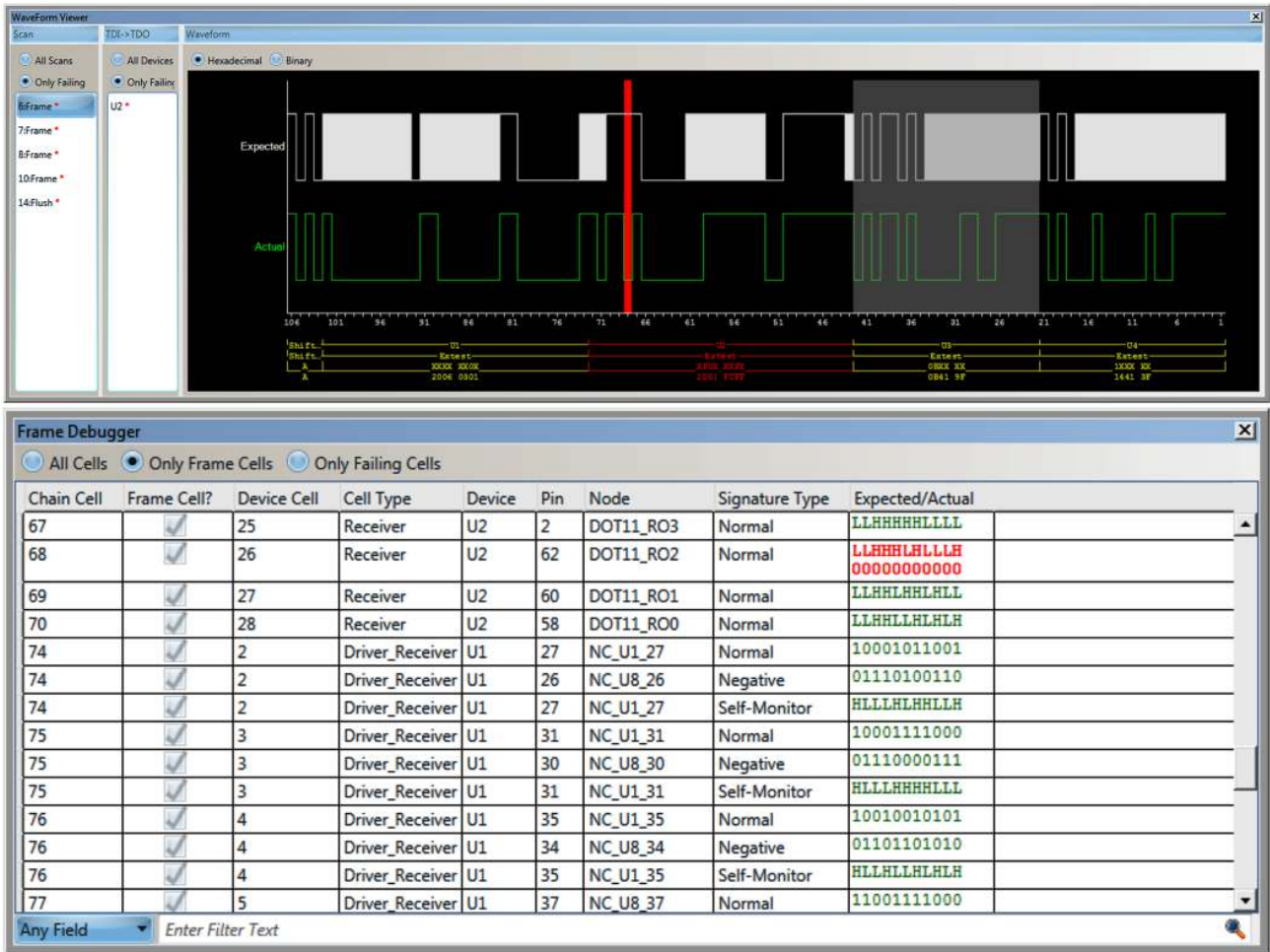
```

U1_U4:interconnect
Tue Jan 29 17:58:42 2013
-----
# 1 of 2
Frame stuck at 0
Suspect open or short to ground
Possible fail at
Node : D0762_IN0_P(U3.47, U4.14)
Expected: 10001001011
Actual: 00000000000
# 2 of 2
Frame stuck at 1
Suspect open or short to power
Possible fail at
Node : D0762_IN0_P(U3.48, U4.13)
Expected: 01110110100
Actual: 11111111111
    
```


Repair Ticket

Pin-level failure reporting and possible cause.

Choice of Waveform Viewer or Frame Debugger views to debug the test.



Product characteristics and general specifications

Controller interface	Ethernet 10/100 MB
	High speed USB 2.0 (For firmware upgrade only)
Power requirement	+12 VDC (typical)
	2 A (maximum) input rated current
	Installation category II
Power consumption	+12 VDC, 260 mA (maximum)
Standard shipped accessories	AC/DC power adapter
	Power cord
	USB cable
	HDMI cable
	Diagnostic clip
	Keysight x1149 boundary scan analyzer 'Quick Start Guide'
	Keysight x1149 software release CD-ROM
	Certificate of calibration
* Compatible with Microsoft® Windows® operating systems only.	
Operating environment	Operating temperature from 0 °C to +55 °C
	Relative humidity at 15% to 85% at 40 °C (non-condensing)
	For indoor use only
Storage compliance	-20 °C to 70 °C
Safety compliance	

Dimensions



Boundary Scan Controller dimension (width × depth × height)	290 mm x 220 mm x 75 mm / 11.417 in x 8.66 in x 2.95 in
Weight	550 g



TAP/IO port dimension (width × depth × height)	120.3 mm x 44.5 mm x 21 mm / 4.72 in x 1.75 in x 0.826 in
Weight	80 g
Warranty	One year plus 2nd year extended warranty.
Software update subscription	One year plus 2nd year extended subscription.

General specifications

Parameter/Specification	
Driver/receiver resources	
Types	GPIO, JTAG TAP
GPIO (General Purpose Input/Output)	5 output/driver pins programmable voltage and share with the common (VREF) Voltage Reference 4 input/receiver pins with fully programmable receiver voltage.
JTAG Test Access Port (TAP)	Supports up to 4 TAP each with TCK,TDI,TDO,TMS with optional TRST signals as defined by IEEE Std 1149.1 TDI, TMS, TRST programmable voltage reference share common VREF with the GP-output pins TDO programmable voltage receiver TCK has a separate programmable voltage reference (VREF) and slew rate.
Cover-Extend Technology (CET)	
Vectorless Enhanced (VTEP)	CET ARM, CET Rx/Tx, VTEP CLK/A/B/Hi/Lo+12 VDC Power
Ground pins	
Fixed location grounds per TAP module	TAP Module pins 1,3,5,7

Hardware GPIO (General Purpose Input/Output) specifications

Parameter/Specification GPIO Specifications	
Resources	5 drivers & 4 receivers with GND pins shared with TAP Pins
Sample/update rate READ, WRITE, READ/WRITE maximum sample/update rate	10 KHz / 100 usec
Per-pin settable features	OUT: data value (0,1, or Z)
	"0" – ≤ 100 mV
	"1" – $\geq VREF-100$ mV
	"Z" – High Z
	IN: VREF (1.1~5.0 V)
General Purpose Input or Receiver	
IN/Receiver	Read digital data "0" or "1", according to VREF and threshold voltage. It can be used to measure the external voltage range from 0 V to 5 V
Reference channel group	+5 V to 0 V in 100 mV steps
Timing	De-skewed. No programmable edges
Termination	> 1 M Ω
Error Detection:	Windowing (two point receive reference), over-voltage, under-voltage, drive-check validation (receiver used to verify driver achieved drive state)
General Purpose Output or Driver	
Update rate(maximum)	10 KHz/100 μ s
Output voltage ³	Range: +5.0 V to +1.1 V, step resolution of 100 mV, static accuracy
Driver current ²	10 mA @ 5 V
	2 mA @ 2.5 V
Continuous output current into a short ³	50 mA at 5 V
	20 mA at 2.5 V
Rise/Fall time ⁴	< 20 ns @ 2.5 V
	< 50 ns @ 1.1 V
Tri-state leakage current (maximum range ⁵)	-65 μ A, +5 μ
Tri-state capacitance (maximum):	Maximum 0.7 nF
	Typical 0.45 nF
Disconnected capacitance	15 pF
Output skew (same board)	Typical < 5 ns
DC output resistance (typical)	35 - 50 Ω

Hardware JTAG TAP specifications

Parameter/Specification	Test Method
JTAG TAP Specifications	
Resources	TDI, TDO, TCK, TMS, TRST and a GND pair for each 4 TAP port
Clock maximum frequency	22.5 Mhz
Per-pin settable features	Data value (0,1, or Z), driver/receive reference; slew rate; termination high-impedance or 50 Ω
Timing	De-skewed. Programmable edges (TCK only)
JTAG TAP Receiver TDO	
Clock maximum frequency	11.25 Mhz
Reference voltage (thresholds)	High: +5 V
	Low: 0 V to 0.5 V
	Step resolution of 100 mV
	Static accuracy
Input voltage range	0 V to 5 V
Input resistance	> 40 K Ω
Pull-up terminations	100k Ω
JTAG TAP Driver TDI, TMS, TRST	
Clock maximum frequency	TDI – 11.25 MHz
	TMS – 7.5 MHz
	TRST – 10 KHz
Output voltage	+5 V to +1.1 V ²
Driver current ³	± 10 mA @ 5 V
	± 2 mA @ 2.5 V
Continuous output current into a short ³	≥ 50 mA at 5 V
	$> = 20$ mA at 2.5 V
Rise/Fall time ³	< 20 ns @ 2.5 V
	< 10 nS @ 1.1 V
Tri-state leakage current (maximum ⁵)	± 65 μ A
Tri-state capacitance (maximum)	1 nF
Output skew (TMS and TRST on all TAPs) (same board)	Typical ± 5 ns
DC output resistance (typical)	35 Ω , 50 Ω

Hardware JTAG TAP specifications (continued)

Parameter/Specification	
JTAP TAP Driver TCK	
Clock maximum frequency	22.5 Mhz
Output Voltage ²	0 to 5 volts with 100 mV resolution)
Driver current ³	10 mA @ 5 V 2 mA @ 2.5 V
Continuous output current ³	≥ 80 mA @ 5 V ≤ 40 mA at 2.5 V
Slew rate: (see note 6)	40 V/μsec to 380 V/μsec
Tri-state leakage current (maximum ⁵)	-3.7 μA
Tri-state capacitance (maximum)	1.1 nF
Disconnected capacitance	15 pF
DC output resistance (typical)	50 Ω

Notes

1. There are 4 GND pins per TAP module, which are common for both GPIO and TAP signals in the same TAP 20-pin connector. However, the GND pins in different TAP modules are isolated.
2. Vref can be configured from 1.1 V to 5.0 V with a step of 0.1 V, which is common to all GPO and TMS/TDI/TRST signals. Vref clk can be separately configured in some situations where the high voltage of TCK needs to be a little higher than the other TAP signals. The logic output high is set to a voltage range from (Vref - 0.2V) to Vref, while the logic low is less than 0.2 V when output current is not more than 0.1 mA.
3. Capable to produce an output current of 10 mA when Vref = 5 V, or 2 mA when Vref = 2.5 V; load 100 Ω for the drive current test. The maximum current is tested when the output pin shorts to GND.
4. Rise time refers to the period when a signal rises from 0.1 Vref to 0.9V ref; fall time is the period when a signal falls from 0.9 Vref to 0.1 Vref.
5. Set the output at high-Z state and connect the pin to GND to measure the positive leakage current; connect the pin to a maximum voltage of power reference value (Vref) for negative leakage current measurement.
6. The TCK reference voltage is set to 5 V. When the voltage for slew rate configuration is set to 0.2 V, the reading of TCK slew rate is ≤ 30 V/uS; while this voltage is set 5 V, the reading is ≥ 400 V/uS.
7. The threshold voltage of TDO is normally set between 0.5 V and 3.5 V. The logic reading from TDO would be '1' if the input voltage ≥ (0.1 V + threshold voltage), and '0' if the input ≤ (threshold voltage - 0.1 V).

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