

775 Nanovolt Noise Measurement for a Low Noise Voltage Reference

Quantifying Silence

by Jim Williams

Introduction

Frequently, voltage reference stability and noise define measurement limits in instrumentation systems. In particular, reference noise often sets stable resolution limits.

Reference voltages have decreased with the continuing drop in system power supply voltages, making reference noise increasingly important. The compressed signal processing range mandates a commensurate reduction in reference noise to maintain resolution. Noise ultimately translates into quantization uncertainty in ADCs, introducing jitter in applications such as scales, inertial navigation systems, infrared thermography, DVMs and medical imaging apparatus.

A new low voltage reference, the LTC6655, has only 0.3ppm (775nV) noise at 2.5V_{OUT}. Table 1 lists salient specifications in tabular form. Accuracy and temperature coefficient are characteristic of high grade, low voltage references. 0.1Hz to 10Hz noise, particularly noteworthy, is unequalled by any low voltage electronic reference.

Noise Measurement

Special techniques are required to verify the LTC6655's extremely low noise. Figure 1's approach appears innocently straightforward but practical

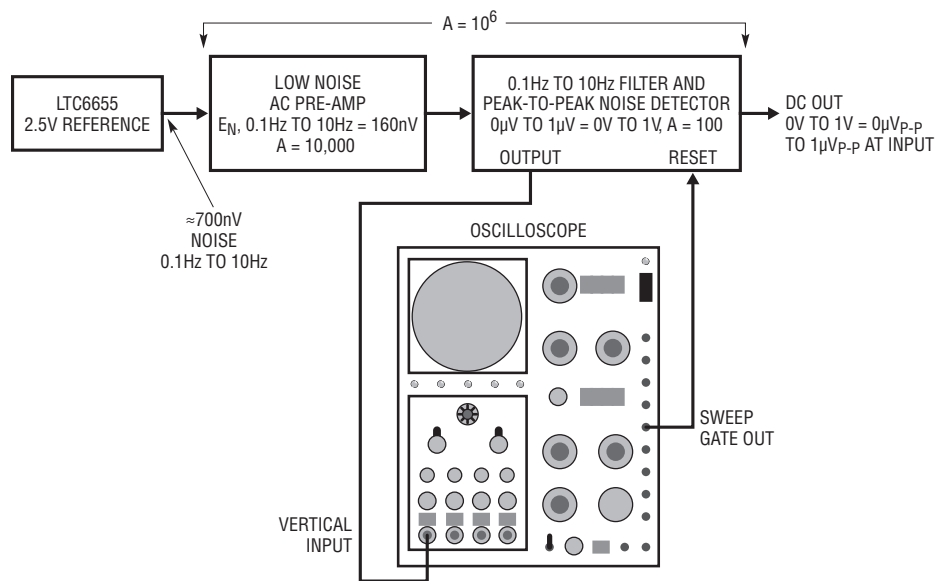


Figure 1. Conceptual 0.1Hz to 10Hz noise testing scheme includes low noise preamplifier, filter and peak-to-peak noise detector. Pre-amplifier's 160nV noise floor, enabling accurate measurement, requires special design and layout techniques.

implementation represents a high order difficulty measurement. This 0.1Hz to 10Hz noise testing scheme includes a low noise preamplifier, filters and a peak-to-peak noise detector. The pre-amplifier's 160nV noise floor, enabling accurate measurement, requires special design and layout techniques. A forward gain of 10⁶ permits readout by conventional instruments.

Figure 2's detailed schematic reveals some considerations required to achieve the 160nV noise floor. The references' DC potential is stripped by the 1300μF, 1.2k resistor combination; AC content is fed to Q1. Q1-Q2, extraordinarily low noise JFETs, are DC stabilized by A1, with A2 providing a single-ended output. Resistive feedback from A2 stabilizes the configuration at a gain of 10,000. A2's

Table 1. LTC6655 reference tabular specifications. The LTC6655 accuracy and temperature coefficient are characteristic of high grade, low voltage references. 0.1Hz to 10Hz noise, particularly noteworthy, is unequalled by any low voltage electronic reference.

SPECIFICATION	LIMITS
Output Voltages	1.250, 2.048, 2.500, 3.000, 3.300, 4.096, 5.000
Initial Accuracy	0.025%, 0.05%
Temperature Coefficient	2ppm/°C, 5ppm/°C
0.1Hz to 10Hz Noise	0.775μV at V _{OUT} = 2.500V, Peak-to-Peak Noise is within this Figure in 90% of 1000 10-Second Measurement Intervals
Additional Characteristics	5ppm/V Line Regulation, 500mV Dropout, Shutdown Pin, I _{SUPPLY} = 5mA, V _{IN} = V _O + 0.5V to 13.2V _{MAX} , I _{OUT(SINK/SOURCE)} = ±5mA, I _{SHORT-CIRCUIT} = 15mA.

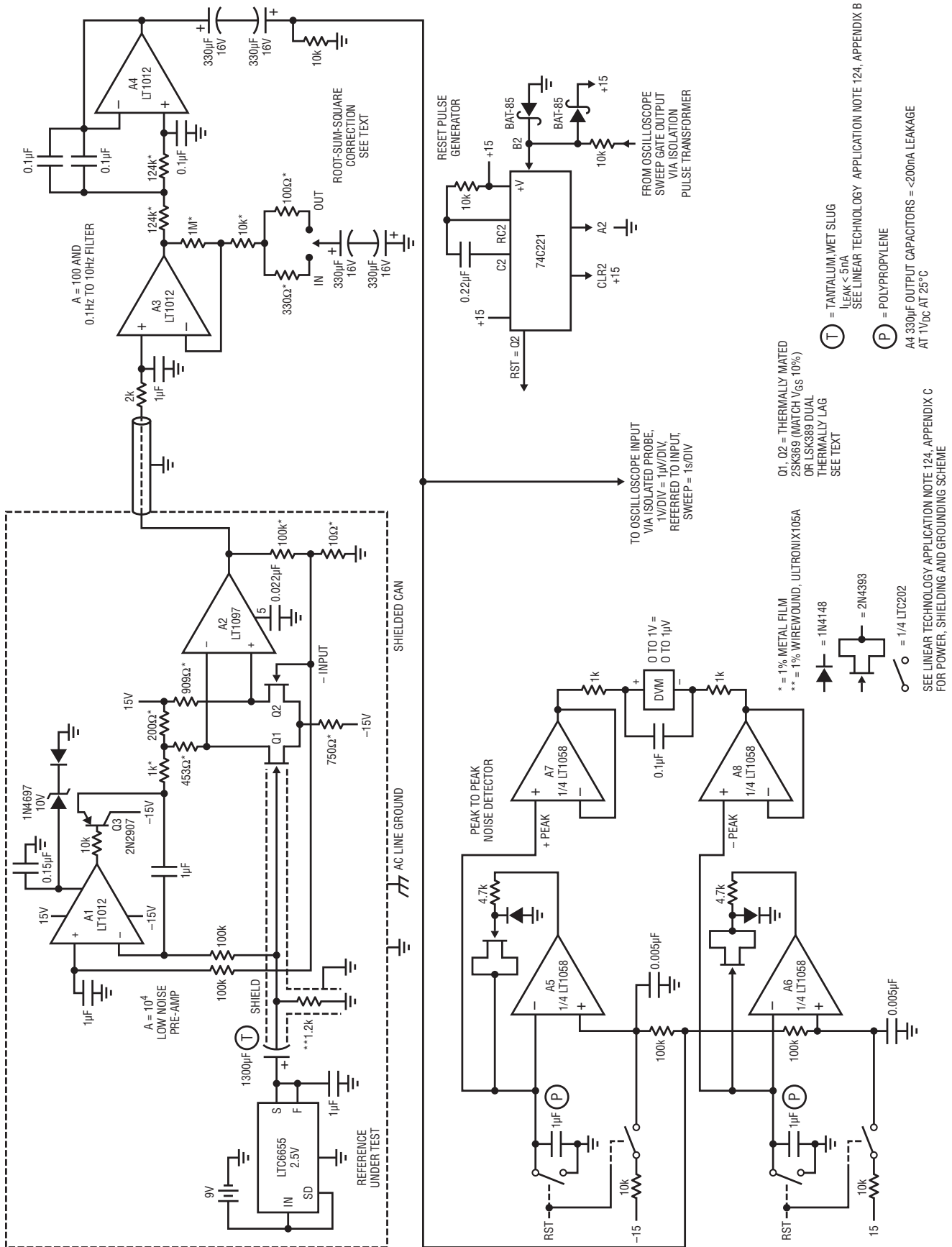


Figure 2. Detailed noise test circuitry. Thermally lagged Q1-Q2 low noise JFET pair is DC stabilized by A1-Q3; A2 delivers A = 10,000 preamplifier output. A3-A4 form 0.1Hz to 10Hz, A = 100, bandpass filter; total gain referred to pre-amplifier input is 10⁶. Peak-to-peak noise detector, reset by monitoring oscilloscope sweep gate, supplies DVM output.

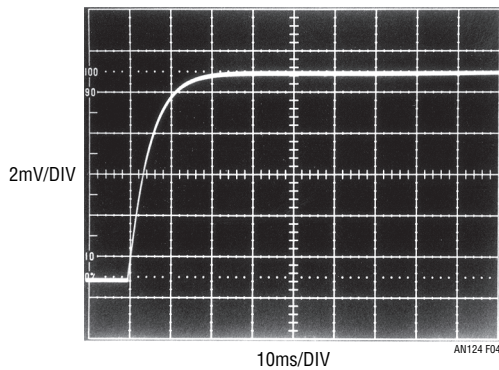


Figure 3. Preamplifier rise time measures 10ms; indicated 35Hz bandwidth ensures entire 0.1Hz to 10Hz noise spectrum is supplied to succeeding filter stage.

output is routed to amplifier-filter A3-A4 which provides 0.1Hz to 10Hz response at a gain of 100. A5-A8 comprise a peak-to-peak noise detector read out by a DVM at a scale factor of 1 volt/microvolt. The peak-to-peak noise detector provides high accuracy measurement, eliminating tedious interpretation of an oscilloscope display. Instantaneous noise value is supplied by the indicated output to a monitoring oscilloscope. The 74C221 one-shot, triggered by the oscilloscope sweep gate, resets the peak-to-peak noise detector at the end of each oscilloscope 10-second sweep.

Numerous details contribute to the circuit's performance. The 1300 μ F capacitor, a highly specialized type, is selected for leakage in accordance with the procedure given in Appendix B. Furthermore, it, and its associ-

ated low noise 1.2k resistor, are fully shielded against pick-up. FETs Q1 and Q2 differentially feed A2, forming a simple low noise op amp. Feedback, provided by the 100k-10 Ω pair, sets closed loop gain at 10,000. Although Q1 and Q2 have extraordinarily low noise characteristics, their offset and drift are uncontrolled. A1 corrects these deficiencies by adjusting Q1's channel current via Q3 to minimize the Q1-Q2 input difference. Q1's skewed drain values ensure that A1 is able to capture the offset. A1 and Q3 supply whatever current is required into Q1's channel to force offset within about 30 μ V. The FETs' V_{GS} can vary over a 4:1 range. Because of this, they must be selected for 10% V_{GS} matching. This matching allows A1 to capture the offset without introducing significant noise. Q1 and Q2 are thermally

mated and lagged in epoxy at a time constant much greater than A1's DC stabilizing loop roll-off, preventing offset instability and hunting. The entire A1-Q1-Q2-A2 assembly and the reference under test are completely enclosed within a shielded can.¹ The reference is powered by a 9V battery to minimize noise and insure freedom from ground loops.

Peak-to-peak detector design considerations include JFETs used as peak trapping diodes to obtain lower leakage than afforded by conventional diodes. Diodes at the FET gates clamp reverse voltage, further minimizing leakage.² The peak storage capacitors highly asymmetric charge-discharge profile necessitates the low dielectric absorption polypropylene capacitors specified.³ Oscilloscope connections via galvanically isolated links prevent

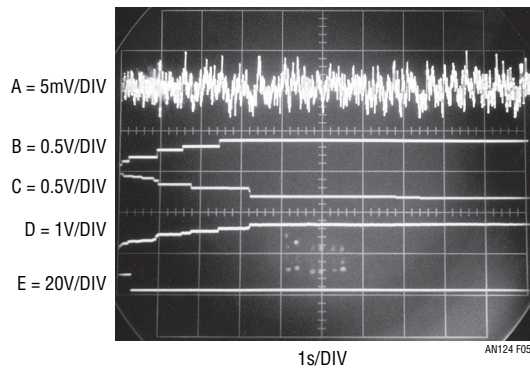


Figure 4. Waveforms for peak-to-peak noise detector include A3 input noise signal (trace A), A7 (trace B) positive/A8 (trace C) negative peak detector outputs and DVM differential input (trace D). Trace E's oscilloscope supplied reset pulse lengthened for photographic clarity.

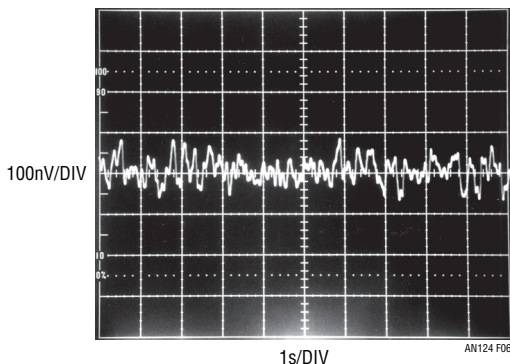


Figure 5. Low noise circuit/layout techniques yield 160nV 0.1Hz to 10Hz noise floor, ensuring accurate measurement. Photograph taken at Figure 3's oscilloscope output with 3V battery replacing LTC6655 reference. noise floor adds \approx 2% error to expected LTC6655 noise figure due to root-sum-square noise addition characteristic; correction is implemented at Figure 2's A3.

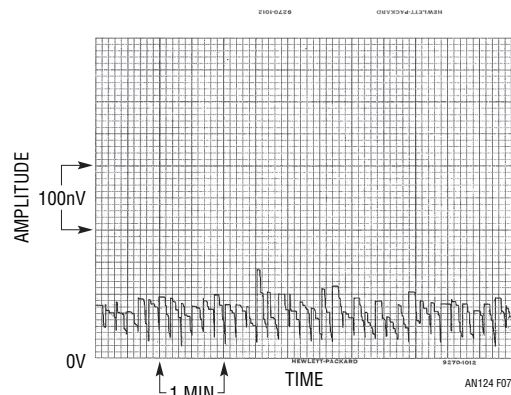


Figure 6. Peak-to-peak noise detector output observed over six minutes shows <160nV test circuit noise. Resets occur every 10 seconds. 3V battery biases input capacitor, replacing LTC6655 for this test.

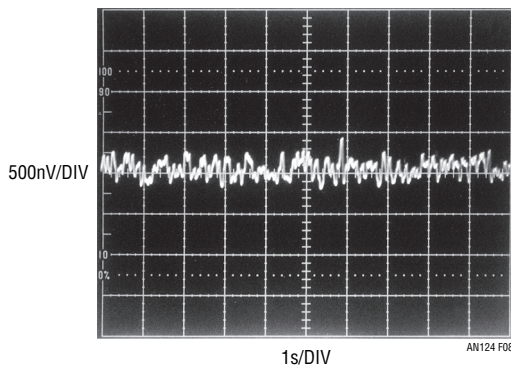


Figure 7. LTC6655 0.1Hz to 10Hz noise measures 775nV in 10-second sample time.

ground loop induced corruption. The oscilloscope input signal is supplied by an isolated probe; the sweep gate output is interfaced with an isolation pulse transformer. For more details, see Linear Technology Application Note 124, Appendix C.

Noise Measurement Circuit Performance


Circuit performance must be characterized prior to measuring LTC6655 noise. The preamplifier stage is verified for >10Hz bandwidth by applying a 1 μ V step at its input (reference disconnected) and monitoring A2's output. Figure 3's 10ms rise time indicates 35Hz response, insuring the entire 0.1Hz to 10Hz noise spectrum is supplied to the succeeding filter stage.

Figure 4 describes peak-to-peak noise detector operation. Waveforms include A3's input noise signal (Trace A), A7 (Trace B) positive/A8 (Trace C) negative peak detector outputs and

DVM differential input (Trace D). Trace E's oscilloscope supplied reset pulse has been lengthened for photographic clarity.

Circuit noise floor is measured by replacing the LTC6655 with a 3V battery stack. Dielectric absorption effects in the large input capacitor require a 24-hour settling period before measurement. Figure 5, taken at the circuit's oscilloscope output, shows 160nV 0.1Hz to 10Hz noise in a 10 second sample window. Because noise adds in root-sum-square fashion, this represents about a 2% error in the LTC6655's expected 775nV noise figure. This term is accounted for by placing Figure 2's "root-sum-square correction" switch in the appropriate position during reference testing. The resultant 2% gain attenuation first order corrects LTC6655 output noise reading for the circuit's 160nV noise floor contribution. Figure 6, a strip-chart recording of the peak-to-

peak noise detector output over six minutes, shows less than 160nV test circuit noise.⁴ Resets occur every 10 seconds. A 3V battery biases the input capacitor, replacing the LTC6655 for this test.

Figure 7 is LTC6655 noise after the indicated 24-hour dielectric absorption soak time. Noise is within 775nV peak-to-peak in this 10 second sample window with the root-sum-square correction enabled. The verified, extremely low circuit noise floor makes it highly likely this data is valid. In closing, it is worth mention that the approach taken is applicable to measuring any 0.1Hz to 10Hz noise source, although the root-sum-square error correction coefficient should be re-established for any given noise level. 

Notes

- ¹ The preamplifier structure must be carefully prepared. See Appendix A in Linear Technology Application Note 124, "Mechanical and Layout Considerations," for detail on preamplifier construction.
- ² Diode-connected JFETs' superior leakage derives from their extremely small area gate-channel junction. In general, JFETs leak a few picoamperes (25°C) while common signal diodes (e.g. 1N4148) are about 1,000 \times worse (units of nanoamperes at 25°C).
- ³ Teflon and polystyrene dielectrics are even better but the Real World intrudes. Teflon is expensive and excessively large at 1 μ F. Analog types mourn the imminent passing of the polystyrene era as the sole manufacturer of polystyrene film has ceased production.
- ⁴ That's right, a *strip-chart recording*. Stubborn, locally based aberrants persist in their use of such archaic devices, forsaking more modern alternatives. Technical advantage could account for this choice, although deeply seated cultural bias may be indicated.

LT3971/91, continued from page 5

and external clock synchronization features, and comes in a 10-pin MSOP or 3mm \times 3mm DFN package, both with an exposed ground pad.

The LT3991 has a typical minimum switch on time of 110ns at room and 150ns at 85°C, which allow higher switching frequencies for large step-down ratios when compared to other parts with similar high input voltage ratings. Figure 8 shows a 48V input to a 3.3V output application with a switching frequency of 300kHz. The 10 μ H inductor and 47 μ F output capacitor yield a small overall solution

size. The output capacitor can be a small ceramic capacitor, as opposed to a tantalum capacitor, because the LT3991 does not need any output capacitor ESR for stability.

Conclusion

The LT3971 and LT3991 are ultralow quiescent current regulators that can regulate a 12V input to a 3.3V output during no load conditions with only 2.8 μ A of input current. Light load operation with single current pulses keeps the output voltage ripple to less than 15mV. These buck regulators can also provide up to 1.2A of output

current. The LT3971 and LT3991 are well suited for keep-alive and remote monitoring systems with low duty cycle, high current, pulsed outputs. The wide input range from 4.3V up to 38V for the LT3971, and 55V for the LT3991, along with the programmable input voltage enable threshold feature, allow these converters to be driven from a wide range of input sources. The ultralow quiescent current performance of the LT3971 and LT3991 make them great choices for battery-operated systems where power conservation is critical. 