2.7MHz 3A Step-Down Converter with I²C Interface

General Description

The RT8088A is a full featured 5.5V, 3A, Constant-On-Time (COT) synchronous step-down converter with two integrated MOSFETs. The current mode COT operation with internal compensation allows the transient response to be optimized over a wide range of loads and output capacitors to efficiently reduce external component count. The RT8088A provides up to 3MHz switching frequency to minimize the size of output inductor and capacitors. The RT8088A is available in the WL-CSP-15B 1.31x2.11 (BSC) package.

Ordering Information

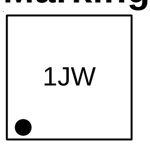
RT8088A□
Package Type
WSC : WL-CSP-15B 1.31x2.11 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



1J : Product Code

W : Date Code

Features

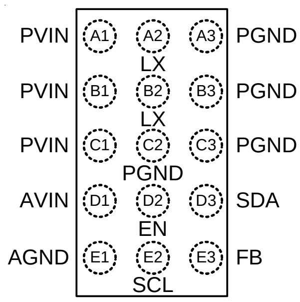
- **2.5V to 5.5V Input Voltage Range**
- **Current Mode COT Control Loop Design**
- **Fast Transient Response**
- **Internal 48mΩ and 22mΩ Synchronous Rectifier**
- **Highly Accurate V_{OUT} Regulation Over Load/Line Range**
- **Robust Loop Stability with Low-ESR C_{OUT}**
- **RoHS Compliant and Halogen Free**

Applications

- Distributed Power Systems
- Enterprise Servers, Ethernet Switches & Routers, and Global Storage Equipment
- Telecom & Industrial Equipment

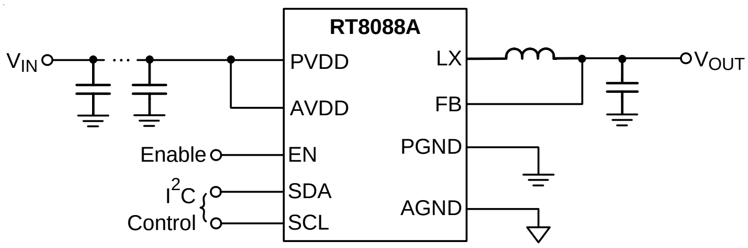
Pin Configurations

(TOP VIEW)



WL-CSP-15B 1.31x2.11 (BSC)

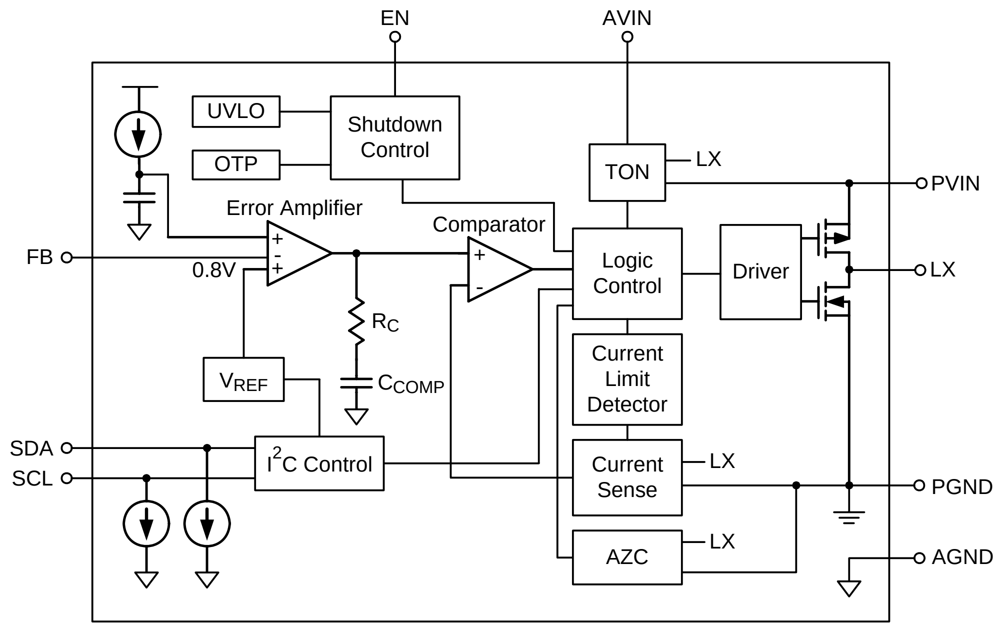
Simplified Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
A1, B1, C1	PVIN	Input Supply Voltage, 2.5V to 5.5V.
A2, B2	LX	Switch Node. The Source of the internal high-side power MOSFET, and Drain of the internal low-side (synchronous) rectifier MOSFET.
A3, B3, C2, C3	PGND	Power Ground.
D1	AVIN	Analog Circuit Input Supply Voltage.
D2	EN	Enable Control Input. Pull high to enable.
D3	SDA	I^2C Data Signal.
E1	AGND	Analog Ground Should be Electrically Connected to GND Close to the Device.
E2	SCL	I^2C Clock Signal.
E3	FB	Feedback Voltage Input.

Function Block Diagram



Operation

The RT8088A is a low voltage synchronous step-down converter that can support the input voltage range from 2.5V to 5.5V and the output current can be up to 3A. The RT8088A uses a constant on-time, current mode architecture. In steady-state operation, the high-side P-MOSFET is turned on when the current feedback reaches COMP level which is the amplified difference between the reference voltage and the feedback voltage. The on-time of high-side P-MOSFET is determined by on-time generator which is a function of input and output voltage. After on-time expires, high-side MOSFET is turned off and low-side MOSFET is turned on. Until the low-side current sensing signal reaches the COMP, the high-side MOSFET is turned on again. In this manner, the converter regulates the output voltage and keeps the frequency constant.

The RT8088A reduces the external component count by integrating the boot recharge MOSFET.

The error amplifier EA adjusts COMP voltage by comparing the output voltage with the internal I^2C set reference voltage. When the load increases, it causes a drop in the output relative to the reference, then the COMP voltage rises to allow higher inductor current to match the load current.

PWM Frequency and Adaptive On-Time Control

The on-time can be roughly estimated by the equation :

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$ where f_{SW} is nominal 3MHz

Auto-Zero Current Detector

The auto-zero current detector circuit senses the LX waveform to adjust the zero current threshold voltage. When the current of low-side MOSFET decreases to the zero current threshold, the low-side MOSFET turns off to prevent negative inductor current. In this way, the zero current threshold can adjust for different condition to get better efficiency.

Under-Voltage Lockout (UVLO)

The UVLO continuously monitors the VCC voltage to make sure the device works properly. When the VCC is high enough to reach the UVLO high threshold voltage, the step-down converter softly starts or pre-bias to its regulated output voltage. When the VCC decreases to its UVLO low threshold voltage, the device will shut down.

Power Good

When the output voltage is higher than PGOOD rising threshold, the PGOOD flag is high.

Output Under-Voltage Protection (UVP)

When the output voltage is lower than 0.4V after soft-start, the UVP is triggered. The system will be latched and the output voltage will no longer be regulated during UVP latched state. Re-start input voltage or EN pin can unlatch the protection state. Using I^2C to shutdown the system and then re-enable it will also unlatch UVP function.

Over-Current Protection (OCP)

The RT8088A senses the current signal when the low-side MOSFET turns on. As a result, The OCP is cycle-by-cycle limit. If the OCP occurs, the converter holds off the next on pulse until inductor current drops below the OCP limit.

Soft-Start

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The typical soft start time is 150μs.

Over-Temperature Protection (OTP)

The RT8088A has an over-temperature protection. When the device triggers the OTP, the system will be latched and the output voltage will no longer be regulated during OTP latched state. Re-start input voltage or EN pin can unlatch the protection state. Using I^2C to shutdown the system and then re-enable it will also unlatch UVP function.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- −0.3V to 6.5V
- Other Pins ---------- −0.3V to (V_{IN} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-15B 1.31x2.11 (BSC) ---------- 2W
- Package Thermal Resistance (Note 2)
  WL-CSP-15B 1.31x2.11 (BSC), θ_{JA} ---------- 49.8°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- −65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 2.5V to 5.5V
- Junction Temperature Range ---------- −40°C to 125°C
- Ambient Temperature Range ---------- −40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.7V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Under-Voltage Lockout Threshold		V_{UVLO}	V_{CC} Rising	--	2.35	--	V
Shutdown Supply Current		I_{SHDN}	EN = 0V	--	1	5	μA
Quiescent Current		I_Q	Active, V_{SENSE} = 0.9V, No Switching	--	75	100	μA
Voltage Reference		V_{REF}	At any set point, with a load from 0 to 3A and over input voltage range	−2	--	2	%
Soft-Start Time		t_{SS}		--	--	150	μs
Enable Input Voltage	Logic-High	V_{EN_H}	Rising	1.05	--	--	V
	Logic-Low	V_{EN_L}	Falling	--	--	0.4	
Switch On-Resistance	High-Side	R_{ONH}		--	48	--	mΩ
	Low-Side	R_{ONL}		--	22	--	
Current Limit Threshold		I_{CL}	Valley Current, IPEAK [1:0] = 11	--	3.9	--	A
Thermal Shutdown Threshold		T_S		--	150	--	°C
Switching Frequency		f_{OSC}		--	2.7	--	MHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Resolution	R_{ES}	Default V_{OUT} = 1.225V (Register 1100100)	7	--	--	Bits
DAC Step Size	V_{DAC}		--	6.25	--	mV
Minimum VOUT	V_{DACMIN}		--	600	--	mV
EN, SDA and SCL High	D_{HIGH}		1.05	--	--	V
EN, SDA and SCL Low	D_{LOW}		--	--	0.4	V
EN, SDA and SCL Current	$D_{CURRENT}$		--	--	0.1	mA

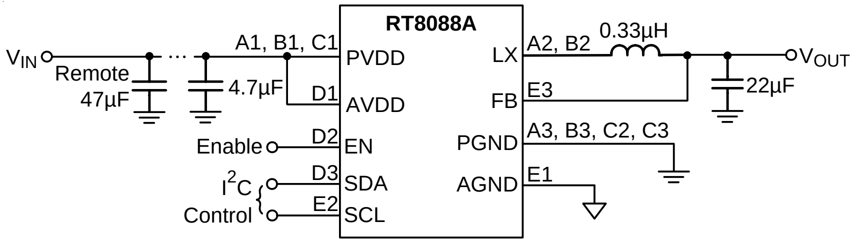
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

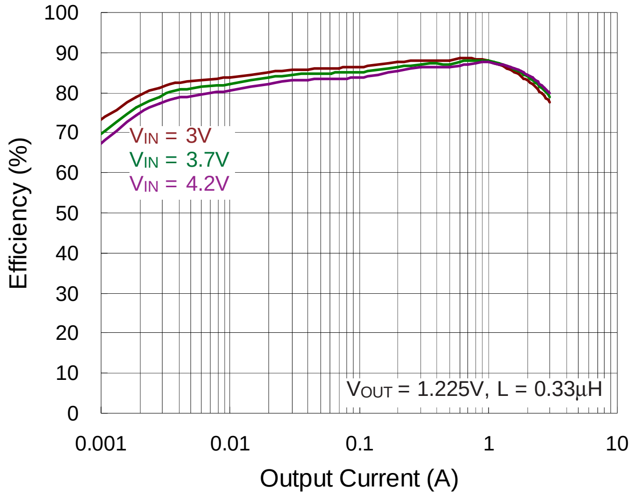
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

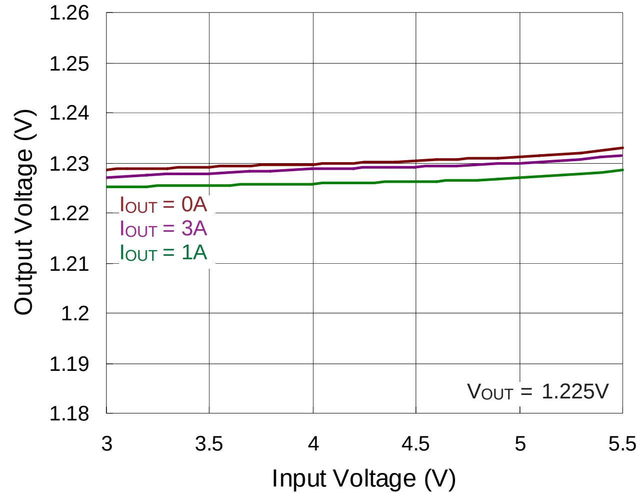


Typical Operating Characteristics

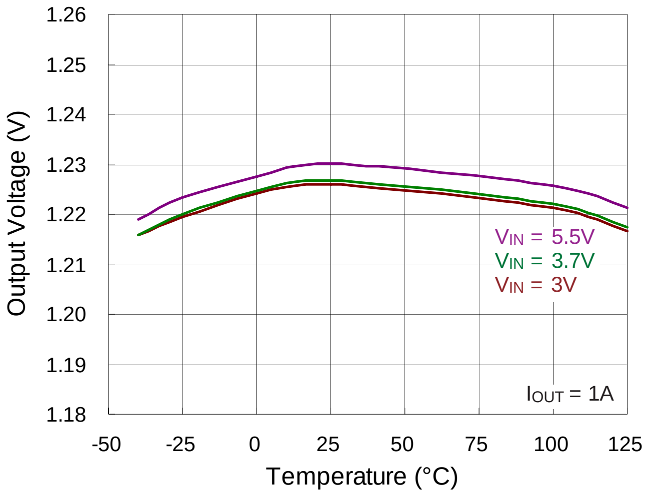
Efficiency vs. Output Current



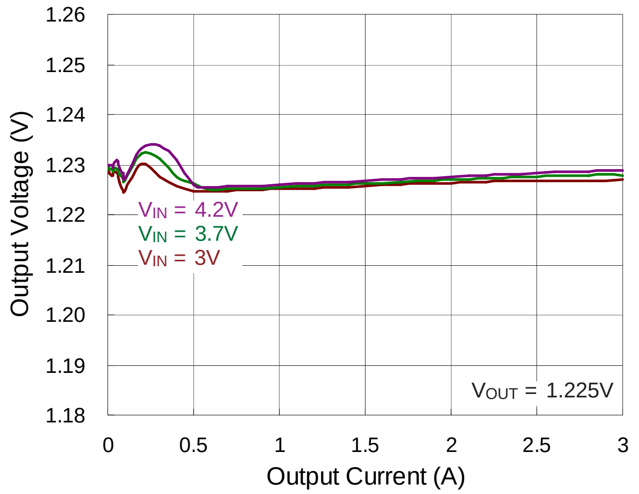
Output Voltage vs. Input Voltage



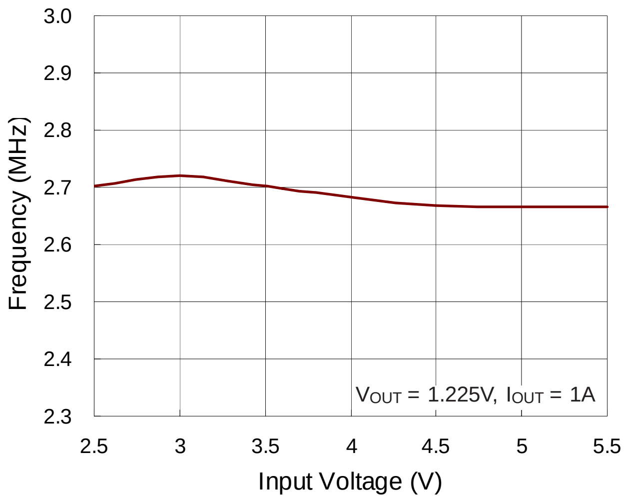
Output Voltage vs. Temperature



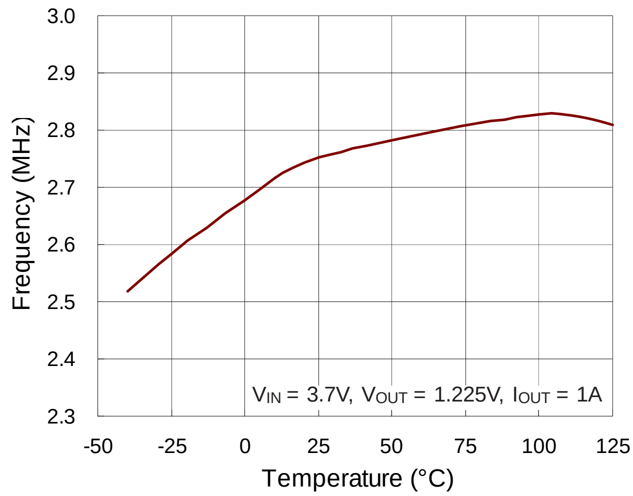
Output Voltage vs. Output Current

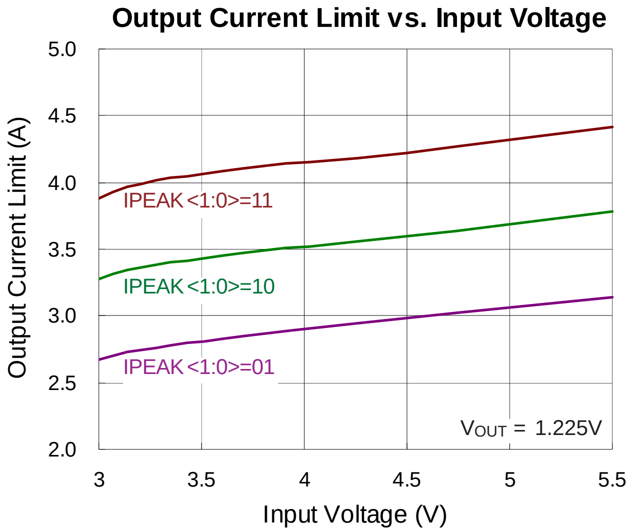


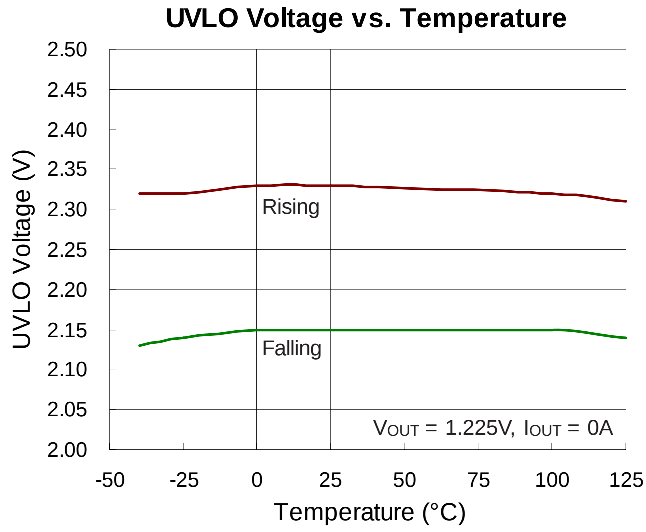
Frequency vs. Input Voltage

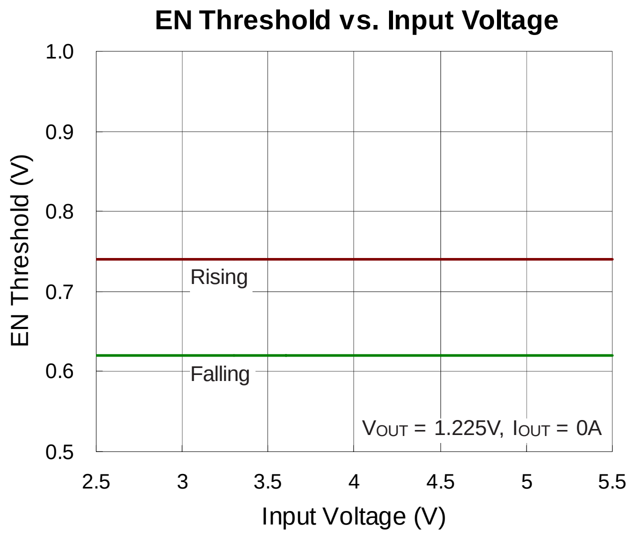


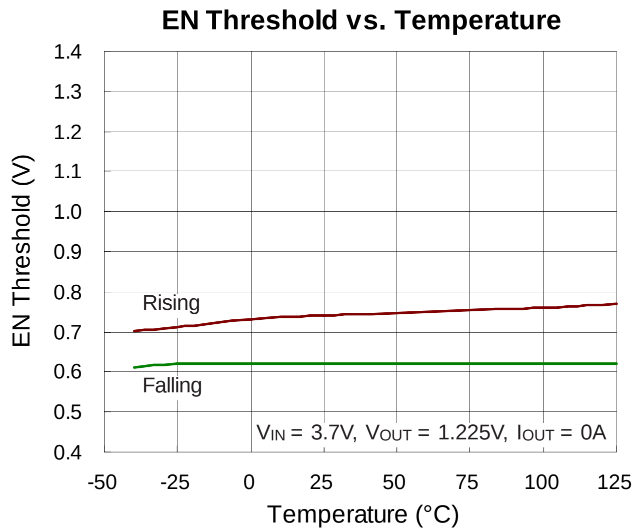
Frequency vs. Temperature

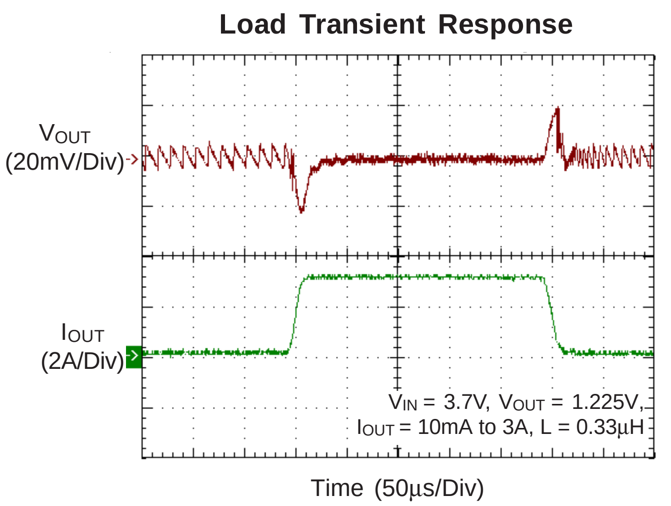


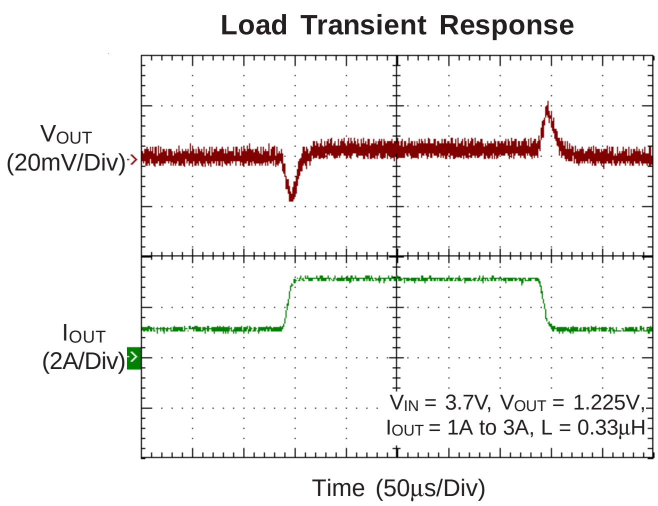

Output Current Limit vs. Input Voltage
Output Current Limit (A)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
IPEAK <1:0>=11
IPEAK <1:0>=10
IPEAK <1:0>=01
VOUT = 1.225V
3
3.5
4
4.5
5
5.5
Input Voltage (V)


UVLO Voltage vs. Temperature
UVLO Voltage (V)
2.50
2.45
2.40
2.35
2.30
2.25
2.20
2.15
2.10
2.05
2.00
Rising
Falling
VOUT = 1.225V, IOUT = 0A
-50
-25
0
25
50
75
100
125
Temperature (°C)

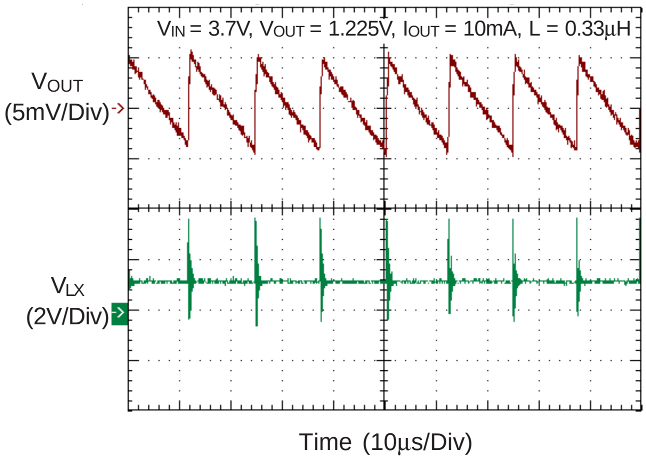

EN Threshold vs. Input Voltage
EN Threshold (V)
1.0
0.9
0.8
0.7
0.6
0.5
Rising
Falling
VOUT = 1.225V, IOUT = 0A
2.5
3
3.5
4
4.5
5
5.5
Input Voltage (V)


EN Threshold vs. Temperature
EN Threshold (V)
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
Rising
Falling
VIN = 3.7V, VOUT = 1.225V, IOUT = 0A
-50
-25
0
25
50
75
100
125
Temperature (°C)

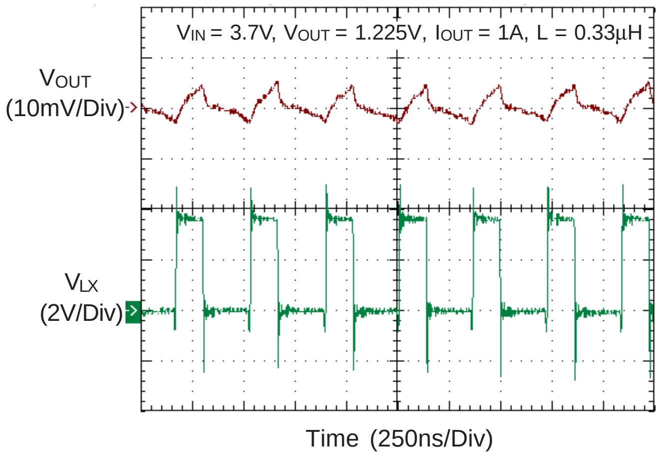

Load Transient Response
VOUT
(20mV/Div)
IOUT
(2A/Div)
VIN = 3.7V, VOUT = 1.225V,
IOUT = 10mA to 3A, L = 0.33µH
Time (50µs/Div)


Load Transient Response
VOUT
(20mV/Div)
IOUT
(2A/Div)
VIN = 3.7V, VOUT = 1.225V,
IOUT = 1A to 3A, L = 0.33µH
Time (50µs/Div)

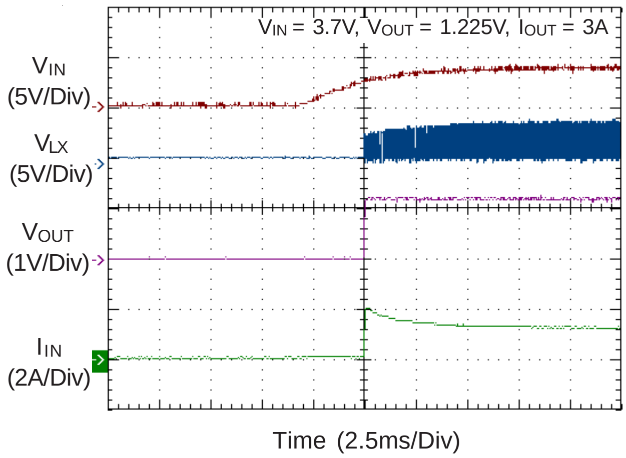
Output Ripple Voltage



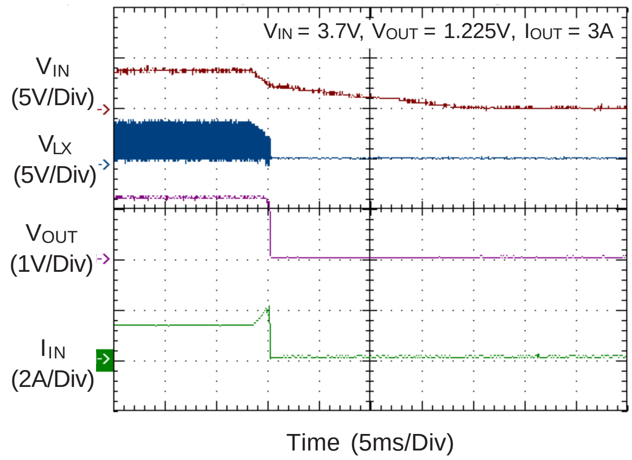
Output Ripple Voltage



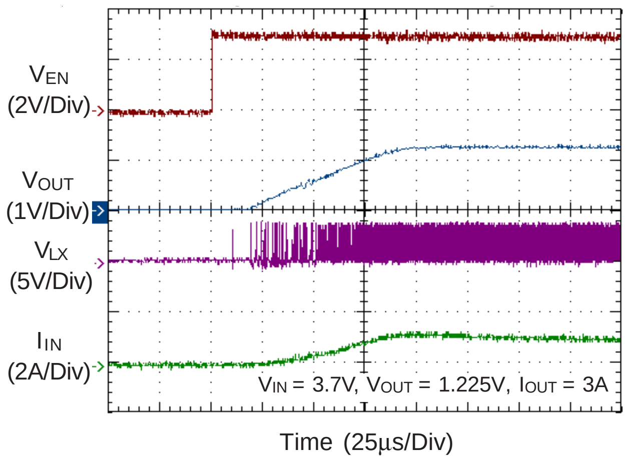
Power On from VIN



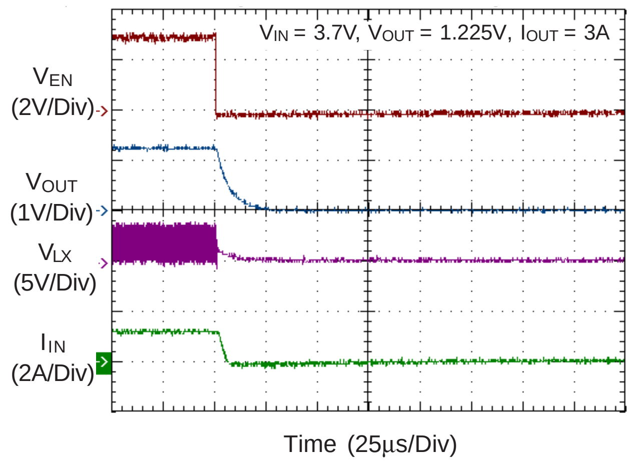
Power Off from VIN



Power On from EN



Power Off from EN



Application Information

The basic RT8088A application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current, ΔI_L, increases with higher V_{IN} and decreases with higher inductance, as shown in equation below :

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

where f is the operating frequency and L is the inductance. Having a lower ripple current reduces not only the ESR losses in the output capacitors, but also the output voltage ripple. Higher operating frequency combined with smaller ripple current is necessary to achieve high efficiency. Thus, a large inductor is required to attain this goal. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified $\Delta I_{L(MAX)}$, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (defined by a temperature rise from 25°C ambient to 40°C) should be greater than the maximum load current and its saturation current should be greater than the short-circuit peak current limit. Refer to Table 1 for the suggested inductor selection.

Table 1. Suggested Inductors for Typical Application Circuit

Component Supplier	Part Number	Dimensions (mm)
CYNTEC	PIFE20161B-R33MS-39	2.0 X 1.6 X 1.2

Input and Output Capacitor Selection

An input capacitor, C_{IN}, is needed to filter out the trapezoidal current at the source of the high-side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. Ceramic capacitors have high ripple current, high voltage rating and low ESR, which makes them ideal for switching regulator applications. However, they can also have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can lead to significant ringing. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. Thus, care must be taken to select a suitable input capacitor.

The selection of C_{OUT} is determined by the required ESR to minimize output voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output voltage ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \le \Delta I_L \left[ESR + \frac{1}{8 f_{OSC} C_{OUT}}\right]$$

where f_{OSC} is the switching frequency and ΔI_L is the inductor ripple current. The output voltage ripple will be the highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Ceramic capacitors have excellent low ESR characteristics, but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. Nevertheless, high value, low cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications.

I2C Interface Function

RT8088A can be used by I2C interface to select Vout voltage level, peak current limit level, thermal warning temperature level, PWM control mode, and so on. The register of each function can be found from the following register map and it also explains how to use these function.

I²C Interface

The RT8088A I²C slave address = 7'b0011100.

I²C Register Map

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
MONITOR	0x01	Meaning	SEN_TSD	SEN_TWARN	SEN_TPREW	RESV				SEN_PG
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
SEN_TSD			0 : Junction temperature below thermal shutdown (150°C) limit 1 : Junction temperature above thermal shutdown (150°C) limit							
SEN_TWARN			0 : Junction temperature below thermal shutdown (135°C) limit 1 : Junction temperature above thermal shutdown (135°C) limit							
SEN_TPREW			0 : Junction temperature below thermal shutdown (105°C) limit 1 : Junction temperature above thermal shutdown (105°C) limit							
RESV			Reserved bits							
SEN_PG			0 : DCDC output voltage below target 1 : DCDC output voltage within nominal range							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
PRODUCT_ID	0x03	Meaning	PRODUCT_ID							
		Default	0	0	0	1	0	1	0	1
		Read/Write	R	R	R	R	R	R	R	R
PRODUCT_ID			PRODUCT_ID							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
REVISION_ID	0x04	Meaning	REVISION_ID							
		Default	0	0	0	0	0	0	0	1
		Read/Write	R	R	R	R	R	R	R	R
REVISION_ID			REVISION_ID							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
FEATURE_ID	0x05	Meaning	FEATURE_ID							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
FEATURE_ID			FEATURE_ID							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
PROG	0x11	Meaning	EN	VOLT_SEL						
		Default	1	1	1	0	0	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
EN			0 : Disabled 1 : Enabled							
VOLT_SEL			VID Table satisfy : SEL [6:0] = 1111111 : V_{OUT} = 1393.75mV ... SEL [6:0] = 1100100 : V_{OUT} = 1.225V (default) ... SEL [6:0] = 0000000 : V_{OUT} = 0.6V 6.25mV step for DCDC, V_{OUT} = 600mV + 6.25mV x SEL							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
DISCHARGE	0x12	Meaning	RESV			DISCHG	RESV			
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R/W	R	R	R	R
RESV			Reserved bits							
DISCHG			0 : discharge path disabled 1 : discharge path enabled							
RESV			Reserved bits							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
COMMAND	0x14	Meaning	PWM	RESV	DVSMODE	RESV				
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R	R/W	R	R	R	R	R
PWM			0 : Auto 1 : Forced PWM							
RESV			Reserved bits							
DVSMODE			0 : Auto DVS transition mode 1 : Forced PWM DVS transition							
RESV			Reserved bits							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
LIMCONF	0x16	Meaning	IPEK <1:0>		TPWTH <1:0>		RESV			
		Default	1	1	1	0	0	0	1	1
		Read/Write	R/W	R/W	R/W	R/W	R	R	R	R

IPEAK <1:0>	00 : 2.9A 01 : 2.9A 10 : 3.4A 11 : 3.9A
TPWTH <1:0>	00 : 83°C 01 : 94°C 10 : 105°C 11 : 116°C
RESV	Reserved bits

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WL-CSP-15B 1.31x2.11 (BSC) package, the thermal resistance, θ_{JA}, is 49.8°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (49.8°C/W) = 2W for WL-CSP-15B 1.31x2.11 (BSC) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

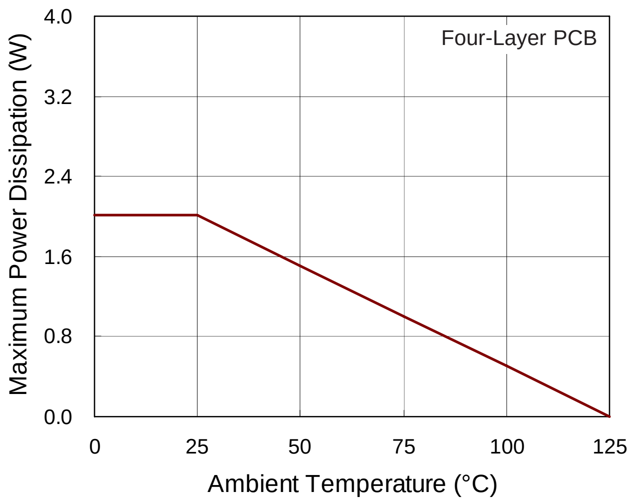
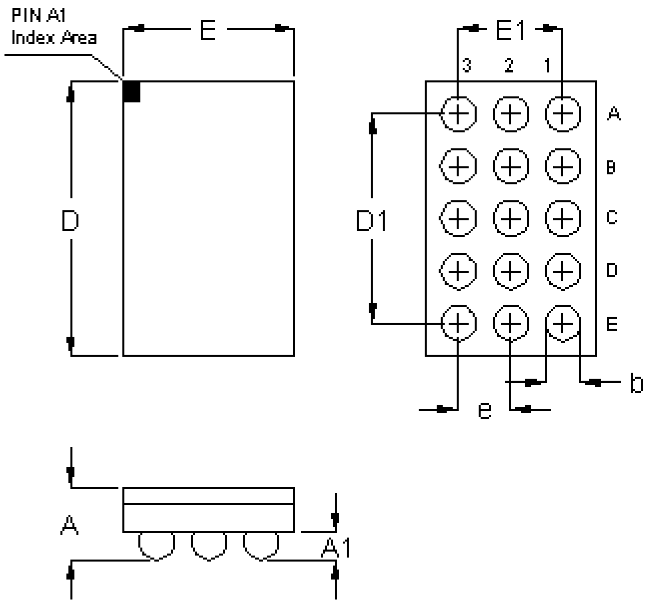


Figure 1. Derating Curve of Maximum Power Dissipation

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.060	2.160	0.081	0.085
D1	1.600		0.063	
E	1.260	1.360	0.050	0.054
E1	0.800		0.031	
e	0.400		0.016	

15B WL-CSP 1.31x2.11 Package (BSC)

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