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tech tips

Performing the Chipper Check Hardware Diagnostic Tests

The Chipper Check software contains a diagnostic section which can completely test the internal circuitry of the Chipper Check interface box. It may also be used to fully check the serial cable and chassis adapters. It also contains selections to help in troubleshooting the hardware circuitry. This document shows you how to setup and perform several of the diagnostic tests to check the internal circuitry of the Chipper Check interface box.

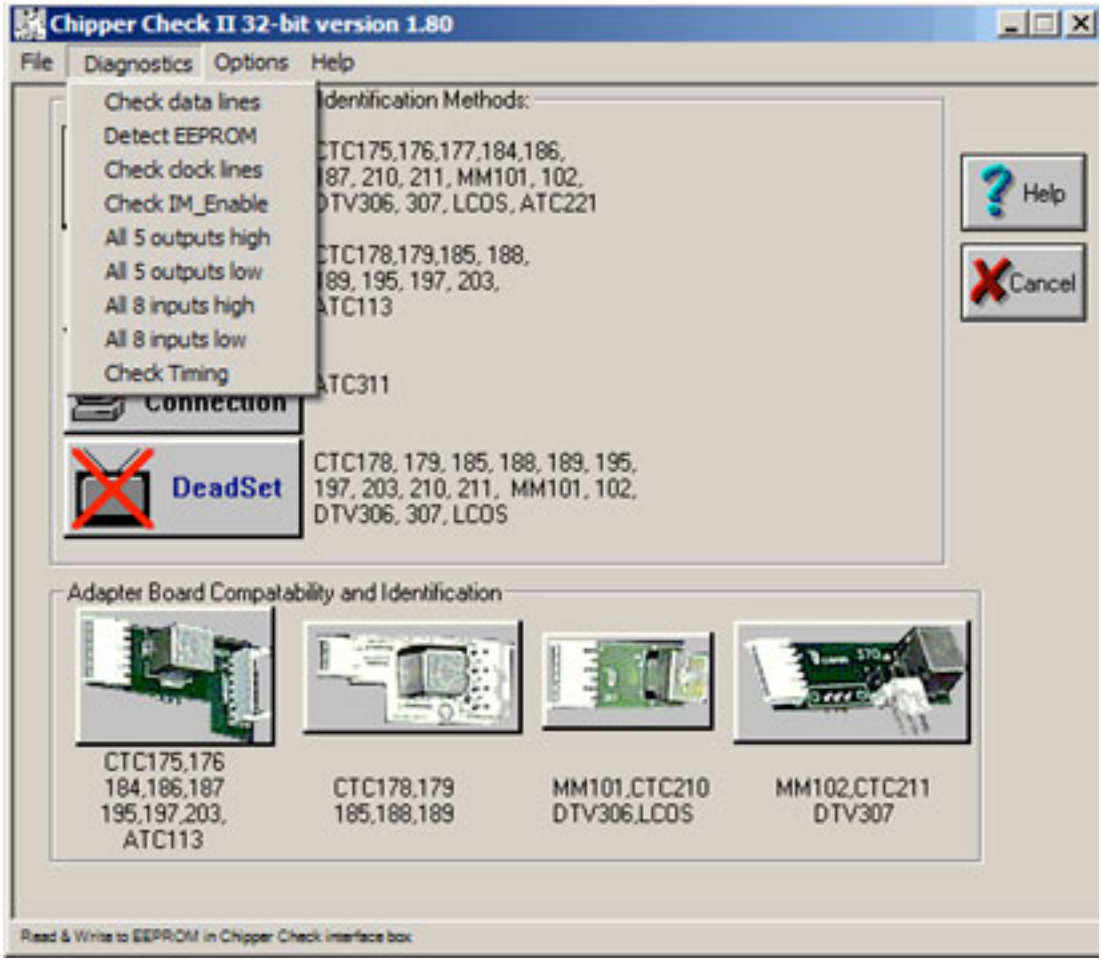


Figure 1. The "Diagnostic" selection in the Chipper Check main screen provides tests that check the hardware circuitry in the Chipper Check interface box.

Use the following tests listed in the Diagnostic section to test the Chipper Check hardware. Perform the Detect EEPROM test last.

Check data lines
Check clock lines
Check IM Enable
Detect EEPROM

These tests check every input/output signal path, enable path and the EEPROM within the Chipper Check interface box. If a test fails you have a problem with the hardware circuitry or power supply within Chipper Check that must be corrected. If all tests are "Good" the Chipper Check circuitry is OK. You may want to extend the tests to include the serial cable and adapter to confirm these components are free from defects.

Setup for Checking Chipper Check Circuitry

The Diagnostic Tests require that the Chipper Check software be loaded and operational on a computer. Start the Chipper Check software by selecting the Chipper Check icon. Click on the "Diagnostic" selection on the start screen within the top menu bar. In earlier versions of Chipper Check software, the Diagnostic tests were selected within the "Help" selection in the top menu bar.

To perform the Diagnostic tests connect the parallel cable between the computer and the Chipper Check interface box. Connect the Power Adapter to an AC outlet and connect the DCV input connector to the Chipper Check box. Confirm that the LED on the Chipper Check box is illuminated. Remove the serial cable from the output of the Chipper Check box as shown in figure 2. The test procedures in this document have you test the Chipper Check circuitry within the interface box.

the computer. A change in the read line returned to the computer indicates a good data signal path loop. Since there are two data signal read/write lines, the check data line test has two steps or parts.

When the Data Line Test is first selected the Data Line test reminds you to be not connected to a TV chassis, because the Data line outputs at pin 4 or 1 may be shorted causing the test to fail. Click on YES to continue.

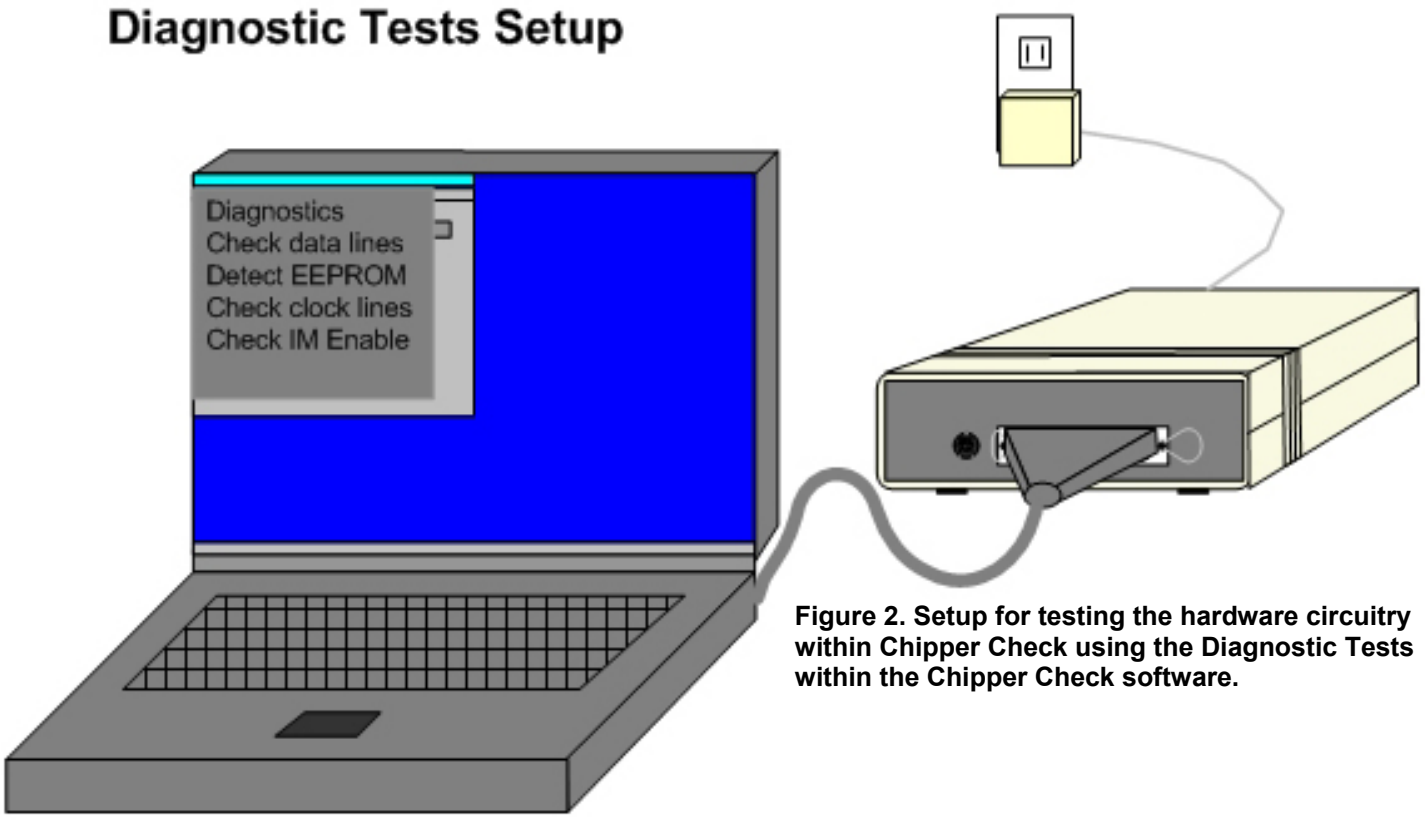


Figure 2. Setup for testing the hardware circuitry within Chipper Check using the Diagnostic Tests within the Chipper Check software.

Check Data Line Test (Part 1)

The first diagnostic test checks the data lines. There are two data signal paths that move data through to the output connector of the chipper check hardware and to the EEPROMs. These data signals are “Data Run” and “Data STBY.” Data Run is output on pin 4 and Data STBY to pin 1 on the output connector. From these same output pins separate Data STBY and Data Run paths return signals back to the computer. These return data signal paths are “Data Run Read” and “Data STBY Read.”

These write/read data signal lines permit a closed loop test of the Data STBY read/write signal paths and Data Run read/write signal paths. The data line test routine changes the state of the write line or input, enables the write line to move data to the output and back through the return or read path to

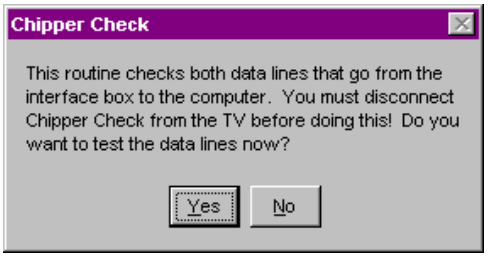


Figure 3. Information screen which appears upon selecting the Check data line test.

Before performing the Data Line Tests the routine asks if the Chipper Check hardware has been updated with the KIT 2 circuitry or add on board. Kit 2 adds a small circuit board with wires containing an EEPROM and control circuits. These circuits add an enable line to Chipper Check that enables the Data STBY write line separate from the Data Run write line. Chipper Check hardware without the addition of Kit 2 use the Write Enable input from the computer to

enable both Data STBY and Data Run write lines. Chipper Check with KIT 2 added use a Data STBY enable line to enable the Data STBY write line. Click YES if the Chipper Checker contains the extra circuitry. The circuitry changes the routine used by Chipper Check to test the two data line. If you have added the KIT 2 circuitry but select NO you will incorrectly get a "Data line Test Failed" message.

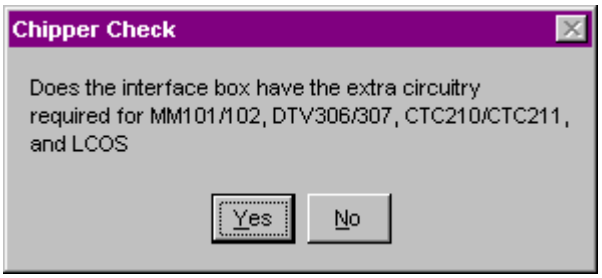


Figure 4. The Check data line test asks if the added circuitry contained in KIT 2 has been installed. Select YES if the circuits have been installed.

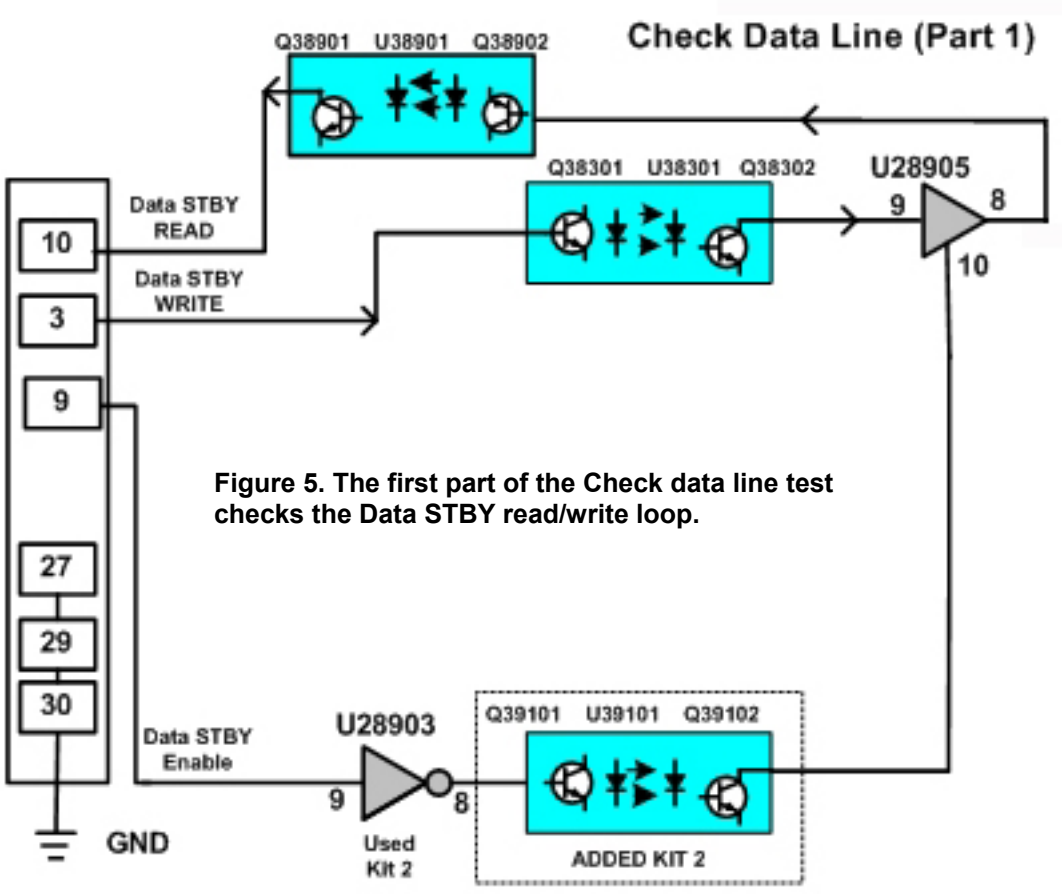


Figure 5. The first part of the Check data line test checks the Data STBY read/write loop.

The first part of the check data line test checks the Data STBY read/write loop. This circuitry is shown in figure 5. A failed test would end with a readout message "Data line test failed! Data line coming from pin 10 of the 36 pin connector was high when it should have been low." This failed test message indicates a defect with the Data STBY circuitry loop. Common causes include a power supply defect or improper installation of KIT 1 or KIT 2.

Check Data Line Test (Part 2)

Upon the conclusion of the first part of the Data line test (Data STBY read/write), the test continues with a test of the Data RUN read/write loop. If both Data line tests are good, the test concludes with a good data lines message.

The message reads "Data line tests were successful, no errors were detected." This message indicates the data write/read signal paths shown in figures 5 and 6 within Chipper Check (including the associated signal paths of the computer parallel port and cable) are all good.

A failure of the second part of the data line test would end with a readout message "Data line test failed! Data line coming from pin 13 of the 36 pin connector was high when it should have been low." This failed test message indicates a defect with the Data Run loop or associated signal paths within the parallel port or cable connecting the computer to the Chipper Check interface box.

Check Clock Line Test (Part 1)

The Check clock line test checks the Clock Run and Clock STBY signal paths and their respective enable circuits in the Chipper Check interface box. Since there are two clock lines there are two parts to the test. The first part of this test checks the Clock STB Y line. The setup for this test is the same as performing the Check data lines as shown in figure 7. A second part of this test checks the Clock Run signal path.

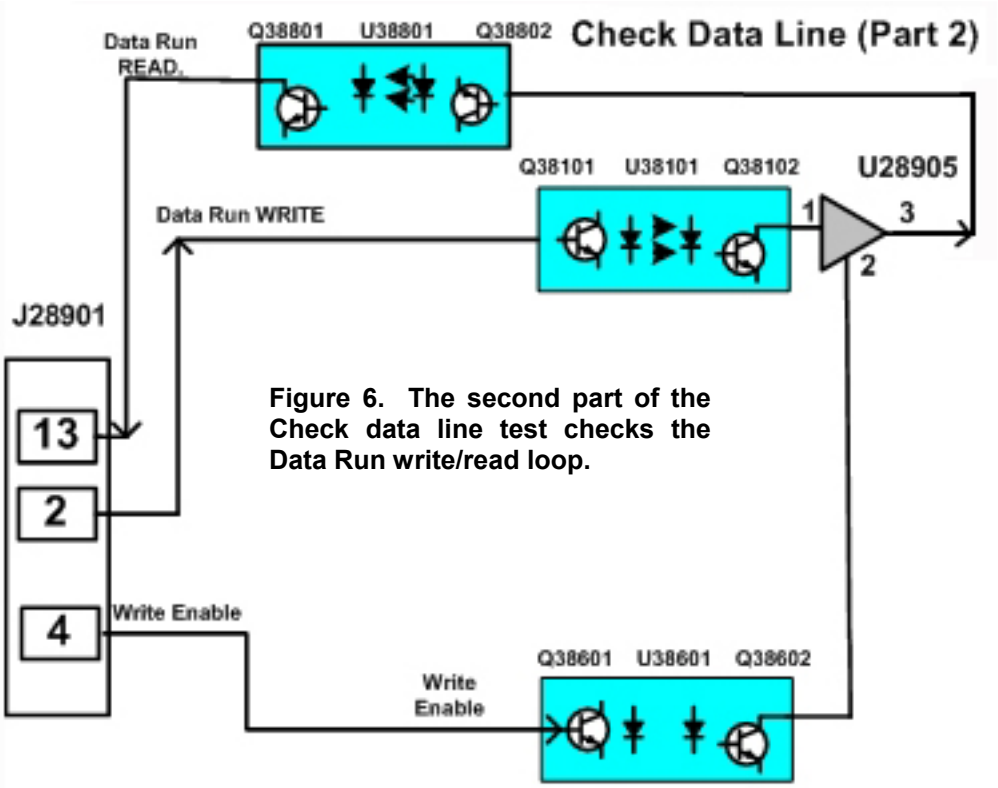


Figure 6. The second part of the Check data line test checks the Data Run write/read loop.

To perform the Check clock line tests requires a return path to the computer. A return path to the computer is created by placing a jumper across the output connector as shown in figure 7 or at the end of a chassis adapter, such as the #212121 adapter. The jumper connects the Clock Run or Clock STBY output to a data write line back to the computer. The created closed loop enables the computer to change the logic state of the input clock line and observe an expected change on a data write line returned to the computer.

The first part of the Check clock line test checks the Clock STBY line. A wire jumper wire must be installed between pins 1 and 2 of the output connector jack on the Chipper Check interface box or across pins 1 and 2 of the #212121 adapter. Use a solid wire of the proper size to properly insert into the output connector for a good electrical connection. Be sure to insert with caution as to not damage the receptacle connections.

With the jumper wire in place, the diagnostic test changes the logic state of the Clock STBY input line to the Chipper Check interface box and looks for the logic state of the Data STBY read line returned to the computer to change logic states. The Clock Enable line is activated to permit the logic state change to occur at the output Clock STBY output.

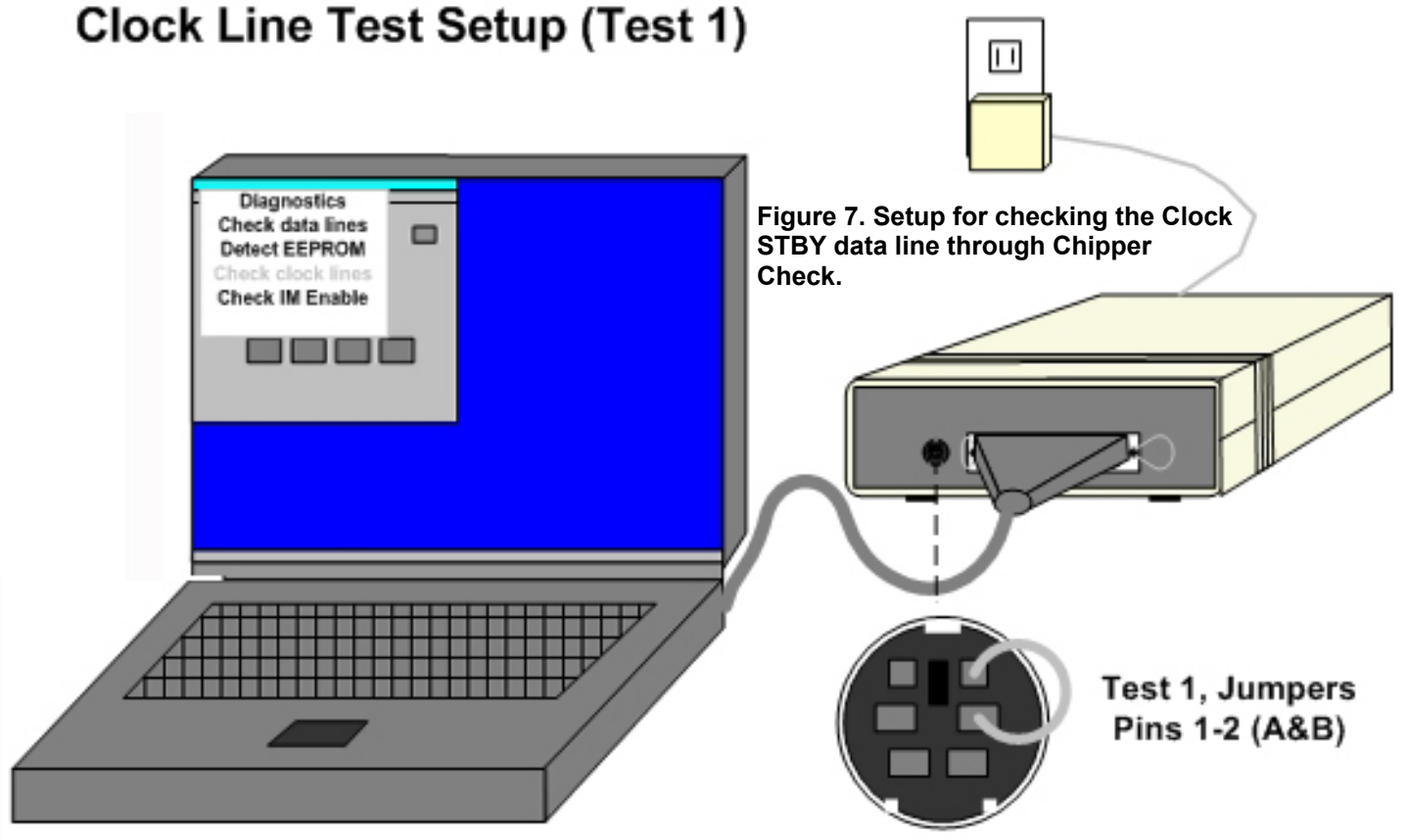


Figure 7. Setup for checking the Clock STBY data line through Chipper Check.

When the Check clock line test is selected within the Diagnostic menu on the Chipper Check software, an initial informative screen appears as shown in figure 8. The message indicates that the test is dependent on properly connecting jumpers across the output connector for a valid test. It also reminds you to disconnect from a TV chassis as to not short out the Clock STBY output pin. Click on the YES when you have properly connected the jumper wire and removed connection from a TV chassis.

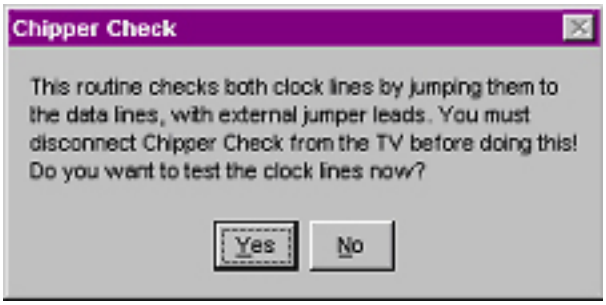


Figure 8. Opening informational box for the Check clock line diagnostic tests.

Before performing the Check clock line test you must connect the Clock STBY output on pin 2 to the Data STBY Write line on pin 1. If you do not properly connect pins 2 and 1 you will incorrectly get a "Clock line Test Failed" message. It is recommended that first you jumper pins 1 and 2 on the output pin of the Chipper Check box to diagnose internal hardware

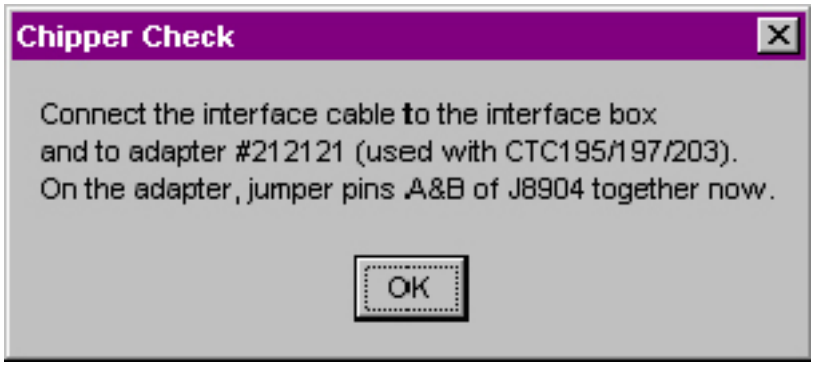


Figure 9. Informational box concerning jumpering Clock STBY line to Data STBY read line for proper testing of the Clock STBY data line.

Clock line circuit failures. You may test the serial cable and adapter by shorting the Clock STBY output to the Data STBY line at the adapter to diagnose cable and adapter defects.

A defective Clock STBY line or Clock enable line in the Chipper Check Interface box result in a failed test message. The message indicates "Clock line test failed. Pin 10 of the 36 pin connector was high when it should have been low. Pin 10 is the Data STBY read line return to the computer. A failed test ends the Check clock line tests and does not permit the 2nd part of the test. A good test simply increments you to the second part of the Check clock line tests.

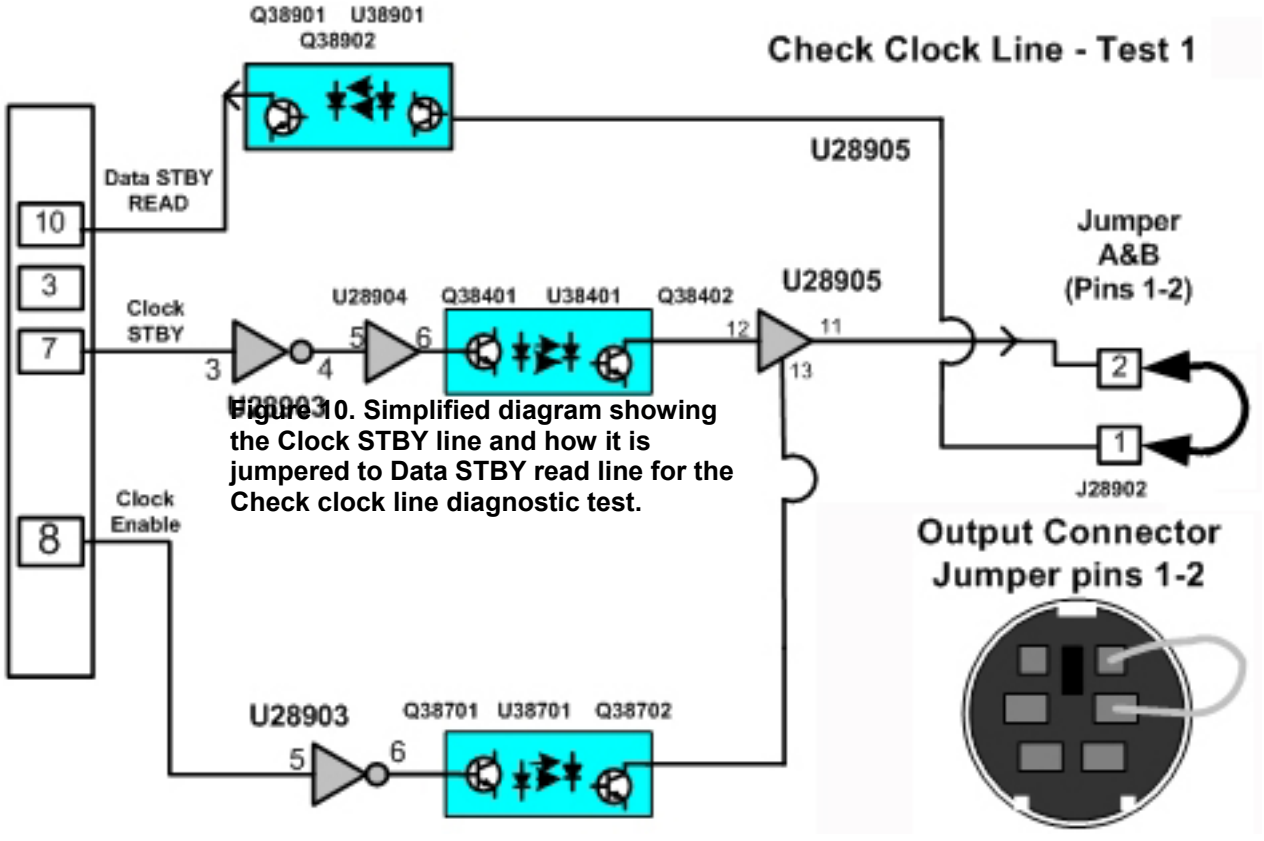


Figure 10. Simplified diagram showing the Clock STBY line and how it is jumpered to Data STBY read line for the Check clock line diagnostic test.

Check Clock Line Test (Part 2)

Upon a successful test of the Clock STBY line the second part of the Check clock line tests are initiated. The second part of the Clock line tests checks the Clock Run signal path in the Chipper Check Hardware. The same setup is used as shown in figure 11. The Clock Run is output from the Chipper Check Interface box on pin 5 of the output connector. When the Clock Run is connected to pin 4 of the output connector, a closed loop path is created back to the computer through the Data Run Read path. This closed loop enables the computer to perform a diagnostic check of the Clock Run and associated Clock Enable circuitry.

A defective Clock Run line in the Chipper Check Interface box results in a failed test message. The message indicates "Clock line test failed. Pin 13 of the 36 pin connector was high when it should have been low. Pin 13 is the Data STBY read line return to the computer. A defect in the Clock Run circuits shown in figure 12 must be isolated and corrected to restore proper clock line operation.

A successful test of both clock lines is indicated with a "Check clock line tests successful." You may test the serial cable and adapter by shorting the Clock STBY output to the Data STBY line at the adapter to diagnose cable and adapter defects.

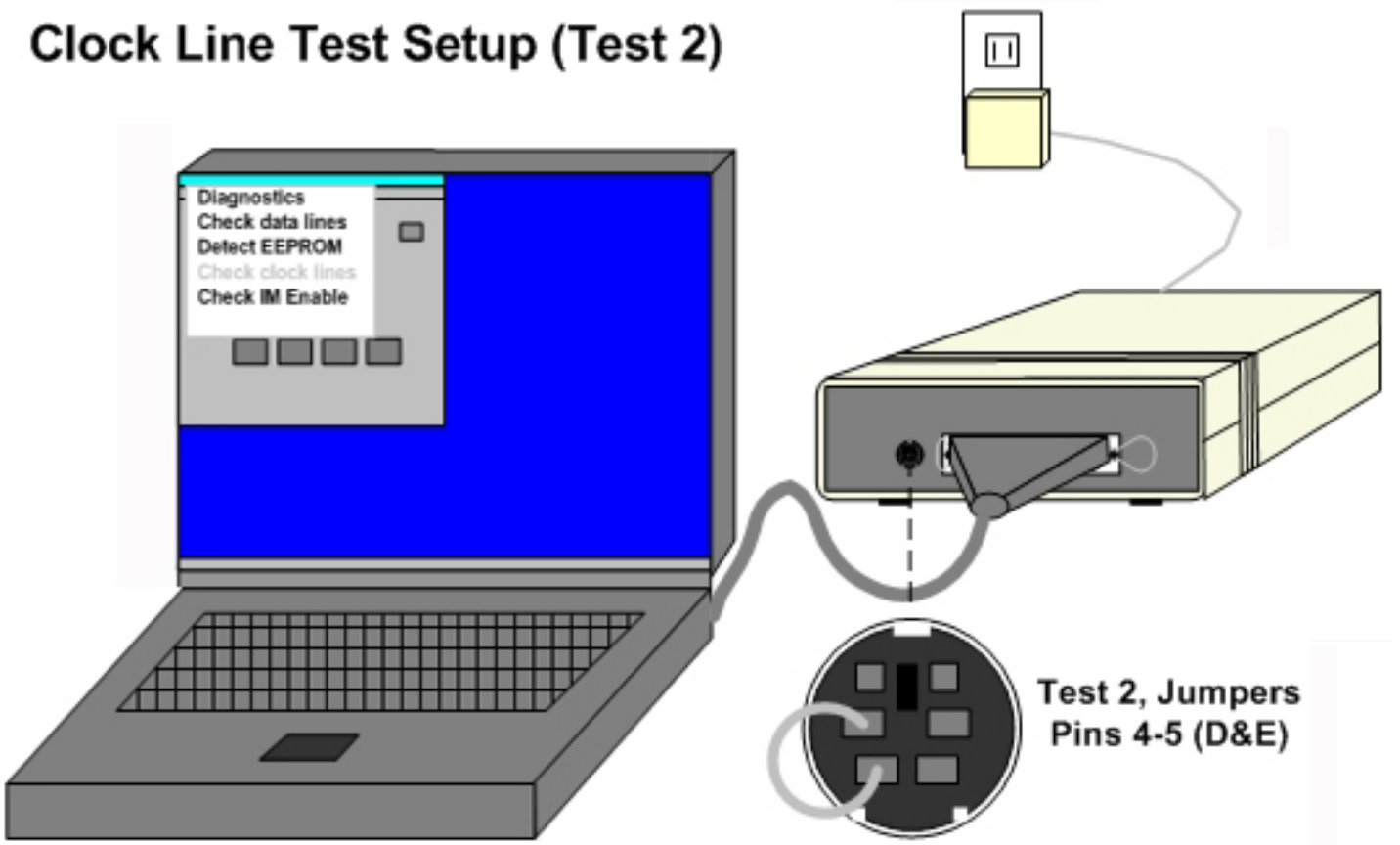


Figure 11. Setup for the 2nd part of the check clock line test. Jumper pins 4 and 5 as shown.

Remove the jumper wire from pins 1 & 2 and install between pins 4 & 5 as shown in figure 11. Remove and insert the jumper wire carefully as to not damage the receptacle. Press OK to proceed.

Check IM Enable Test

This diagnostic test checks the IM Enable line circuitry in the Chipper Check interface box. There is only one part to this test. The setup for performing the IM Enable test is shown in figure 13. The IM Enable test connects the IM enable line to the Data Run Read line returned to the computer enabling a closed circuit loop.

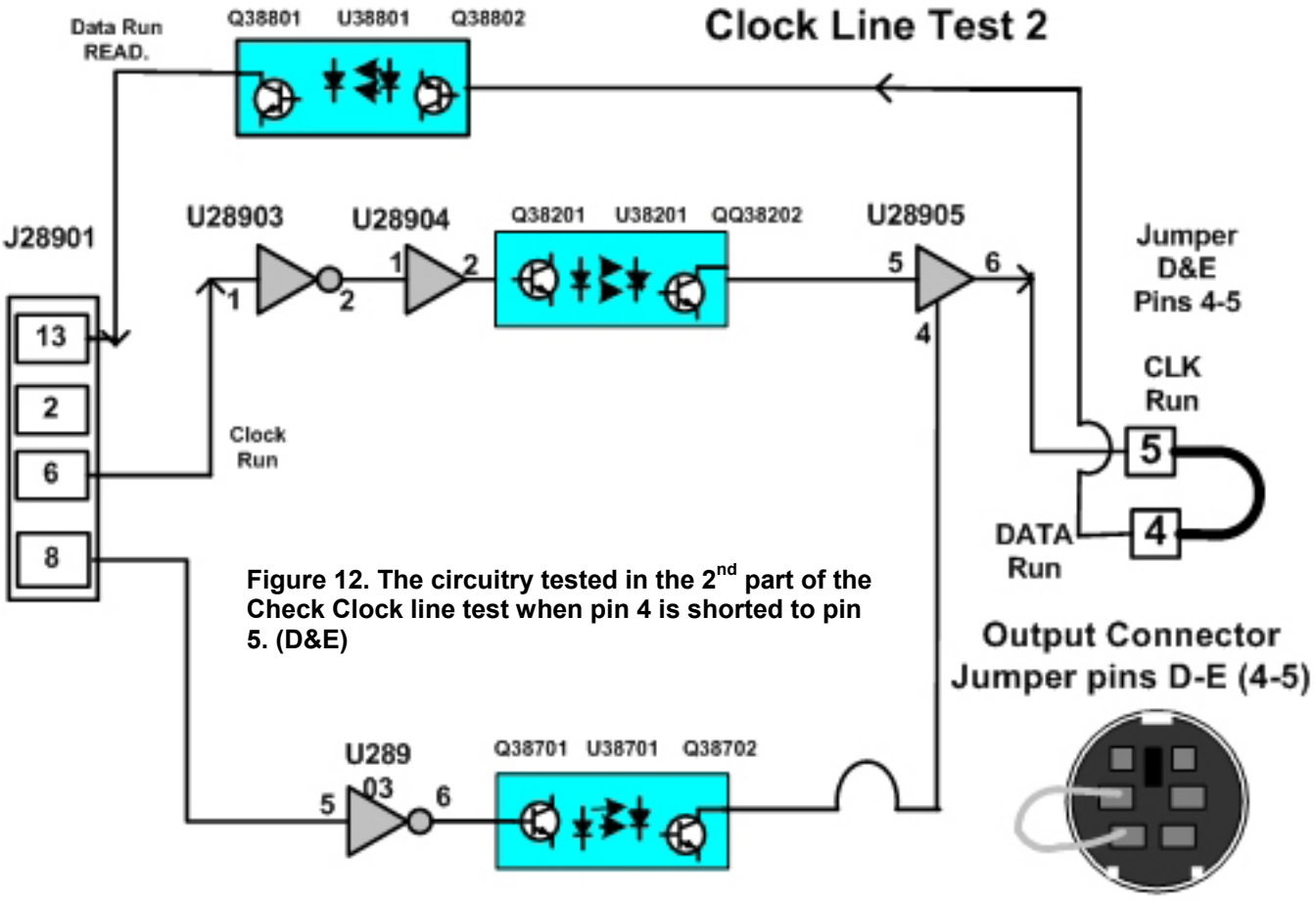


Figure 12. The circuitry tested in the 2nd part of the Check Clock line test when pin 4 is shorted to pin 5. (D&E)

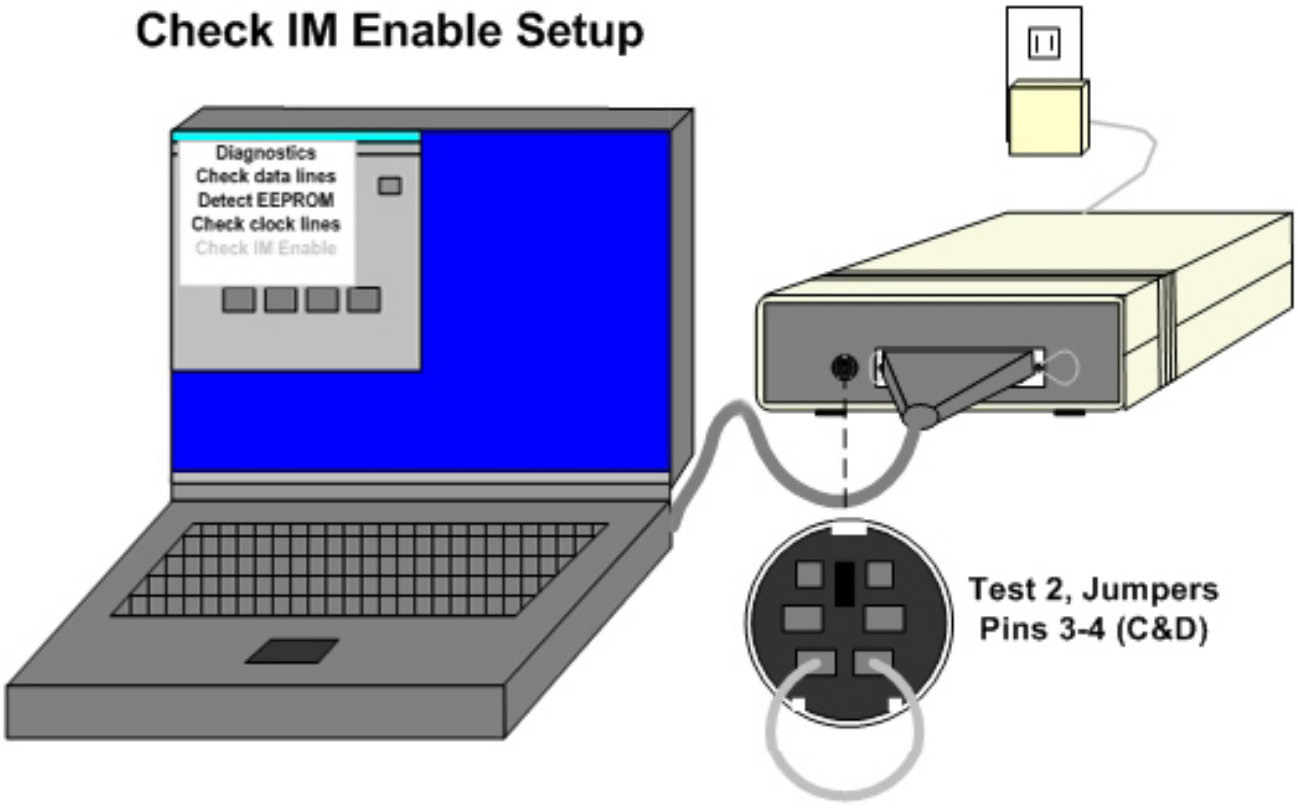


Figure 13. Setup for performing the IM Enable Test. Jumper pins 3 and 4 as shown.

The initial information box indicates that as in the other diagnostic tests you must remove the adapter from a TV chassis to avoid shorting out the IM enable line on pin 4 of the Chipper Check output connector and on adapter #212121. Select YES when you have removed these connections.

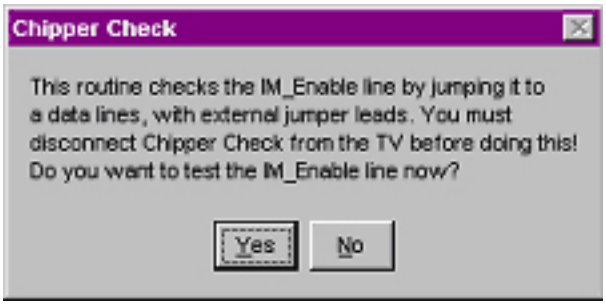


Figure 14. Introduction to IM Enable Test.

A failed test is indicated by a message "IM Enable test failed. Pin 13 of the 36 pin connector was high when it should have been low." This message indicates a defect in the IM Enable line of the Chipper Check interface box. You may want to repeat the test making sure you have correctly installed the jumper between pins 3 and 4. A defect in the IM Enable line must be corrected to restore normal operation to the Chipper Check.

A good working IM Enable line results in a message indicating the IM Enable line tests was successful. This message indicates no defects with the IM Enable circuit path in the Chipper Check interface box. You may repeat the IM Enable test connecting the jumper across the chassis adapter connector's IM Enable (pin3) to Data Run (pin 4) to test the serial cable and chassis adapter.

The next informational box informs you to jumper the IM Enable output on pin 3 to the Data Run read line on pin 4 before performing the test. Failure to connect the jumper will incorrectly result in an IM Enable test failure. Select YES when you have installed the jumper. It is recommended to jump pins 3 and 4 in the output connector of the Chipper Check interface box to test the hardware circuitry. You may short pins 3 & 4 in adapter #212121 to diagnose IM Enable path in the serial cable and adapter. Use caution when inserting the jumper wire to avoid connector damage.

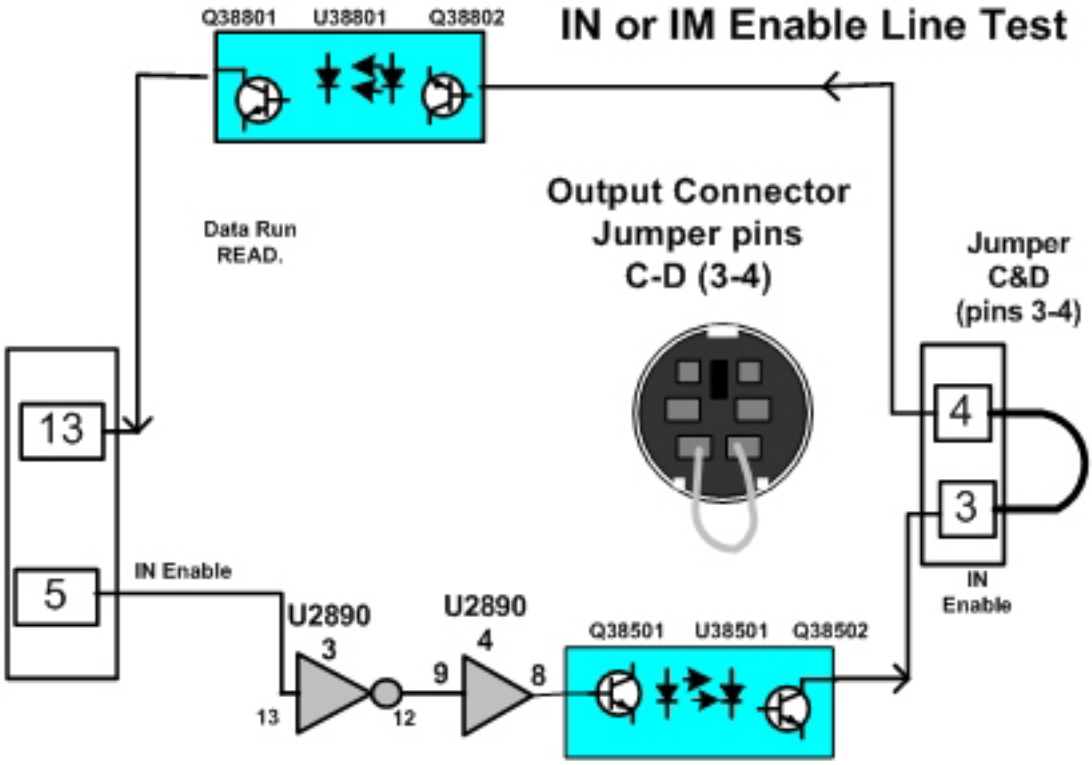


Figure 16. Internal circuit paths of the Chipper Check interface box tested with the IM Enable diagnostic test.

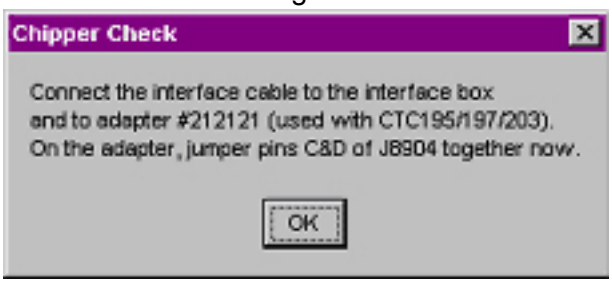


Figure 15. Informational box advising connection of pins 3 to pin 4 (C&D).

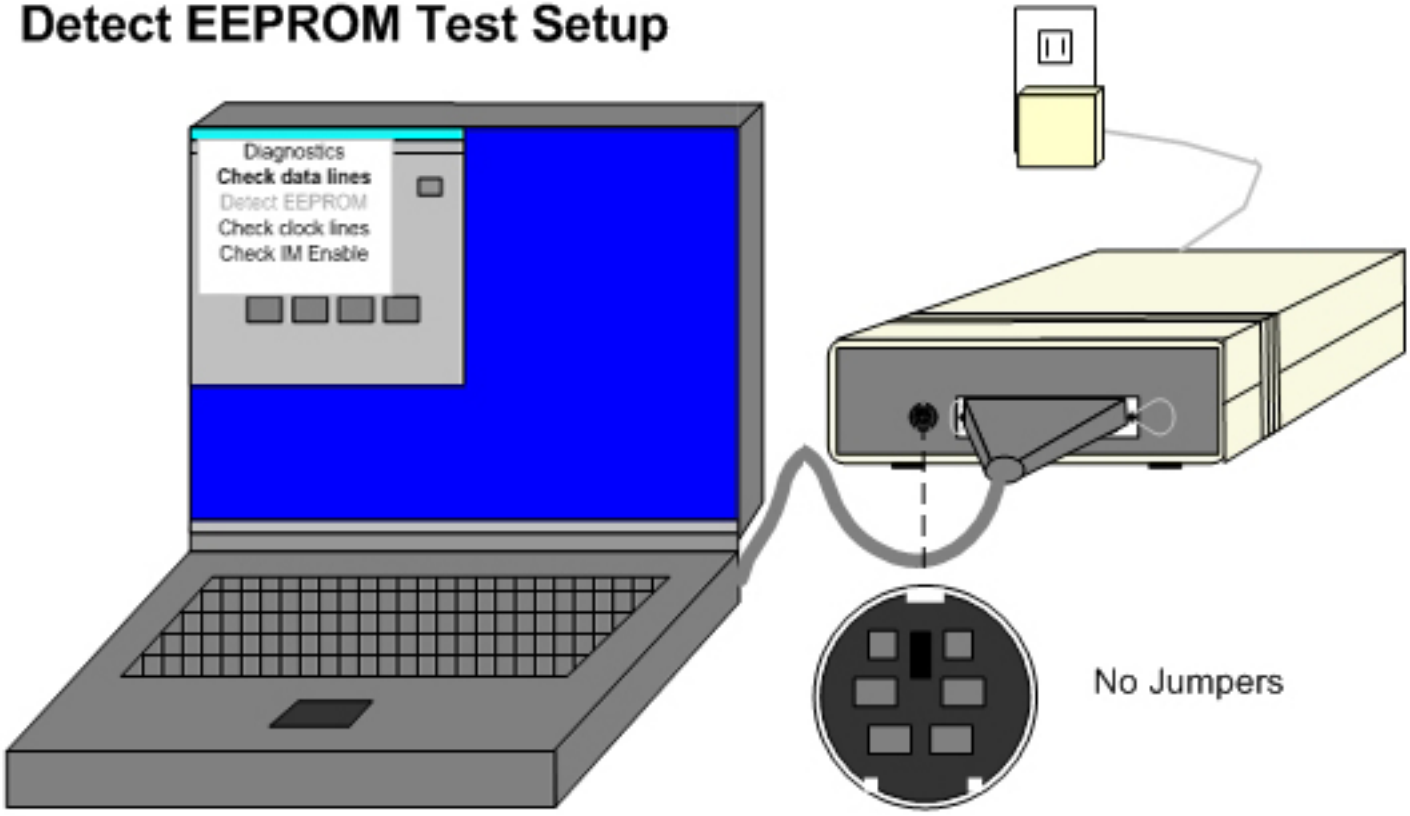


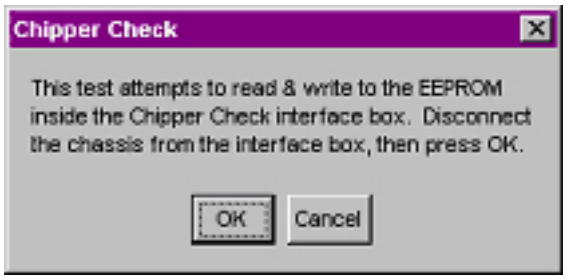
Figure 17. Setup for performing the Detect EEPROM test. NO jumpers are required.

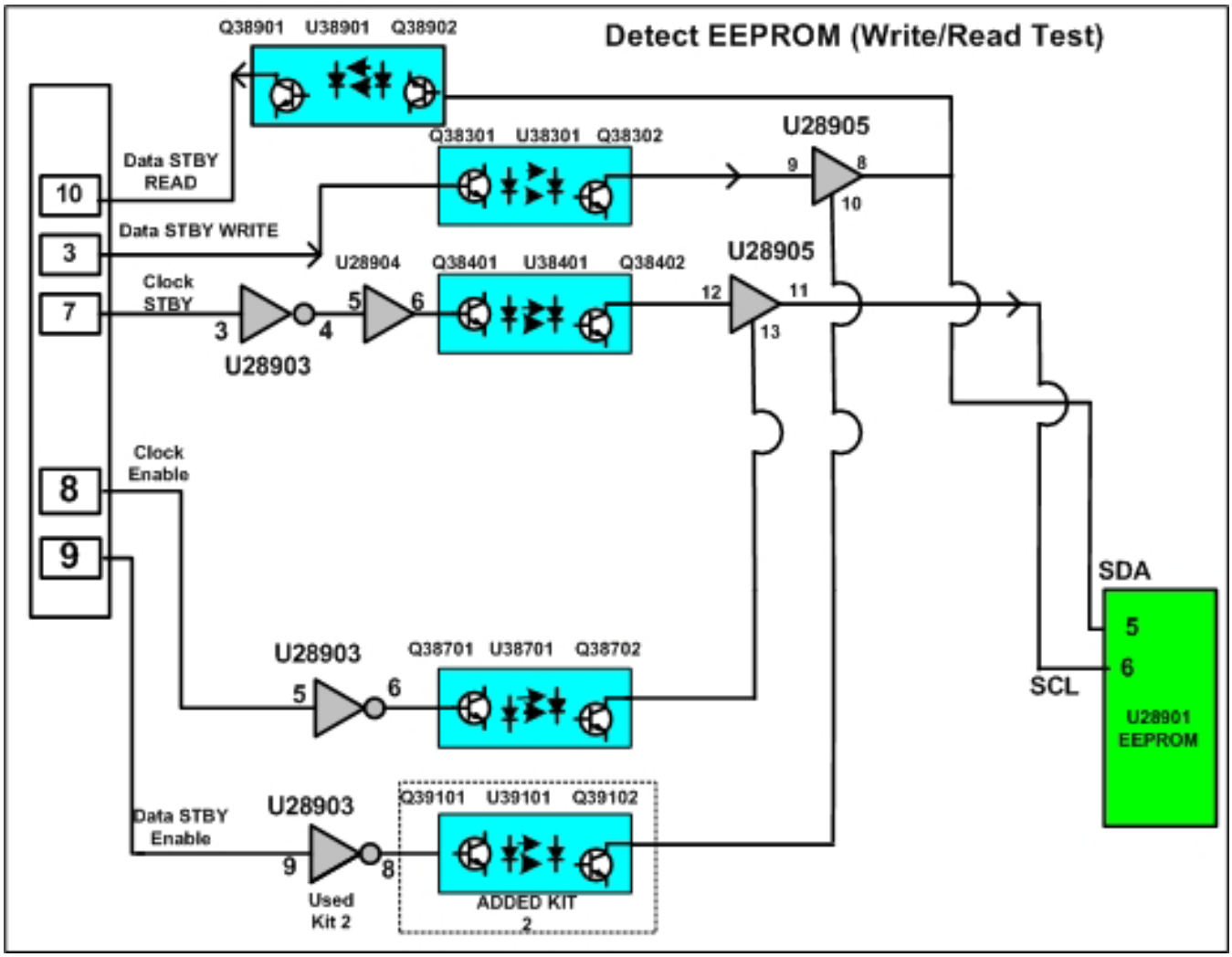
Detect EEPROM Test

The Detect EEPROM diagnostic test checks the EEPROM contained in the Chipper Check. The test clocks data through the DATA STBY Write line to the EEPROM. Then data is clocked out of the EEPROM through the Data STBY Read line back to the computer. The write/read process uses the clock, data, and enable lines contained in the Chipper Check interface box. These lines have all been tested with the Data line and Clock line and IM diagnostic tests. The Detect EEPROM test uses these lines to read and write to the EEPROM in the Chipper Check. Use the same setup as the other diagnostic tests as shown in figure 17.

Upon selecting the Detect EEPROM test an information box advises to disconnect the interface box from a TV chassis. Be sure any adapter is disconnected from the TV chassis and/or no jumper wires are left in the output connector of the Chipper Check interface box from previous diagnostic tests. Press OK to proceed.

An "EEPROM communications was successful" message indicates that the computer is able to read and write data to the EEPROM within the Chipper Check interface box. A problem message indicating "A communication error occurred" indicates a defect with the EEPROM or SCL or SDA lines to the EEPROM.





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