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tech tips

Troubleshooting Chipper Check Data, Clock and Enable Signal Lines

If you suspect the Chipper Check interface box is not working properly, use the built-in Diagnostic tests provided by the Chipper Check software. For more information on the diagnostic tests and how to diagnose Chipper Check hardware see the document titled “Testing the Chipper Check Hardware - Diagnostic Tests.” The Diagnostic tests confirm if a problem exists in the Chipper Check interface box.

Use the Diagnostic tests to determine which of the data, clock, enable lines and EEPROM do not work. If all diagnostic tests fail, test the power supplies within Chipper Check. See the document titled “Chipper Check Power Supply Troubleshooting.” If any of the Diagnostic tests pass, the Chipper Check power supply is likely good and you should refer to the Chipper Check simplified block diagram to determine what circuits to troubleshoot.

Troubleshooting Methods

There are two methods you can use to isolate defects in the Chipper Check data, clock or enable signal lines. First you can use several features within the Diagnostic tests in the Chipper Check software. The tests that can help you troubleshoot, include:

All 5 outputs high
All 5 outputs low
All inputs high
All inputs low

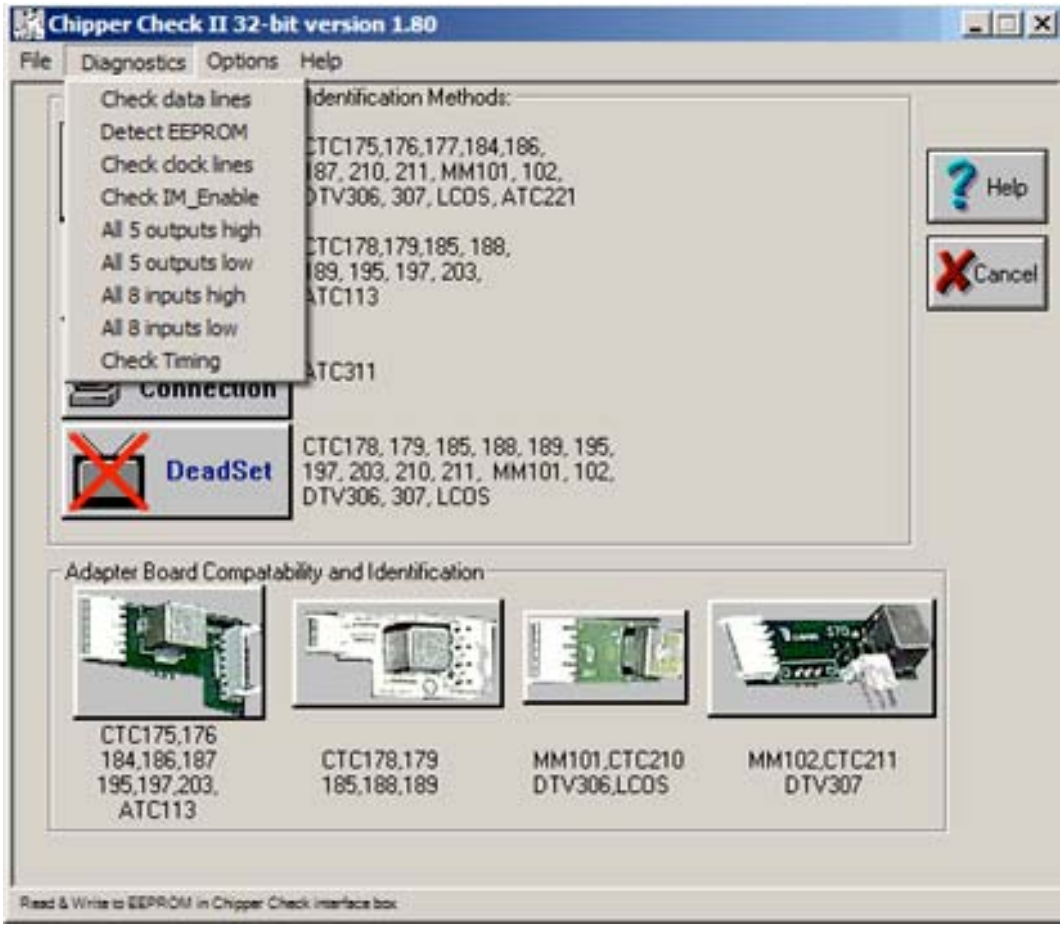


Figure 1. Use the Diagnostic software tests “All 5 outputs high (low)” to troubleshoot the Chipper Check interface box with DCV measurements.

The “All 5 outputs high/low” diagnostic tests apply the proper input logic state from the computer to cause the clock, data, and IM enable output pins on the output connector of the Chipper Check interface box to go to a high logic state (approx. 5V) or a low logic state (near 0V). The output lines can be measured with a voltmeter in respect to S ground located on pin 6. You may then take voltage measurements at key circuit points along the suspect data, clock or enable line to isolate the suspect circuitry and component. A helpful hint would be to toggle the diagnostic test between “All 5 outputs high” and “All 5 outputs low” and look for a logic voltage change at key circuit points.

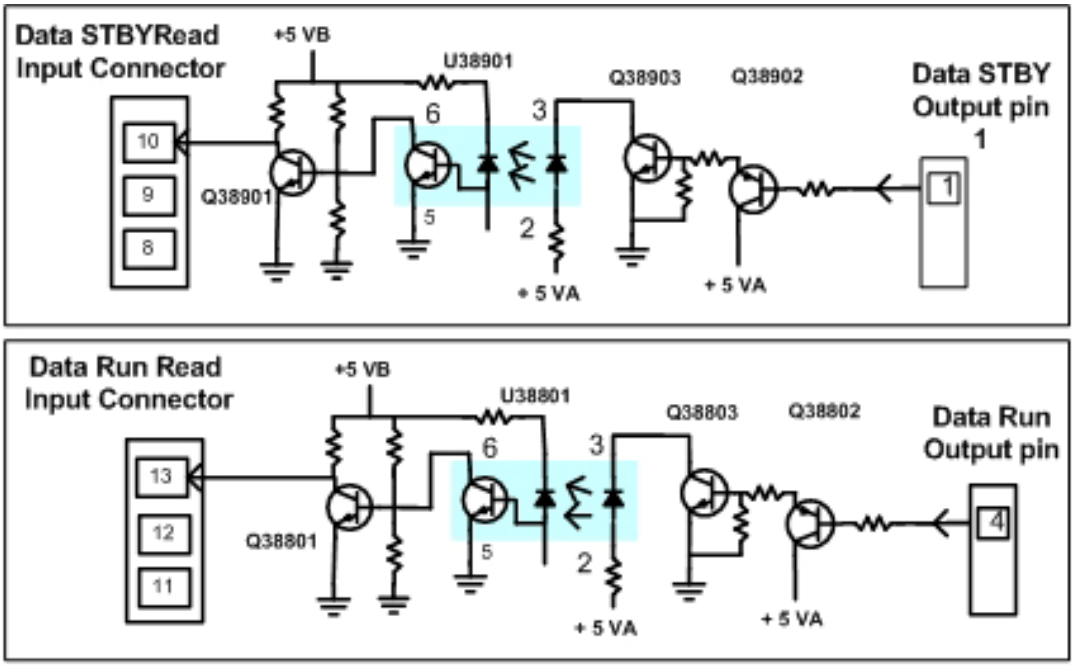


Figure 2. A Data STBY Read line returns data from chassis to computer. The circuitry in the Data Run line is identical.

A second method involves using a signal generator to input a logic waveform to a data, clock or IM enable signal path while providing the proper logic level to its respective enable line. You may then utilize an oscilloscope to trace along the signal path to isolate a defect.

Understanding Data, Clock, IM Enable and Enable Lines

Data STBY and Data Run

The Data STBY and Data Run read lines return data from the chassis to the computer. A high output voltage at pin 1 causes Q38902 to turn on and bias on Q38903. Current in the light sensitive side of the opto-coupler pulls down the voltage at the base of Q38901 to about 0.1 volts. With Q38901 biased off, the collector pulls to near 5 volts. The Data Run line works the same.

Data STBY and Data Write

The Data Run Write and Data STBY Write lines move data from the computer to the chassis and Chipper Check EEPROM. A Data Run Write input at pin 3 of over 3 volts turns on Q38101 producing light in the opto-coupler. The receive transistor conducts pulling the base of Q38102 near 0.1 volts. With Q38102 off, the collector pulls to near 5 volts. When pin 1 of the tri-state buffer IC, U28905 is high the logic high of the

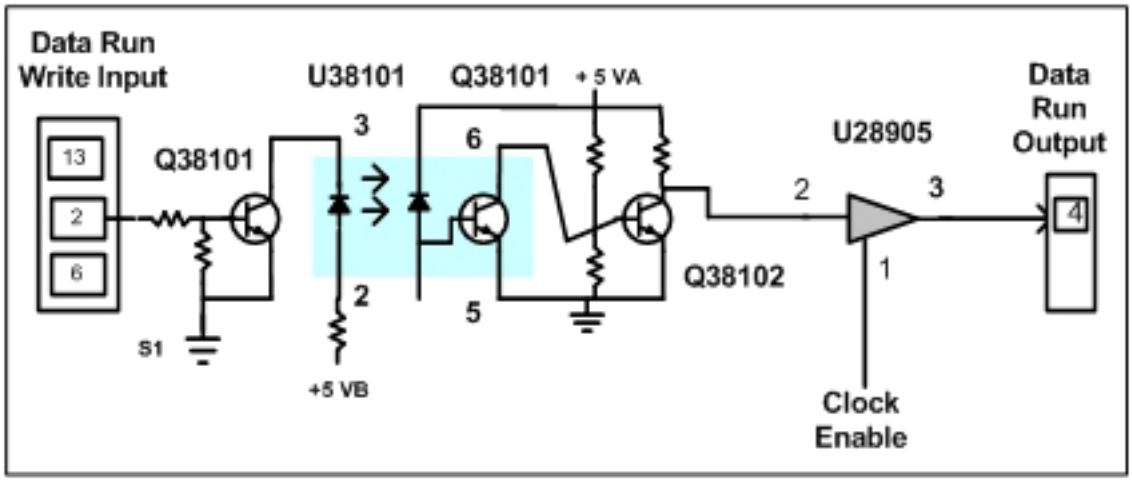


Figure 3.The Data Run Write line which moves data from the computer to the chassis. The Data STBY Write line is identical.

input at pin 2 is coupled to the output at pin 3.
The Data STBY Write line is identical.

Clock Run and Clock STBY

The Clock Run line and Clock STBY lines move clock signals from the computer to the chassis and EEPROMs. A high input to pin 1 of U28903 is inverted to a low on its output pin 2. U28904 inverter changes the voltage back to a high on its output pin 2. Transistor Q38201 turns on producing transmitted light in the opto-coupler. The base of Q38202 is pulled low turning it off and pulling the collector and output at pin 5 to a logic high near 5 volts. The Clock STBY line is identical.

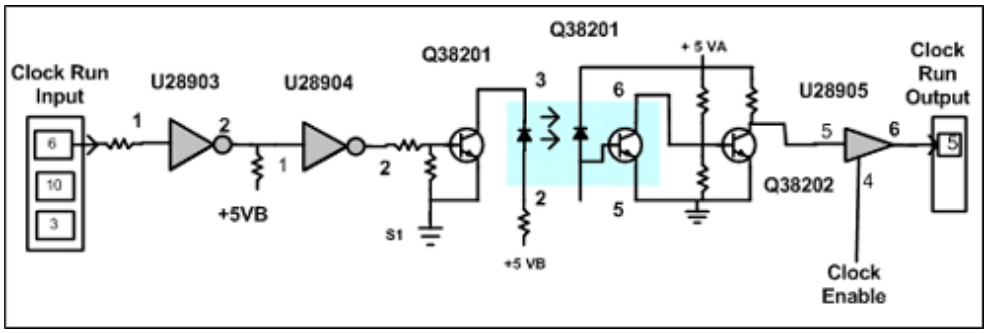


Figure 4. The Clock Run and Clock STBY lines move clock signals from the computer to the chassis and EEPROMs.

IN or IM Enable

The IM Enable line is used by the computer to communicate with the chassis. The circuit operation is identical to the operation describe for the Clock lines without the tri-state buffer circuit.

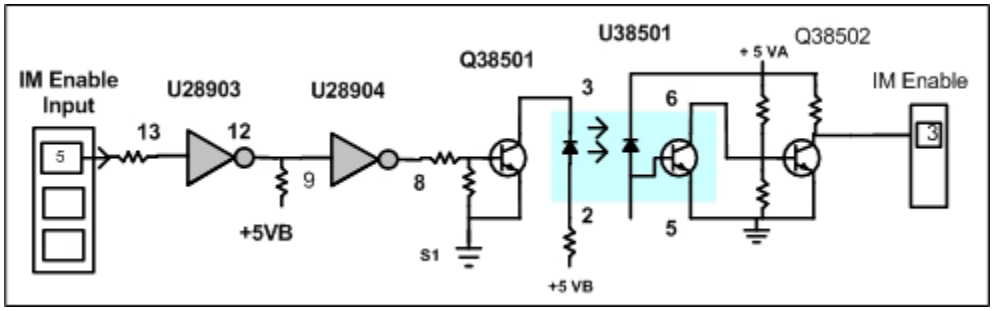
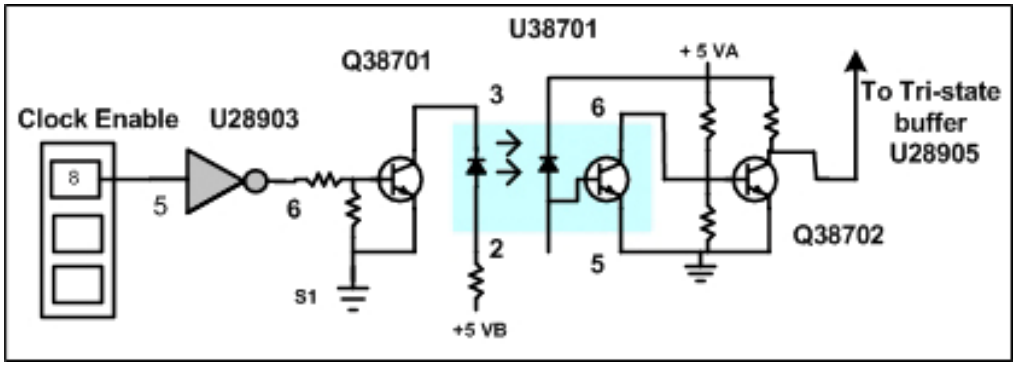


Figure 5. The IM Enable line is used by the computer to communicate with the chassis.

Data Run, Data STBY, Clock Enable

The Chipper Check interface box has Data Run, Data STBY and clock enable lines. These circuits control the tri-state buffer IC, U28905. The tri-state buffer operates like an open or closed gate. With a high to the control input the clock or data signals pass through. With a low to the control input, the gate is closed and output circuit is a high impedance.

Figure 6. Example of Enable Lines (Clock Enable)



Troubleshooting Data and Data Enable Circuits

If the Chipper Check Diagnostic tests “Check Data Line Test” indicates a failure, a defect exists in one of the two data write/read signal loops. A defect in part 1 of the Check Data Line Tests indicates a defect in the Data STBY write/read loop including the Data STBY Enable line. A failure in the second part of the Check Data Line tests indicates a defect in the Data Run write/read loop including the Write Enable line. The Data Run write/read circuits are shown in figure 7. The Data STBY circuits function the same.

You can trouble shoot the Data Run or Data STBY circuit loops by referring to the key test points and voltage reference charts shown in figure 7. Figure 7 lists the key test points and respective DCV measurements with the Chipper Check software Diagnostic test “All 5 outputs high.” This test applies the proper logic states to the input of the Chipper Check interface box to make all the outputs high (5V).

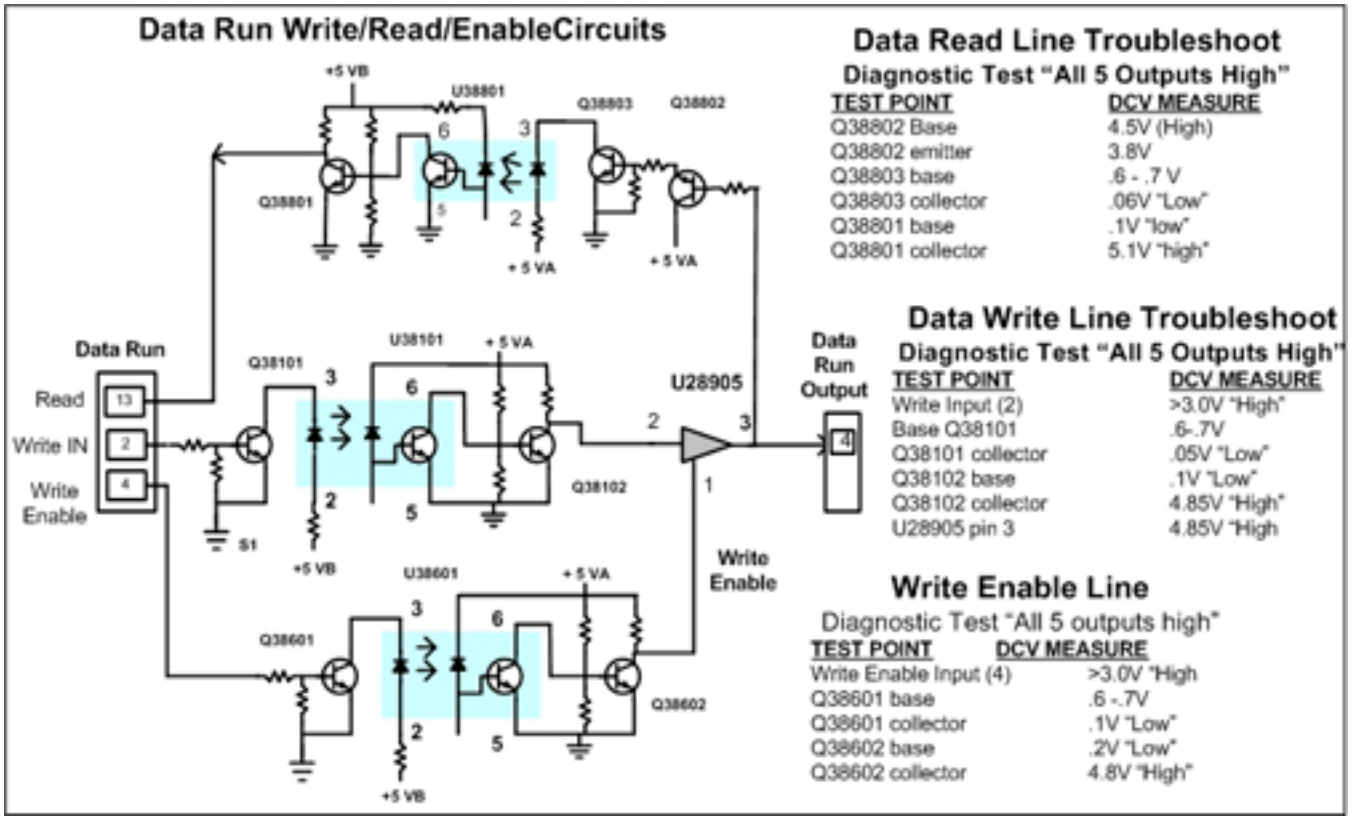
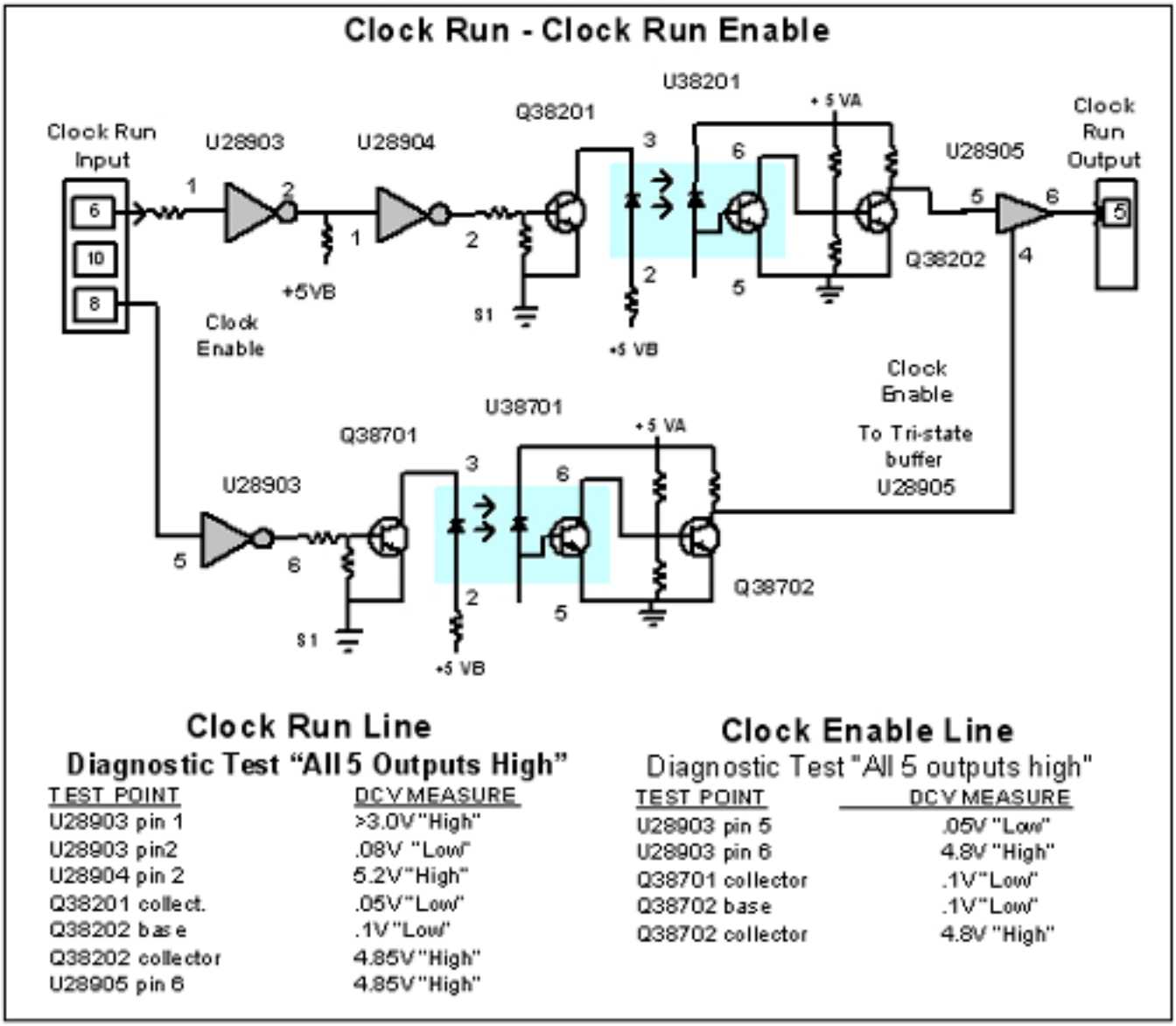


Figure 7. Data and Data Enable key test point reference voltage measurements.

Troubleshooting Clock and Clock Enable Circuits

If the Chipper Check Diagnostic tests show Check Data Line tests are successful but the Check clock line tests indicate a failure, a Clock line or its respective enable line is likely bad. A failure on the first part of the Check clock line test indicates a problem with the Clock STBY line. A failure in the second part of the Check clock line test indicates a problem with the Clock Run line.

You can troubleshoot the Clock Run or Clock STBY lines and their respective Enable lines by referring to figure 8. Figure 8 lists the key test points and respective DCV measurements with the Chipper Check software Diagnostic test "All 5 outputs high." This test applies the proper logic states to the input of the Chipper Check interface box to make all the outputs high (5V).



Clock Run Line
Diagnostic Test "All 5 Outputs High"

TEST POINT	DCV MEASURE
U28903 pin 1	>3.0V "High"
U28903 pin2	.08V "Low"
U28904 pin 2	5.2V "High"
Q38201 collect.	.05V "Low"
Q38202 base	.1V "Low"
Q38202 collector	4.85V "High"
U28905 pin 6	4.85V "High"

Clock Enable Line
Diagnostic Test "All 5 outputs high"

TEST POINT	DCV MEASURE
U28903 pin 5	.05V "Low"
U28903 pin 6	4.8V "High"
Q38701 collector	.1V "Low"
Q38702 base	.1V "Low"
Q38702 collector	4.8V "High"

Figure 8. Clock and Clock Enable key test point reference voltage measurements.

Troubleshooting IM Enable Circuits

If the Chipper Check software diagnostic test indicates a failure when performing the “Check IM Enable” test, a defect is likely in the IM Enable line. You can trouble shoot the IM Enable line by referring to the key test points and voltages shown in figure 9. Figure 9 shows voltages at key circuit points with the Chipper Check software Diagnostic test “All 5 outputs high.” This test applies the proper logic states to the input of the Chipper Check interface box to make the IM Enable output high (5V).

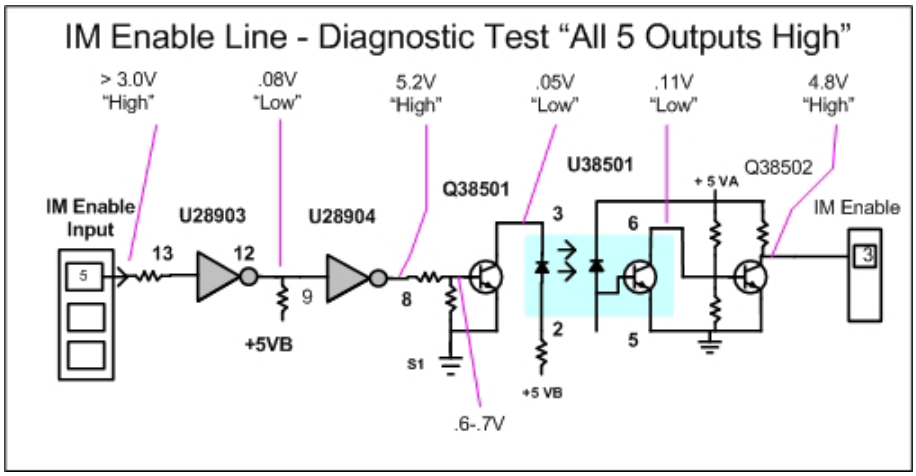


Figure 9. IM Enable key test point reference voltage measurements.

Troubleshooting With a Square-ware Generator & Oscilloscope

The combination of a square-wave signal generator and oscilloscope can provide a second option for troubleshooting data, clock or IM enable signal paths within Chipper Check.

Connect a square-wave generator to the input of the suspect data, clock or IM Enable pin of the 36 pin input connector. Connect the square-generator ground to the S1 (input) ground. The generator must produce a voltage change from 0 to approximately 5VDC. This requires a generator with a DC offset to raise the low transition to approximately 0 VDC.

The square-wave passes through the circuit lines to the output of the Chipper Checker. Use the oscilloscope to signal trace the square-wave through the circuit path to isolate the defect. The circuit that does not permit the square-wave to pass indicates a defect. Remember to change oscilloscope grounds as you probe on the input side of the opto-coupler (S1 ground) to the output side (S ground).

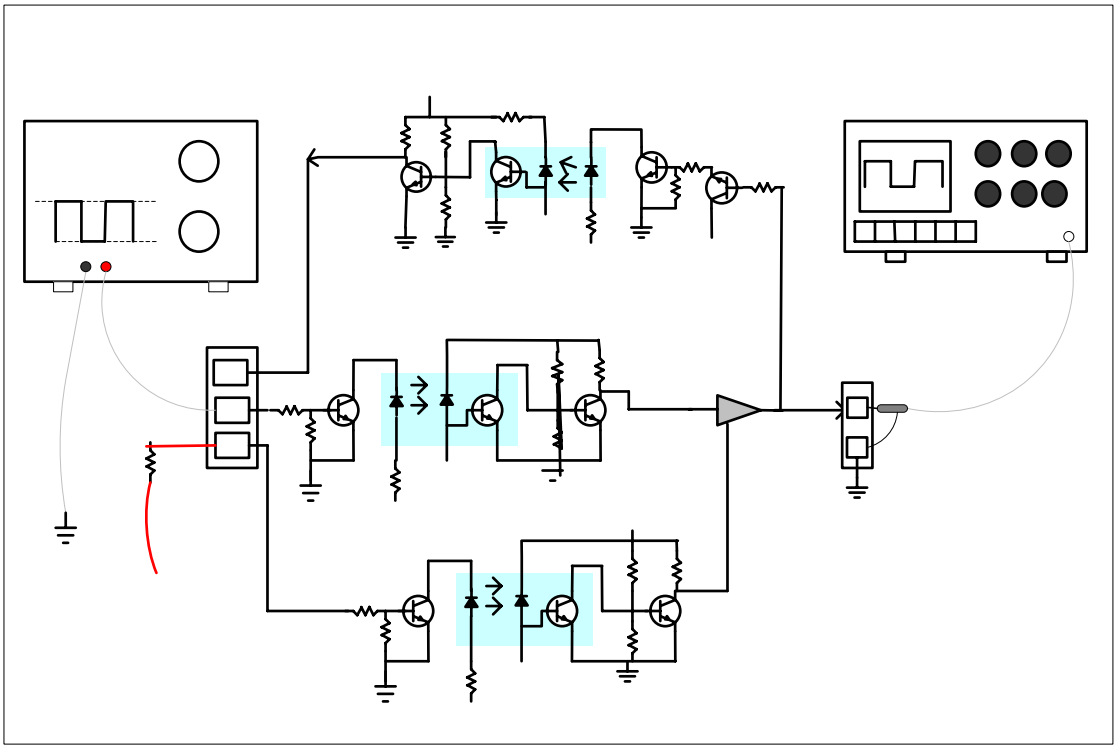


Figure 10. Trace the square wave though the data write path to output pin 4 and then back through the Data read path to pin 13 of the input connector.

You must apply the proper logic state, high or low, to the input pins of the write enable, data enable or clock enable inputs. Improper operation of the enable circuits can cause a low voltage to the tri-state buffer IC (U28905) which blocks the square-wave from passing through to the output.

To troubleshoot the Data Run write/read loop, place a 1 K ohm resistor from pin 4 of the 36 pin input connector (Write Enable) to + 5VB. This pulls the Write Enable input high which causes the Write Enable line to place a high to pin 1 of the tri-state buffer IC U28905. This permits the square-wave signal to pass through to the output pin 4. Use the same procedure when trouble-shooting the Data STBY line.

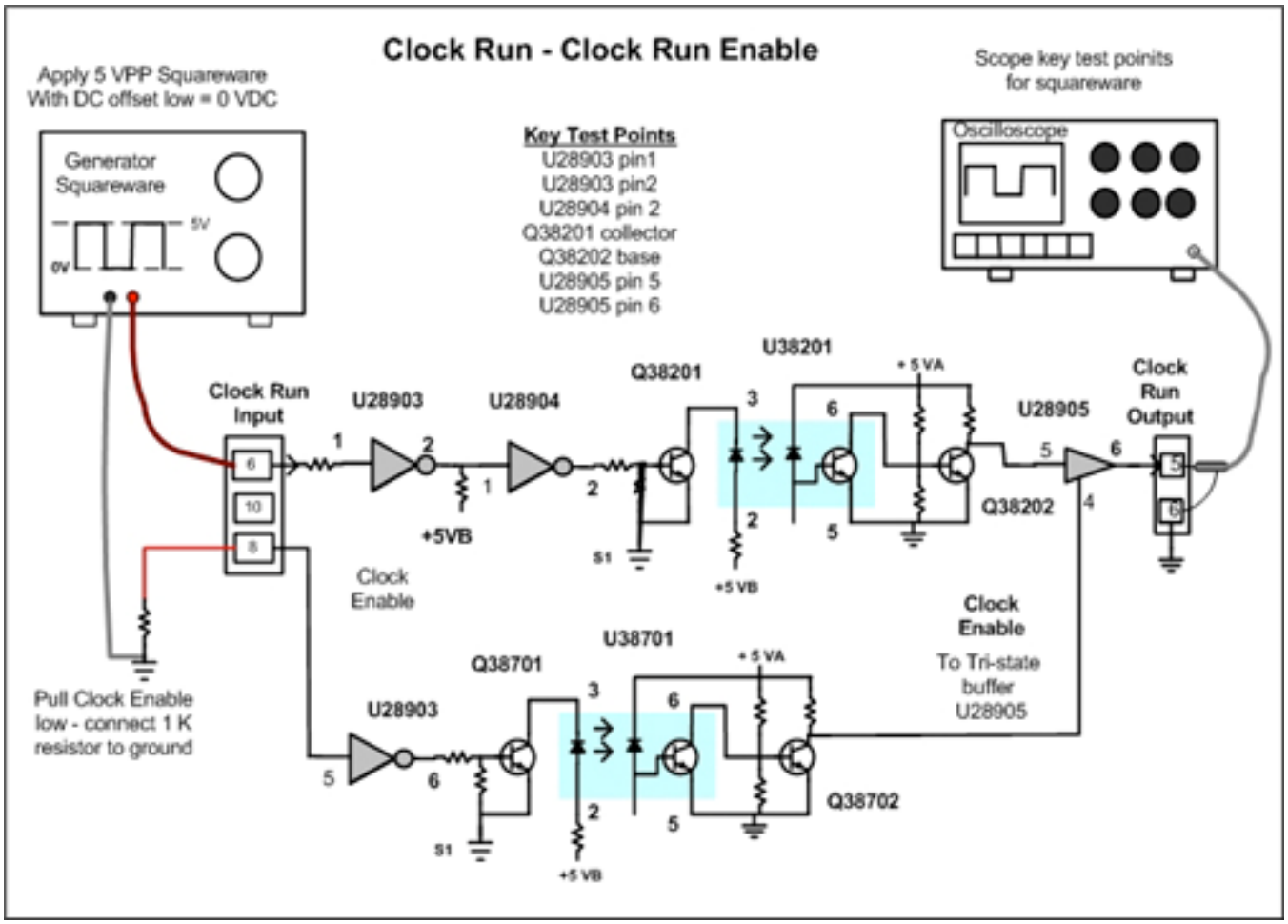


Figure 11. Trace the square-wave through the clock line to the output to isolate defects. The Clock Run and Clock STBY lines are identical.

To troubleshoot the Clock Run and Clock STBY lines, connect the square-wave generator to the Clock Run (pin 6) or Clock STBY (pin 7) input pin of the 36 pin input connector. Pull the Clock Enable pin low by connecting a 1 k ohm resistor from pin 8 of the 36 pin input connector to S1 ground.

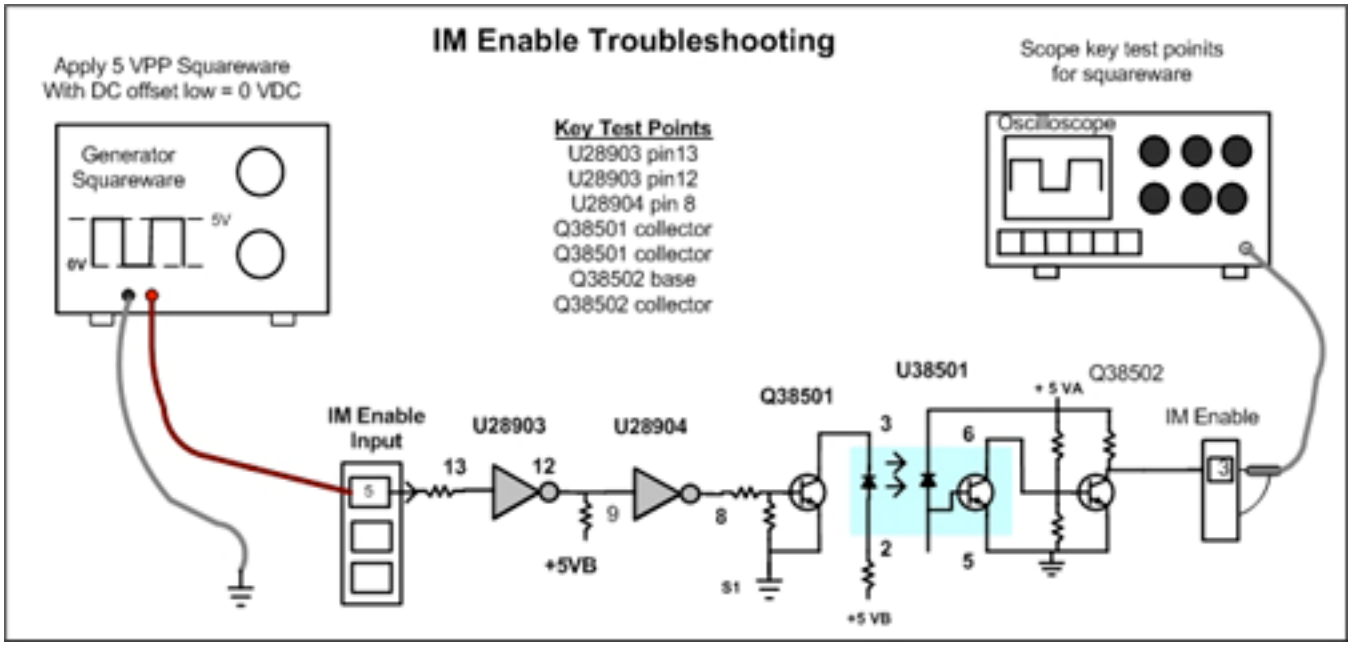


Figure 12. Trace the square-wave through the IM Enable path to isolate a defect.