PT 400933 Issue:-1.0

Date: 15.05.91

ECO 3855

4920/4920M Digital Assembly Test Procedure.

Test Equipment Required.

- 1. 4920 Test Chassis
- 2. Power supply load
- 3. 1061 DMM
- 4. Dual trace Scope
- 5. Frequency Counter
- 6. FSV Box

Abbreviations Used.

- 1. BUT Board Under Test
- 2. UUT Test Chassis
- 3. FSV Factory Selected Value
- 4. wrt With Respect To

Notes.

- 1. Unless otherwise specified, scope earth and/or DMM Lo should be connected to either TP503 or D513 anode during measurements on the BUT.
- 2. References to Left (LH), Right (RH), Front (FR) etc. should be applied to the view from the front of the test chassis.
- 3. A tick list should be raised (Page 5 of this procedure.) as testing of each assembly commences. The test procedure should be carried out in the sequence listed, faults recorded and rectified as they occur.
- 4. Ensure the board is at the latest ECO state.
- 5. Safety glasses should be worn throughout this procedure.

Procedure

- 1.0. Preliminary Checks.
- 1.1. Visually check the board for short circuits and components correctly fitted. Pay particular attention to polarised components.
- 1.2. Check that FSV R511 is not fitted.
- 1.3. Move TL502 to position B (rear) and TL501 to position B (right).

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- 1.4. Fit the EUT into the test chassis and connect PL5.
- 2.0. -15V and +5V Supplies.
- 2.1. Set the load to 5V, Lo load. Connect the load +ve lead to the front pin on TL502. Connect the -ve lead to TP503.
- 2.2. Set DMM to DCV Autorange. Connect DMM +ve lead to TP504 wrt load Lo test point.
- 2.3. Switch on UUT. If DMM reads more +ve than -10V switch off immediately and investigate fault. Check DMM reads between -15V and -16V.
 Check for overheating components.
- Move DMM Hi lead to Load Hi test point. Check DMM reads between +4.85V and +5.15V. Note reading. (Use A-B on DMM). Switch test load to Hi load and check that voltage changes by less than 0.050V.

 Deselect A-B on DMM.
 Switch load to S/C and check that DMM reads less than 3V.
 Switch off UUT.
- 3.0. 17V Supply.
- 3.1. Transfer load +ve lead to the left hand pin of TL501 and the -ve lead to TP501.
- 3.2. Set load to 17V, lo load.
 Switch on UUT. Check DMM reads between +15.6V and +16.9V.
 Select FSV R511 for +17.10V to +17.17V. (Limits 39K2 to 1M58)
 Note reading (use A-B).
 Switch load to Hi and check the change is less than 0.125V.
 Cancel A-B.
 Switch load to s/c and check DMM reads less than 1.5V.
 Switch off UUT.
- 3.3. Move TL502 to position A (front) and TL501 to position A (left).
- 4.0. Instrument Supplies.
- 4.1. Fit PL4, PL6, PL3, PL1 and PL2. Connect DMM +ve lead to TP502 and the -ve lead to TP503.
- 4.2. Switch on UUT. If DMM reads less than +35V or the displays are excessively bright, switch off and investigate. Check DMM reads between +42.75V and +47.25V.
- Transfer Hi lead to PL4.3 and check DMM reads between 7.3V and 8.1V.

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Select ACV, autorange on DMM. Check that the voltage between PL4-2 and PL4-4 is between 6.4V and 7.0V. Remove DMM.

- 4.5. Check that the voltage between PL6-1 and PL6-5 is between 30.2V and 31.8V. Remove DMM.
- 4.6. Select DCV autorange on DMM. Connect DMM Hi to D516 anode (OV STBY1) and Lo to TP503. Check that DMM reads less than 100mV.
- 4.7. Transfer Hi lead to D513 cathode, and check that DMM reads between +4.875V and +5.125V. Remove DMM.
- 4.8. Set scope as follows:

Mode : ADD, CH2 invert (Y1 and Y2 off)

Y1 and Y2 : 100mV/cm AC coupled Trigger mode : Line, AC coupled

Connect Y1 and Y2 probes either side of R502, earth to D513 anode.

Check scope shows an asymmetrical waveform approximately 200mV to 400mV pk-pk at frequency 100Hz with no HF ringing.

- 5.0. Processor Clock
- 5.1. Connect frequency counter to TP102 wrt TP503. Check that counter shows between 7.99200MHz and 8.00800MHz. Remove frequency counter.
- 6.0 2.5V Reference.
- 6.1. Connect DMM +ve lead to TP201 and the -ve lead to TP503. Check that DMM reads between +2.4V and +2.5V. Remove DMM.
- 7.0. Power Fail Detector.
- 7.1. Short TP305 to TP503 and check that the display goes blank and then returns to its powered up state upon removal of the short.
- 8.0. Clear cal stores
- 8.1. Slide switch on the rear panel to the right hand position to enable CAL.
- 8.2. Connect the temporary battery +ve lead to R533 and the -ve lead to E502.

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8.3. On UUT, press CAL and check that the left hand display shows the CAL legend.

Follow the sequence of key strokes:-

Press Spcl, Yes, ClrNV, All. The right hand display will display: Writing New BITSUMS When this message disappears press Caltrig.

The right hand display will display: NV Ram Clear in Progress. When this message disappears press Quit twice. Press Date, and check that the right hand display shows 12.12.81.12.12. Then press Quit, Due, and Quit twice.

- 9.0. Operational Test.
- 9.1. Press Test and from the menu select OPER. The UUT will now step through the various tests and on successful completion will display "OPER TEST COMPLETED".

 Press ACV.
- 10.0. External Trigger.
- 10.1. Press ExtTrig. Momentarily short E204 to TP503 and check that the LED on the A to D board flashes. Press ExtTrig to deselect.

ALL TESTS COMPLETE

11.0. Switch off UUT. remove temporary battery and solder R511.

4920/4920M Digital Assembly Test Procedure.

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Operator: -Serial No .:-Preliminary Checks. 1. -15V and +5V Supplies. 2. 3. 17V Supply. Instrument Supplies. 4. 5. Processor Clock. 2.5V Reference (6. Power Fail Detector. (7. Clear Cal Stores. (8. Operation Test. External Trigger.) 9.) 10. Remove Battery. Solder R511