



AOD410, AOD410L (Lead-Free)
N-Channel Enhancement Mode Field Effect Transistor

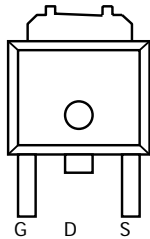
General Description

The AOD410 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications. AOD410L is offered in a lead-free package.

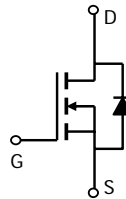
Features

V_{DS} (V) = 30V
 I_D = 8A
 $R_{DS(ON)} < 65m\Omega$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 105m\Omega$ ($V_{GS} = 4.5V$)

TO-252
D-PAK



Top View
Drain Connected to
Tab



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ\text{C}$	A
		$T_C=100^\circ\text{C}$	
Pulsed Drain Current ^B	I_{DM}	20	
Avalanche Current ^C	I_{AR}	8	A
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	10	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10\text{s}$	20	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		Steady-State	46	
Maximum Junction-to-Case ^C	$R_{\theta JL}$	5.3	7	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1	1.8	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=4.5\text{V}$, $V_{DS}=5\text{V}$	10			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=8\text{A}$ $T_J=125^\circ\text{C}$		48 76	65 100	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=6\text{A}$		75	105	
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=8\text{A}$		6.2		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.75	1	V
I_S	Maximum Body-Diode Continuous Current				4.3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1\text{MHz}$		288		pF
C_{oss}	Output Capacitance			57		pF
C_{rss}	Reverse Transfer Capacitance			39		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		3		Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $I_D=8\text{A}$		6.72		nC
$Q_g(4.5\text{V})$	Total Gate Charge			3.34		nC
Q_{gs}	Gate Source Charge			0.76		nC
Q_{gd}	Gate Drain Charge			1.78		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $R_L=1.8\Omega$, $R_{GEN}=3\Omega$		3.7		ns
t_r	Turn-On Rise Time			3.7		ns
$t_{D(off)}$	Turn-Off Delay Time			15.6		ns
t_f	Turn-Off Fall Time			2.6		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=8\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		12.6		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=8\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		5.1		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any a given application depends on the user's specific board design, and the maximum temperature fo 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on $T_{J(MAX)}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

G: The maximum current rating is limited by bond-wires.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

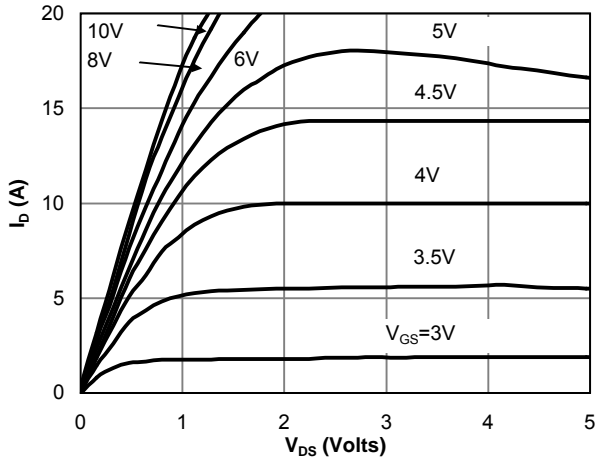


Fig 1: On-Region Characteristics

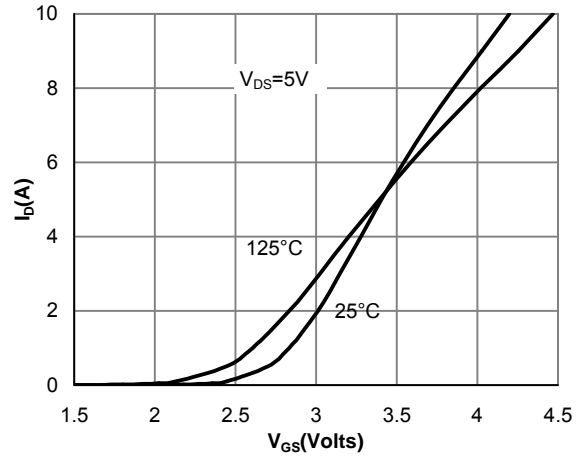


Figure 2: Transfer Characteristics

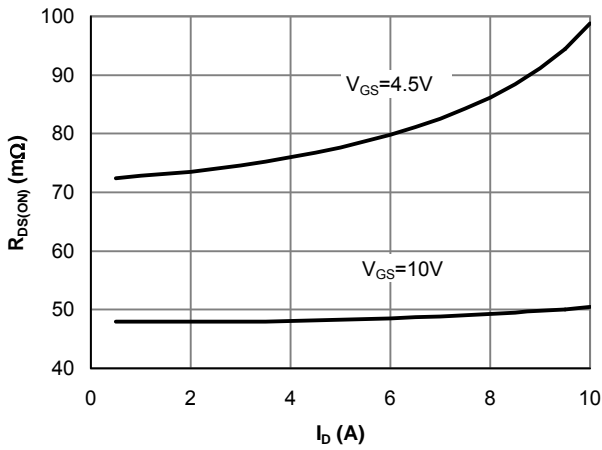


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

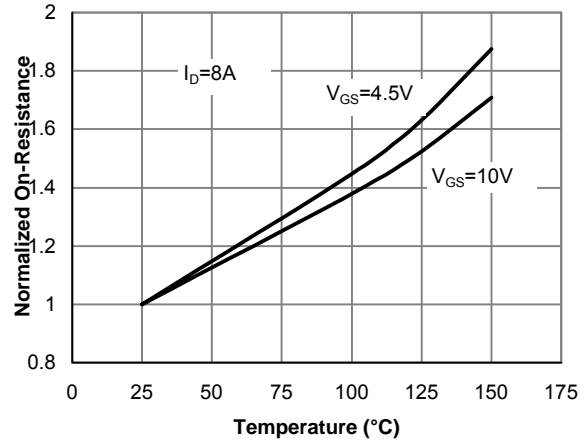


Figure 4: On-Resistance vs. Junction Temperature

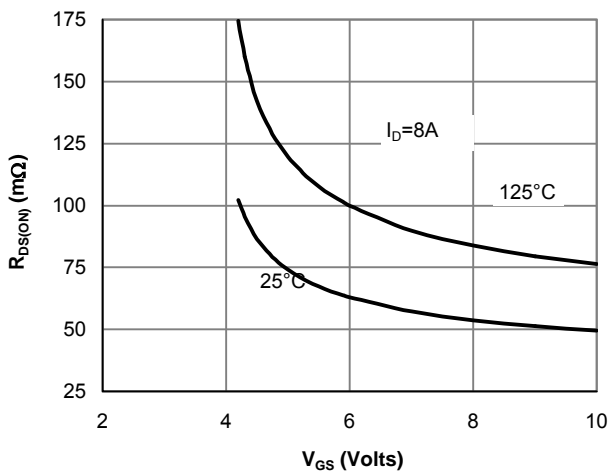


Figure 5: On-Resistance vs. Gate-Source Voltage

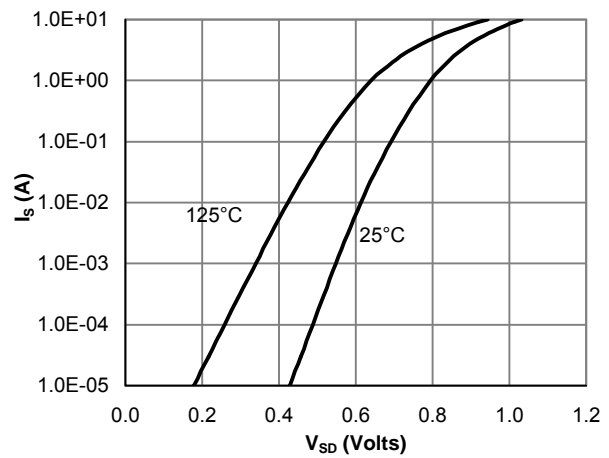


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

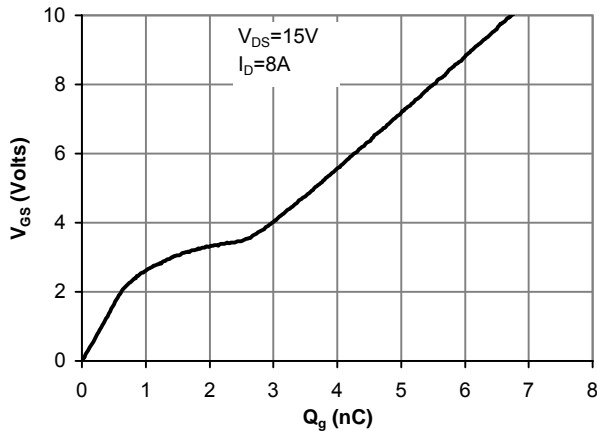


Figure 7: Gate-Charge Characteristics

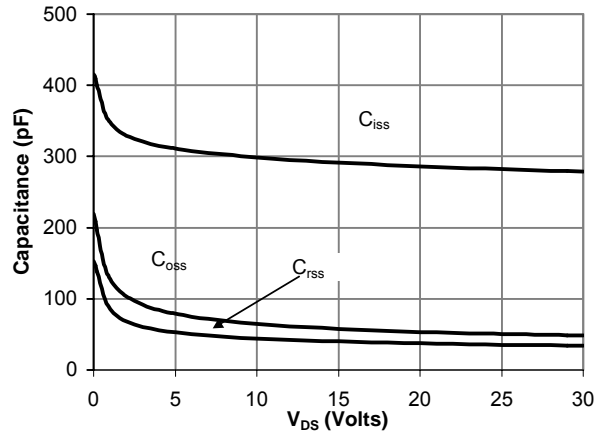


Figure 8: Capacitance Characteristics

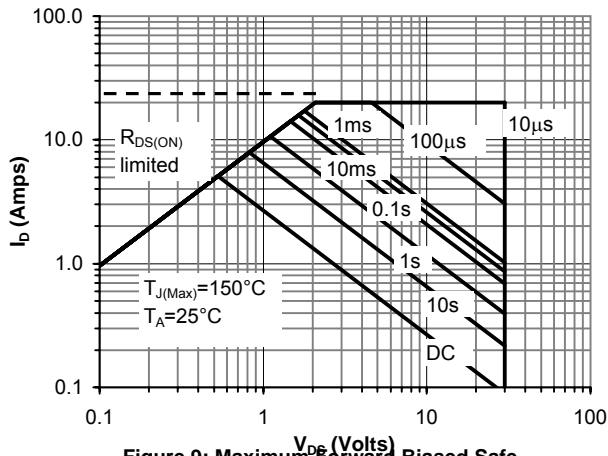


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

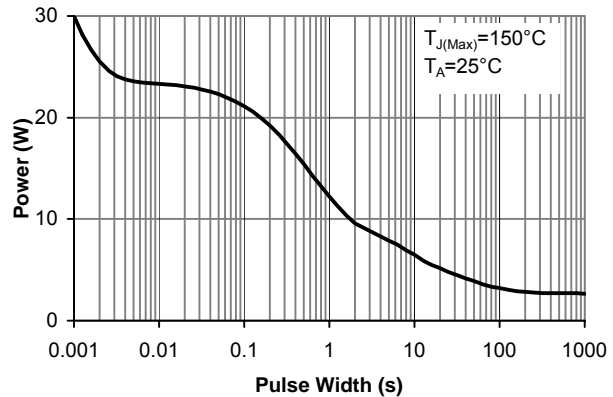


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

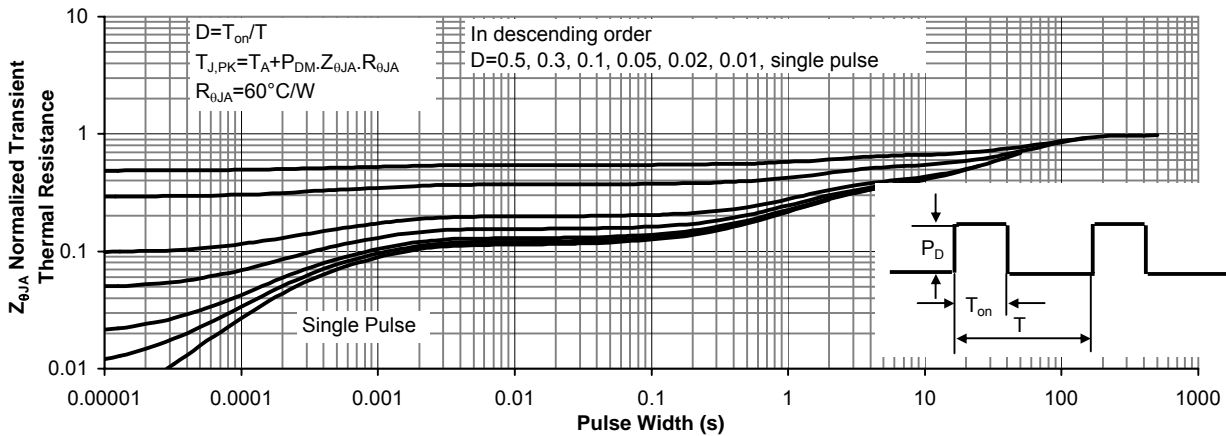
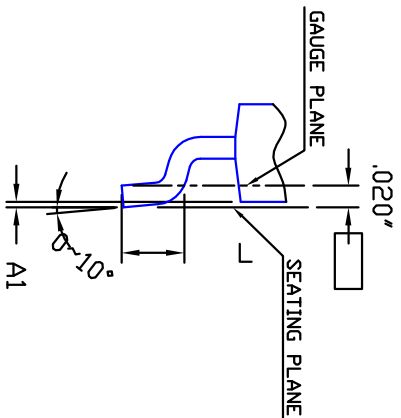
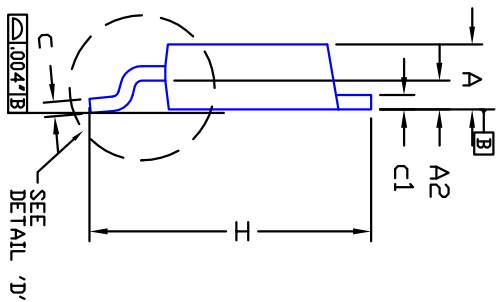
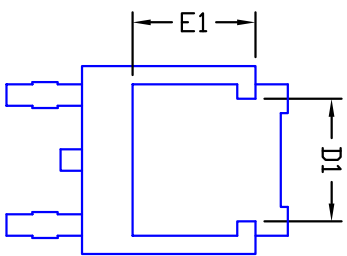
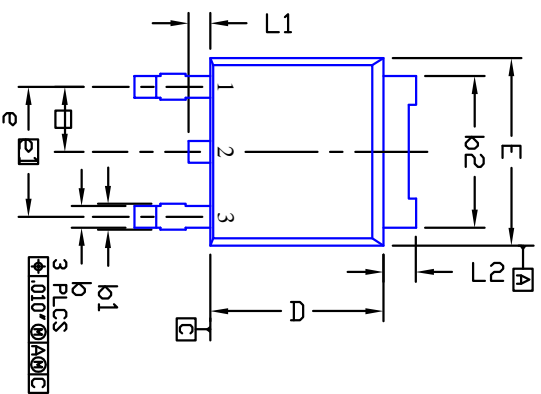


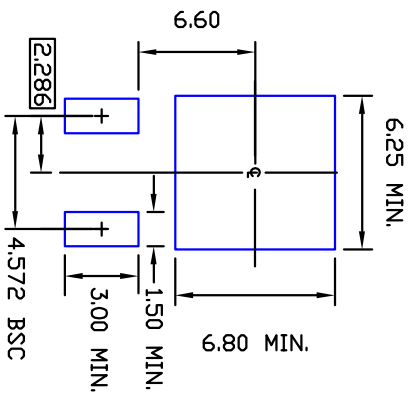
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



- NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS
 2. DIMENSION L IS MEASURED IN GAGE PLANE
 3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED
 4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
 5. FOLLOWED FROM JEDEC TO-252 (AA)

SYMBOL	DIMENSION IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.235	2.286	2.388	0.088	0.090	0.094
A1	0.000	-----	0.102	0.000	-----	0.004
A2	0.889	-----	1.143	0.035	-----	0.045
b	0.686	0.762	0.889	0.027	0.030	0.035
b1	0.889	-----	1.143	0.035	-----	0.045
b2	5.207	4.45	5.461	0.205	-----	0.215
c	0.457	0.508	0.559	0.018	0.020	0.022
c1	0.483	-----	0.584	0.019	-----	0.023
D	5.969	6.096	6.223	0.235	0.240	0.245
D1	4.318	-----	5.334	0.170	-----	0.210
E	6.477	6.604	6.731	0.255	0.260	0.265
E1	4.318	-----	-----	0.170	-----	-----
e	2.286 BSC.			0.090 BSC.		
e1	4.572 BSC.			0.180 BSC.		
H	9.779	-----	10.414	0.385	-----	0.410
L	1.270	-----	2.032	0.050	-----	0.080
L1	0.635	-----	1.016	0.025	-----	0.040
L2	0.889	-----	1.270	0.035	-----	0.050

RECOMMENDED LAND PATTERN



UNIT: mm

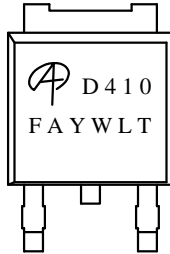
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL X.X ± XXX ± XXXX ± INTERPRET DIM AND TOL PER ASME Y14.5M - 1994 PRINTING IS SCALED TO FIT DO NOT SCALE DRAWING		
	THIRD ANGLE PROJECTION	
Document No.	PD-00009	DPak TO-252 PACKAGE OUTLINE
Version	rev A	
Title	DPak TO-252 PACKAGE OUTLINE	




ALPHA & OMEGA
SEMICONDUCTOR, LTD.

Document No.	PD-00086
Version	rev C
Title	AOD410 Marking Description

PACKAGE MARKING DESCRIPTION



NOTE:

-  - AOS LOGO
- D410 - PART NUMBER CODE.
- F&A - FOUNDRY AND ASSEMBLY LOCATION
- Y - YEAR CODE
- W - WEEK CODE.
- L T - ASSEMBLY LOT CODE

DPAK PART NO. CODE

PART NO.	CODE
AOD410	D410

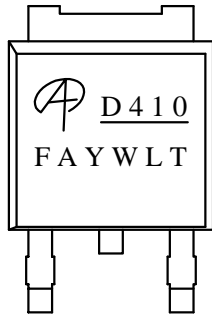


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SEMICONDUCTOR, LTD.


Document No.	PD-00190
Version	rev C
Title	AOD410L Marking Description

DPAK LEAD FREE

PACKAGE MARKING DESCRIPTION



NOTE:

-  - AOS LOGO
- D410 - PART NUMBER CODE, LEAD FREE
- F&A - FOUNDRY AND ASSEMBLY LOCATION
- Y - YEAR CODE
- W - WEEK CODE
- LT - ASSEMBLY LOT CODE

DPAK PART NO. CODE

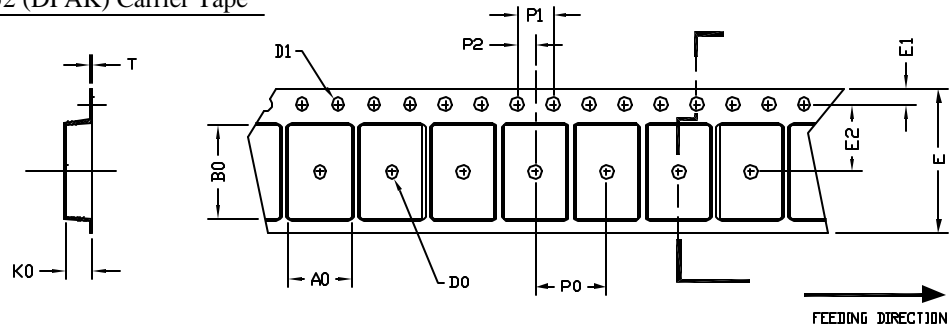
PART NO.	CODE
AOD410L	<u>D410</u>



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TO-252 (DPAK) Tape and Reel Data

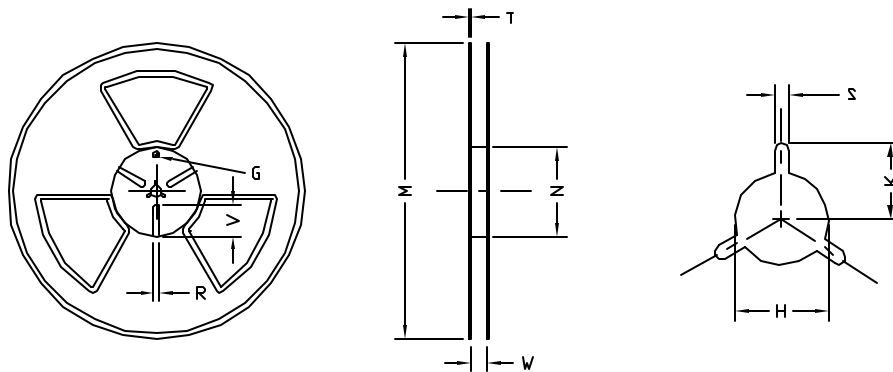
TO-252 (DPAK) Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TO-252(DPAK) (16 mm)	6.90 ±0.10	10.50 ±0.10	2.70 ±0.10	1.50 ±0.10	1.50 MIN.	16.00 ±0.10	1.75 ±0.10	7.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.30 ±0.05

TO-252 (DPAK) Reel



UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	T	H	K	S	G	R	V
16 mm	φ330	φ330.00 ±0.10	φ99.50 ±0.10	17.50 ±0.50	2.30	φ13.50 ±0.10	10.60	2.50 ±0.10	---	---	---

TO-252 (DPAK)

Leader / Trailer
& Orientation

