

Evaluation Board for Pseudo Differential Input, 10-/12-Bit ADCs with a Serial Interface

EVAL-AD7441/AD7451

FEATURES

Full-featured evaluation board for the AD7441/AD7451 EVAL-CONTROL-BRD2 compatible Standalone capability On-board analog buffering and reference Various linking options PC software for control and data analysis when used with the EVAL-CONTROL-BRD2

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

This data sheet describes the evaluation board for the AD7441/AD7451, which are 10-bit/12-bit, high speed, low power, successive approximation ADCs with a pseudo differential analog input. These parts operate from a single 2.7 V to 5.25 V power supply. Full details about the parts are available in the AD7441/AD7451 data sheet from Analog Devices, Inc., and it should be consulted in conjunction with this data sheet when using the evaluation board.

On-board components include

- One AD780, a pin-programmable, 2.5 V or 3 V ultrahigh precision band gap reference
- One AD8022 dual op amp
- One AD8021 single op amp
- One AD713 quad op amp
- One 7S04 inverter

Various link options are explained in Table 1 and Table 2.

Interfacing to this board is through a 96-way connector, which is also compatible with the EVAL-CONTROL-BRD2 from Analog Devices. External sockets are provided for a number of signals, including the V_{REF} input, the V_{IN+} and V_{IN-} inputs, the optional, external SCLK input, the \overline{CS} input, and the SDATA output.

Rev. 0

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TABLE OF CONTENTS

Features	1
Functional Block Diagram	1
General Description	1
Revision History	2
Evaluation Board Hardware	3
Power Supplies	3
Link Options	3
Setup Conditions	4
Interfacing to the EVAL-CONTROL-BRD2	5
Sockets	6
Connectors	6

REVISION HISTORY

12/06—Revision 0: Initial Version

Test Points	6
EVAL-CONTROL-BRD2 Operation	6
Evaluation Board Software	7
Installing the Software	7
Setting Up the Evaluation Board/EVAL-CONTROL-BRD2	27
Configuring the Boards	7
Using the Software	8
Evaluation Board Schematics and Artwork	. 11
Ordering Information	. 16
Ordering Guide	. 16
ESD Caution	. 16

EVALUATION BOARD HARDWARE

POWER SUPPLIES

When using this evaluation board with the EVAL-CONTROL-BRD2, all supplies are provided from the EVAL-CONTROL-BRD2 through the 96-way connector.

When using the board as a standalone unit, external supplies must be provided. This evaluation board has three power supply inputs.

- V_{DD} and AGND
- AGND, +12 V, -12 V
- +5 V and DGND

If the evaluation board is used in standalone mode, 2.7 V to 5.25 V must be connected to the V_{DD} input to supply the AD7441/AD7451 V_{DD} pin. To supply the AD8022 dual op amp, the AD713 quad op amp, and the AD780 voltage reference, +12 V and -12 V is needed. To supply the 7S04 inverter, +5 V is needed.

The supplies are decoupled to the relevant ground plane with 10 μ F tantalum and 0.1 μ F multilayer ceramic capacitors at the point where they enter the board. The supply pins of all op amps and the reference are also decoupled to AGND with a 10 μ F tantalum capacitor and a 0.1 μ F ceramic capacitor. The AD7441/AD7451 VDD supply pin is decoupled to AGND with 10 μ F tantalum and 0.1 μ F multilayer ceramic capacitors.

Extensive ground planes are used on this board to minimize the effect of high frequency noise interference. There are two ground planes, AGND and DGND. These are connected at one location close to the AD7441/AD7451.

LINK OPTIONS

There are 16 link options that must be positioned for the required operating setup before using the evaluation board. The functions of these options are outlined in Table 1.

Table 1. Link Option Functions

Link No.	Function
LK1	This link option selects the source of the VDD supply for the ADC.
	In Position A, the V_{DD} is supplied from the EVAL-CONTROL-BRD2.
	In Position B, the V_{DD} must be supplied from an external source via the power connector, J2.
LK2	This link option selects the analog input to V _{IN+} .
	In Position A, the analog input is generated by the bias-up circuit.
	In Position B, an external, unipolar, single-ended signal must be applied to the V_{IN+} input via P1.
	In Position C, the input to U2A, the AD8022 op amp used to buffer the single-ended signal, is tied to AGND.
LK3	This link option selects the analog input to V_{IN-} .
	In Position A, an external dc signal can be applied to the V_{IN-} input via P2.
	In Position B, V_{IN-} is tied to GND.
LK4	This link option selects the reference voltage applied to the VREF pin of the AD7441/AD7451.
	In Position A, an external signal must be supplied to the V_{REF} pin via P3.
	In Position B, the AD780 provides a 2.5 V/3 V reference to the V_{REF} pin.
_	In Position C, a divided down reference, 4/5 of the AD780 output, is applied to V _{REF} pin. Resistor R2 and Resistor R3 can be varied to alter the reference input.
LK5	This link option selects whether the output of the AD780 reference is applied directly to the AD7441/AD7451 or if it is divided down before it is applied.
	This link should be in Position A if a 2.5 V reference is required. In this case, LK7 should be inserted.
	This link should be in Position B if a 2 V reference is required. In this case, LK7 should be removed.
LK6	This link option controls the program pin of the AD780 reference voltage.
	When this link is inserted, the AD780 output voltage is set to 3.0 V.
	When this link is removed, the AD780 output voltage is set to 2.5 V.
LK7	This link option selects the analog input to U5, the op amp used to buffer the divided reference output from the AD780.
	When this link is removed, the divided reference voltage is applied to the noninverting input of the op amp. In this case, it acts as a buffer.
_	When this link is inserted, the noninverting input to the op amp is tied to GND. This link should be inserted if the op amp is not being used.
LK8	This link option sets the dc bias voltage that is applied to the bias-up circuit.
	In Position A, the bias voltage is set to V_{REF} (that is, the output of the AD780).
	In Position B, the bias voltage is set to $4/5 \times V_{REF}$.
	In Position C, the bias voltage is set to AGND. In this configuration, the bias-up circuit is not used.

Link No.	Function
LK9	This link option selects where the serial data out (SDATA) appears.
	In Position A, the data can be read by the EVAL-CONTROL-BRD2.
	In Position B, the data can be read via the external socket, P5.
LK10	This link is used to control the polarity of the serial clock applied to the SCLK pin.
	This link must be in Position A when LK11 is in Position A and when the SCLK is provided by the EVAL-CONTROL-BRD2. This means that data is valid on the falling edge of SCLK.
	This link may be placed in Position B when LK11 is in Position B to invert an SCLK from P6 if necessary. This would mean data could be read on the rising edge of SCLK but would only be possible with a slower SCLK frequency.
LK11	This link option selects the source of the SCLK input.
	In Position A, the SCLK input is provided by the EVAL-CONTROL-BRD2.
	In Position B, the SCLK input is provided via the external socket, P6.
LK12	This link option selects the source of the \overline{CS} input.
	In Position A, the CS input is provided by the EVAL-CONTROL-BRD2.
	In Position B, the CS input is provided via the external socket, P7.
LK13	This link option adds a 50 Ω termination to AGND at the VIN socket of the bias-up circuit (P4) for the analog input. This link should be inserted if a 50 Ω termination is required on the analog input.
LK14	This link option is used to select the source of the V– (-12 V) supply that is used to power the op amps.
	In Position A, the V– is supplied from the EVAL-CONTROL-BRD2 through the 96-way connector.
	In Position B, the V– is supplied from an external source via the power connector, J3.
LK15	This link option is used to select the source of the V+ (+12 V) supply that is used to power the op amps and external reference.
	In Position A, V+ is supplied from the EVAL-CONTROL-BRD2 through the 96-way connector.
	In Position B, V+ is supplied from an external source via the power connector, J3.
LK16	This link option selects the source of the +5 V digital supply.
	In Position A, +5 V is supplied by the EVAL-CONTROL-BRD2.
	In Position B, +5 V must be supplied from an external source via J4.

SETUP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are set up per the required operating mode. Table 2 shows the position that all the links are set to when the evaluation board is shipped. The board is compatible with the EVAL-CONTROL-BRD2 when shipped.

Link No.	Position	Function
LK1	А	V_{DD} is supplied by the EVAL-CONTROL-BRD2.
LK2	А	The analog input applied to V_{IN+} is supplied by the bias-up circuit.
LK3	В	V_{IN-} is tied to GND.
LK4	В	The voltage reference applied to V_{REF} is supplied by the AD780.
LK5	А	The voltage reference is taken directly from the output of the AD780.
LK6	Removed	The AD780 is set to provide a 2.5 V reference.
LK7	Inserted	U5 is not used; the input is tied to GND.
LK8	А	A voltage of 2.5 V from the AD780 is applied to the bias-up circuit.
LK9	А	SDATA is read by the EVAL-CONTROL-BRD2.
LK10	А	SCLK is not inverted.
LK11	А	SCLK is supplied by the EVAL-CONTROL-BRD2.
LK12	А	CS is supplied by the EVAL-CONTROL-BRD2.
LK13	Removed	A 50 Ω termination to GND is not applied to the input of the bias-up circuit.
LK14	А	V– is supplied by the EVAL-CONTROL-BRD2.
LK15	А	V+ is supplied by the EVAL-CONTROL-BRD2.
LK16	А	+5 V is supplied by the EVAL-CONTROL-BRD2.

Table 2. Initial Link Positions

INTERFACING TO THE EVAL-CONTROL-BRD2

Interfacing to the evaluation board is via a 96-way connector, J1. J1 is used to connect the evaluation board to the EVAL-CONTROL-BRD2 or other system. The pinout for the J1 connector is shown in Figure 2. Table 3 describes the pins on the 96-way connector used to interface between the EVAL-CONTROL-BRD2 and the EVAL-AD7441/AD7451. Table 4 gives its pin designations and functions.

Table 3. 96-Wa	y Connector Pin	Description
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Mnemonic	Description
DRO	Data Receive Zero. This input is connected to the SDATA pin of the AD7441/AD7451 via LK9. The data stream of the AD7451 consists of four leading zeros followed by the 12 bits of conversion data, provided MSB first. The data stream of the AD7441 consists of four leading zeros, followed by the 10 bits of conversion data, followed by two trailing zeros.
SCLK0	Serial Clock Zero. This continuous clock output is connected to the SCLK pin of the AD7441/AD7451 via LK11.
TFS0	Transmit Frame Sync Zero. This output is connected to the CS pin of the AD7441/AD7451 via LK12 to initiate conversions and to frame the serial data transfer.
RFS0	Receive Frame Sync Zero. This input is connected to the TFS0 pin of the ADSP-2189 to frame the serial data read.
DGND	Digital Ground. These lines are connected to the digital ground plane on the evaluation board. This allows the user to provide the digital supply via the connector along with the other digital signals.
AGND	Analog Ground. These lines are connected to the analog ground plane on the evaluation board.
AVDD	Analog +5 V Supply. These lines are connected to the VDD supply line on the evaluation board via LK1 to provide the supply for the AD7441/AD7451.
±12 V	± 12 V Supply. These lines are connected to the ± 12 V supply lines on the evaluation board via LK14 and LK15 to supply ± 12 V to the AD713, the AD8022s, and ± 12 V to the AD780.
AVSS	Analog –5 V Supply. These lines are connected to the AVSS supply line on the evaluation board via LK2 to supply –5 V to the AD8138 differential amplifiers.
+5 V	Digital +5 V Supply. This is used to provide a digital supply to the evaluation board for the digital logic.



Pin No	Row A	Row B	Row C
1 TIT NO.	NUW A		NUW C
1			
2			
3	DCND	DCND	
4	DGND	DGND	DGND
5	TECO		DRU
0	TFSU CCLV0		RFSU
/	SCLKU		SCLKU
8	+5 V	+5 V	+5 V
9			
10			
11	DCND	DCND	DCND
12	DGND	DGND	DGND
13			
14			
15	DCND	DCND	
10	DGND	DGND	DGND
1/			
18			
19		DCND	
20			
21			
22	AGND		
23			
24			
25	AGND		
20 27	AGND		AGND
27			
2ð 20			
29 20			
5U 21			
וכ רכ	AVOD	AVDD	AVDD
52	AVDD	AVDD	AVDD

¹The unused pins of the 96-way connector are not shown.

SOCKETS

There are seven input sockets relevant to the operation of the AD7441/AD7451 on this evaluation board. All sockets are used for applying an externally generated signal to the evaluation board. When operating the board with the EVAL-CONTROL-BRD2, the only necessary external socket used is P1. All of the other sockets are optional and if they are not used, their signals are supplied by the EVAL-CONTROL-BRD2. Most of these sockets are used when operating the board as a standalone unit, as all the required signals are supplied from external sources. The functions of these sockets are outlined in Table 5.

Table 5. Socket Functions

Socket	Function	Description
P1	VIN+ EXT	Subminiature BNC socket for an external unipolar input to be applied to the V_{IN+} analog input.
P2	VIN– EXT	Subminiature BNC socket for an external dc input to be applied to the V_{IN-} analog input.
Р3	EXT VREF	Subminiature BNC socket for an external reference input to be applied to the V _{REF} input.
P4	VIN	Subminiature BNC socket for a bipolar analog input signal to the V _{IN+} analog input (via the bias-up circuit).
P5	SDATA EXT	Subminiature BNC socket for the SDATA output.
P6	EXT SCLK	Subminiature BNC socket for an external SCLK input.
P7	EXT_CS	Subminiature BNC socket for an external CS input.

CONNECTORS

There are four connectors on the AD7441/AD7451 evaluation board as outlined in Table 6.

Table 6. Connector Functions

Connector	Function
J1	96-way connector for serial interface and power supply connections.
J2	External VDD and GND power connector.
J3	External +12 V, –12 V, and AGND power connector.
J4	External +5 V power connector.

TEST POINTS

There are five test points on the inputs to and the data output from the AD7441/AD7451 on the evaluation board. These enable the user to have easy access to these signals for probing, evaluating, and debugging.

EVAL-CONTROL-BRD2 OPERATION

The evaluation board can be operated as a standalone unit or in conjunction with the EVAL-CONTROL-BRD2. The EVAL-CONTROL-BRD2 is available from Analog Devices under the order entry EVAL-CONTROL-BRD2.

When interfacing the EVAL-AD7441/AD7451 directly to the EVAL-CONTROL-BRD2, all supplies and control signals to operate the AD7441/AD7451 are provided by the EVAL-CONTROL-BRD2. However, due to the nature of the DSP interface on the EVAL-CONTROL-BRD2, AD7441/AD7451 sampling rates greater than 580 kHz are not supported when interfacing the evaluation board directly to the EVAL-CONTROL-BRD2. This is because the clock frequencies on the ADSP-2189 on the EVAL-CONTROL-BRD2 are limited by the equation

$$\frac{CLKOUT}{2 \times (SCLKDIV + 1)}$$

where:

CLKOUT = 40 MHz

SCLKDIV = the number that users can choose to determine their required clock frequency.

This equation shows that the CLKOUT frequency can only be divided by factors of two because the value of SCLKDIV can only be an integer. Therefore, in the case of the AD7441/AD7451 where the maximum clock frequency is 18 MHz, the nearest clock frequency that can be generated by the DSP is 10 MHz (that is, SCLKDIV = 1), which results in a maximum sampling frequency of 580 kHz.

Software to communicate with the EVAL-CONTROL-BRD2 and AD7441/AD7451 is provided with the AD7441/AD7451 evaluation board package (see the Evaluation Board Software section). This EVAL-CONTROL-BRD2 also operates with all Analog Devices evaluation boards that end with the letters CB in their title.

The 96-way connector on the EVAL-AD7441/AD7451 plugs directly into the 96-way connector on the EVAL-CONTROL-BRD2. The EVAL-CONTROL-BRD2 provides all the supplies for the evaluation board. It is powered from a 12 V ac transformer. Suitable transformers are available from Analog Devices as an accessory under the following part numbers:

- EVAL-110VAC-US (for use in the U.S. or Japan)
- EVAL-220VAC-UK (for use in the U.K.)
- EVAL-220VAC-EU (for use in Europe)

These transformers are also available from other suppliers including Digikey (U.S.) and Campbell Collins (U.K.).

Connection between the EVAL-CONTROL-BRD2 and the serial port of a PC is via a standard Centronics printer port cable that is provided with the EVAL-CONTROL-BRD2 package. Refer to the manual accompanying the EVAL-CONTROL-BRD2 for more details.

EVALUATION BOARD SOFTWARE INSTALLING THE SOFTWARE

The EVAL-AD7441/AD7451 kit includes a CD-ROM containing the software that controls the EVAL-CONTROL-BRD2 and, therefore, the evaluation board.

When the CD is inserted into a PC, an installation program automatically begins. This program installs the evaluation software.

SETTING UP THE EVALUATION BOARD/EVAL-CONTROL-BRD2

This section describes how the evaluation board, EVAL-CONTROL-BRD2, and software should be set up to begin using the complete system.

- 1. Connect the EVAL-CONTROL-BRD2 and evaluation board together (via the 96-way connector).
- 2. Apply power to the EVAL-CONTROL-BRD2 via a 12 V ac transformer.
- 3. At this stage, the red LED should be flashing, which indicates that the EVAL-CONTROL-BRD2 is functional and ready to receive instructions.

Note that the software should be installed before connecting the printer port cable between the EVAL-CONTROL-BRD2 and the PC. This ensures that the printer port initializes properly. The printer port cable can then be connected between the PC and the EVAL-CONTROL-BRD2.

CONFIGURING THE BOARDS

For the AD7441/AD7451 evaluation board and EVAL-CONTROL_BRD2 to communicate with the software, the required configuration files must be loaded from the **Setup Menu** (see Figure 3). The configuration files are text based files that contain information about the evaluation board to be tested. The information covers the part name, number of samples to be taken, default sampling frequency, maximum sampling frequency, and power supply settings. The configuration file also contains the name of the DSP program file to be downloaded to the EVAL-CONTROL-BRD2.

To load the required configuration files, follow these steps:

- 1. Open the AD7441/AD7451 evaluation software.
- 2. Open the **File** menu and select **Setup**. This displays the setup menu dialog box (see Figure 3).
- 3. In the **Select a Configuration File** list box, select the appropriate configuration files. When using the AD7451, click the **AD7451.cfg** file. When using the AD7441, click the **AD7441.cfg** file.
- 4. Click the Load button. This resets the EVAL-CONTROL-BRD2 and downloads the DSP program. When the download is complete, the power supply settings indicated in the configuration file are set. You may hear some of the relays clicking. Drop-down list boxes such as Select No. Of Samples and Select Sample Frequency have been set to the default values specified by the configuration file. You are free to change these at will.
- 5. When all the settings are set, click **Close** to return to the main window (see Figure 4).

Note that the maximum clock frequency that can be used is limited by the ADSP-2189 on the EVAL-CONTROL-BRD2 (see the EVAL-CONTROL-BRD2 Operation section). In this case, the maximum clock that can be used is 10 MHz, giving a maximum sampling frequency of 580 kHz.



Figure 3. The Setup Menu

Typical Configuration File

A typical software configuration file (*.cfg) is shown here.

EVAL-CONTROL BOARD partname:AD7451 programname:ad7451-41.PRG

samplefrequency:100000
maxsamplefrequency:580000
samples:2048

+/-15V:on dvdd:5:on avdd:5:on bus:on ;options 2scomp, binary dataformat:Binary numberofbits:12 inputVmax:2.5 inputVmin:0 [endofconfig]

Operating with Difference Voltage Reference Inputs

The functionality of the AD7441/AD7451 allows a variable reference input in the range 100 mV to 3.5 V. The allowable reference input depends on the power supply to ensure the maximum ratings of the device are not exceeded. The standard reference on the evaluation board is 2.5 V. This maximum input voltage is setup in the configuration file (see the **inputVmax**: **2.5** in the Typical Configuration File section). As you change the reference input, you must be sure to adjust the **inputVmax** figure in the configuration file to ensure that accurate data is displayed in the software.

USING THE SOFTWARE

With the hardware properly set up and configured, you can now use the software to control the EVAL-CONTROL-BRD2 and the AD7441/AD7451 evaluation board.

The main window in Figure 4 appears when the software is loaded. The main function of this window is to allow you to read a predetermined number of samples from the evaluation board and display them in both the time and frequency domain. This section discusses the content of the main window as they are illustrated in Figure 4.

Status Boxes

These boxes indicate the setup of the evaluation board/device, the number of samples taken, and display any information or error messages that are generated.

Menu Bar

The menu bar allows you to enter the setup menu, select the printer port to be used to control the EVAL-CONTROL-BRD2, load and save data, and get information about the software.

File Menu

The options available from this menu include the following:

- Setup Menu. Selecting this option displays the Setup Menu. See Figure 3 and the Configuring the Boards section for a detailed description of this menu.
- Load Raw Data. Selecting this option allows you to load data that had been saved by the software during a previous session.
- Save Raw Data. Selecting this option allows you to save the current set of sample data points. The data can later be reloaded to the EVAL-CONTROL-BRD2 software or can be used by other programs for further analysis.
- Save Binary Data. Selecting this option allows you to save the current set of sample data points. The data is saved in binary format as a text file. This method can be useful for examining issues such as code flicker, stuck bits, and more.
- Save FFT Data. Selecting this option allows you to save the current set of FFT data points. FFT data cannot be reloaded into the EVAL-CONTROL-BRD2 software, but can be loaded into other software packages for further analysis.
- **Exit.** Quits the program.

Printer Port

If the operating system being used is Windows[®] 95 or Windows[®] 98, this menu item allows you to select which printer port should be used for communication with the EVAL-CONTROL-BRD2.

- **LPT1.** This option selects 0x378 as the printer port address. This is the default option.
- **LPT2.** This option selects 0x278 as the printer port address.
- **PRN.** This option selects 0x3BC as the printer port address.

If Windows 2000° or Windows° NT is used, the software automatically detects the first printer port.

Help

This menu item gives information about the current revision of software for the particular evaluation board being used.



Figure 4. AD7441/AD7451 Evaluation Software, Main Window

Control Buttons

The control buttons allow you to take samples, power up and power down the part, reset the part, and quit the program.

Sample Button

When you click **Sample**, the software instructs the EVAL-CONTROL-BRD2 to take the required number of samples at the required frequency from the evaluation board. The AD7441/ AD7451 evaluation board runs up to 580 kSPS. As a result, you can choose the sampling frequency up to this rate and can also choose the number of samples to be taken. The maximum sampling frequencies as described in the AD7441/AD7451 data sheet can only be achieved when operating the evaluation board as a standalone unit. This is a clock frequency limitation of the DSP on the EVAL-CONTROL-BRD2 (as explained in the EVAL-CONTROL-BRD2 Operation section).

The samples taken are then uploaded and displayed. An FFT and Histogram are also calculated and displayed (see the Fast Fourier Transform/Histogram section). If you click **Cont Samp**, the software repeats the process indefinitely until you click the **Stop Samp** button. When the software is continuously sampling data, the other control buttons are disabled.

Power Down/Power Up Buttons

These buttons allow you to place the part into power-down and then power up the part again.

To enter power-down, click the **Power Down** button.

To exit power-down, click the **Power Up** button (see the Modes of Operation section in the AD7441/AD7451 data sheet).

Reset Button

The **Reset** button causes the EVAL-CONTROL-BRD2 to perform a reset function. When this happens, the power supplies are turned off and the program in DSP memory is lost. Repeat the setup instructions to download another program, if required.

Quit

The **Quit** button exits the software; the program running on the EVAL-CONTROL-BRD2 is not terminated.

Digital Storage Oscilloscope (DSO)

When samples are uploaded from the EVAL-CONTROL-BRD2, they are displayed here. The samples can be displayed as either integer values or voltages. Once samples have been displayed, click any point on the graph to display the sample number and value directly beneath the pointer. Along the axis of the graph are zoom sliders. These allow you to zoom in and zoom out to get a closer look at a particular sample, if required.

When another set of samples is taken, the graph attempts to display all values collected unless the **Hold Zoom** check box is selected. In this case, the graph keeps the same axis settings as the previous set of data samples. Additional check boxes are provided to give you control over the vertical grids, horizontal grids, and data points.

Fast Fourier Transform/Histogram

The lower section of the screen shows either a fast fourier transform (FFT) of the data or a histogram that shows the number of occurrences of each particular code read back.

The FFT (the default option) is typically selected if you are concerned with examining the ADC performance in the frequency domain.

The histogram gives an indication of the ADC performance to dc signals. The option displayed can be switched by clicking the **FFT Mode/Histogram Mode** button in the top right of the screen. Figure 5 shows the main window when the histogram mode option is selected.

6233-004



Figure 5. AD7441/AD7451 Evaluation Software, Main Screen, Histogram Mode

EVALUATION BOARD SCHEMATICS AND ARTWORK 900-52390 RFSO (J1-A6 TFSD DR0 J1-C5 <J1-C6 J1-C7 (J1-A7 EDATA EXT SCLK − Ex1_CS یں ابلو PK9 LK12 LK1 N N G G NC7S0. ≺ J1-A32 J1-B32 J1-C32 U3 QVQ QVQ LK10 10 CF 40 E) 2<u>5</u>2 E> ╡┟ 0.1uF ខ SDATA S SCLK VBIAS Ľ AD7441/51/53BRT GND 680 \triangleright ĝ 5 ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ VREF \triangleright ⊥ C2 ⊤ 0.1⊌F -0.1uF VBD EXT J2-1 D GND J2-2 Ot G 62R Ç Ξ Ò U5 ADB021AR 10pf 0.1uF | C13 + 0.1uF | C14 10 LF 0.1uF C15 U2-B 81+ \land 9 \triangleright 390R . LK7 100R QAO AO Ģ С C 20 2 VIN+ EXT VIN- EXT AD780 OP_SEL NIV+ EMP 킈 51 69 \rightarrow + ^ C9 10uF 16V Figure 6. AD7441/AD7451CB Evaluation Board Schematic Page 1

Rev. 0 | Page 11 of 16



Rev. 0 | Page 12 of 16

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Eval-AD7441/51/53CB (Rev. 0) - Component Side View Component Side

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Figure 8. Component Side Artwork

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06233-009



Eval-AD7441/51/53CB (Rev. 0) - Component Side View

Solder Side

-\$--

Figure 9. Solder Side Artwork

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06233-010



Eval-AD7441/51/53CB (Rev. 0) - Component Side View

Silkscreen

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Figure 10. Component Placement Drawing

ORDERING INFORMATION

Table 7. Bill Of Materials

Qty	Part Type	Reference Designator	Order Number ¹
1	AD7441/AD7451/AD7453	U1	AD7441BRT/
			AD7451BRT/
1	400000		AD/453BRI
1		02	AD8022AR
1	NC/S04M5	03	FEC 685-914
1	AD780	04	AD780AR
1	AD8021	05	AD8021AR
1	AD713	06	AD713JN
4	10 μF Tantalum Capacitor, 10 V	C1, C4, C5, C28	FEC 197-130
17	0.1 µF Ceramic Capacitor, SMD 0603	C2, C3, C6, C8, C10, C11, C14, C15, C19, C22, C24, C26, C27, C29, C31, C34, C35	FEC 499-675
1	1 nF Ceramic Capacitor, SMD 0603	C7	FEC 317-202
1	10 pF Ceramic Capacitor SMD 0603	C12	FEC 111-8159
11	10 μF Tantalum Capacitor, 16 V	C9, C13, C16, C20, C21, C23, C25, C30, C32, C33, C36	FEC 498-737
2	68 pF Ceramic Capacitor, SMD 0603	C17, C18	FEC 722-066
1	SCD103C Schottky Diode	D1	SD 103C
1	62 Ω, 0.1 W, 0.1% Resistor, SMD 0603	R1	FEC 357-1257
1	100 Ω, 0.1 W, 0.1% Resistor, SMD 0603	R2	FEC 114-0391
1	390 Ω, 0.1 W, 0.1% Resistor, SMD 0603	R3	FEC 911-185
1	3 kΩ, 0.1 W, 0.1% Resistor, SMD 0603	R4	FEC 357-1452
5	1 kΩ, 0.1 W, 0.1% Resistor, SMD 0603	R5, R7, R8, R9, R10	FEC 911-239
1	51.1 Ω, 0.1 W, 0.1% Resistor, SMD 0603	R6	FEC 114-0446
1	CON\41612\96 Connector	J1	FEC 225-393
2	2-Pin Terminal Block	J2 and J4	FEC 151-785
1	3-Pin Terminal Block	J3	FEC 151-786
10	2-Way Jumper (2 \times 2)	LK1, LK3, LK5, LK9 to LK12, LK14 to LK16	FEC 511-791
3	3-Way Jumper (2 \times 3)	LK2, LK4, LK8	FEC 511-780
3	1-Way Jumper (2 \times 1)	LK6, LK7, LK13	FEC 511-705
16	Shorting Link	LK1 to LK16	FEC 150-411
7	Gold 50 Ω SMB Jack	P1 to P7	FEC 419-4615
5	Test Point	TP1, TP2, TP3, TP4, TP5	FEC 240-382
4	Stick-On Feet	Each Corner	FEC 148-922

¹ FEC= Farnell Electronic

ORDERING GUIDE

Model	Description
EVAL-AD7441CB	AD7441 Evaluation Board
EVAL-AD7451CB	AD7451 Evaluation Board

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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