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# HD74ALVC162835A

## 18-bit Universal Bus Driver with 3-state Outputs

# HITACHI

ADE-205-294A (Z)  
2nd. Edition  
November 1999

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### Description

The HD74ALVC162835A is an 18-bit universal bus driver designed for 2.3 V to 3.6 V  $V_{CC}$  operation.

Data flow from A to Y is controlled by the output enable ( $\overline{OE}$ ). The device operates in the transparent mode when the latch enable (LE) is high. When LE is low, the A data is latched if the clock (CLK) input is held at a high or low logic level. If the LE is low, the A data is stored in the latch/flip flop on the low to high transition of CLK. When  $\overline{OE}$  is high, the outputs are in the high impedance state.

To ensure the high impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

All outputs, which are designed to sink up to 12 mA, include series dumping resistors to reduce overshoot and undershoot.

### Features

- Supports PC133 and meets “PC SDRAM registered DIMM specification, Rev. 1.1”
- $V_{CC} = 2.3\text{ V to }3.6\text{ V}$
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V}$  (@  $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot  $> 2.0\text{ V}$  (@  $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- High output current  $\pm 12\text{ mA}$  (@  $V_{CC} = 3.0\text{ V}$ )
- All outputs have series dumping resistors, so no external resistors are required
- $t_{pd}$  (CLK to Y) = 3.5 ns (Max) (@  $V_{CC} = 3.3\pm 0.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_a = 0\text{ to }85^\circ\text{C}$ )
- $t_{pd}$  (CLK to Y) = 2.5 ns (Max) (@  $V_{CC} = 3.3\pm 0.3\text{ V}$ ,  $C_L = 30\text{ pF}$ ,  $T_a = 0\text{ to }85^\circ\text{C}$ )

**Function Table****Inputs**

$\overline{OE}$	LE	CLK	A	Output Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L or H	X	$Y_0^{*1}$

H : High level

L : Low level

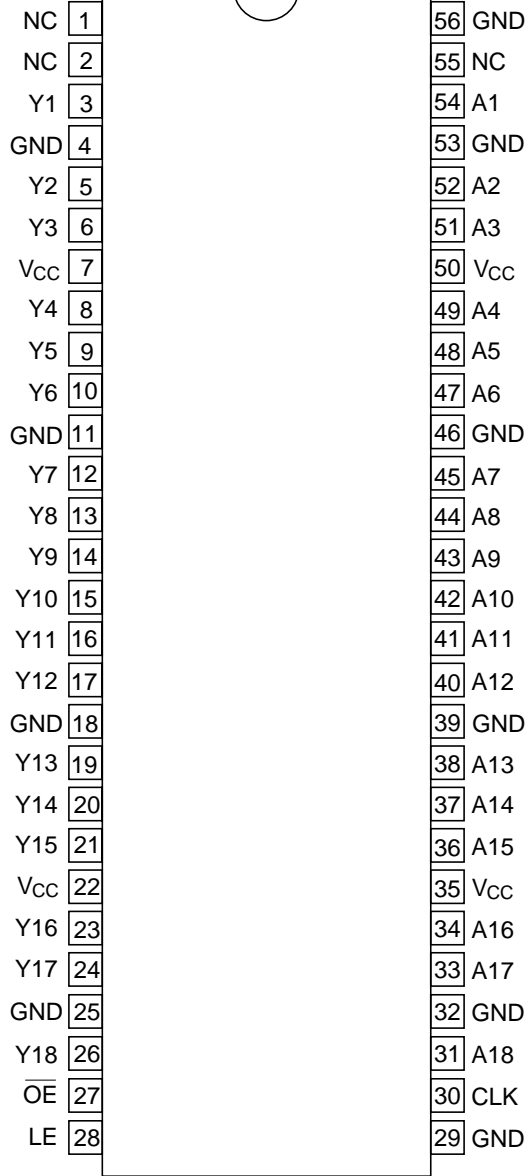
X : Immaterial

Z : High impedance

↑ : Low to high transition

Note: 1. Output level before the indicated steady-state input conditions were established.

Pin Arrangement



(Top view)

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	$V_{CC}$	-0.5 to 4.6	V	
Input voltage range <sup>1</sup>	$V_I$	-0.5 to 4.6	V	
Output voltage range <sup>1, 2</sup>	$V_O$	-0.5 to $V_{CC}+0.5$	V	
Input clamp current	$I_{IK}$	-50	mA	$V_I < 0$
Output clamp current	$I_{OK}$	$\pm 50$	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	$\pm 50$	mA	$V_O = 0$ to $V_{CC}$
$V_{CC}$ , GND current / pin	$I_{CC}$ or $I_{GND}$	$\pm 100$	mA	
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) <sup>3</sup>	$P_T$	1	W	TSSOP
Storage temperature range	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating condition" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

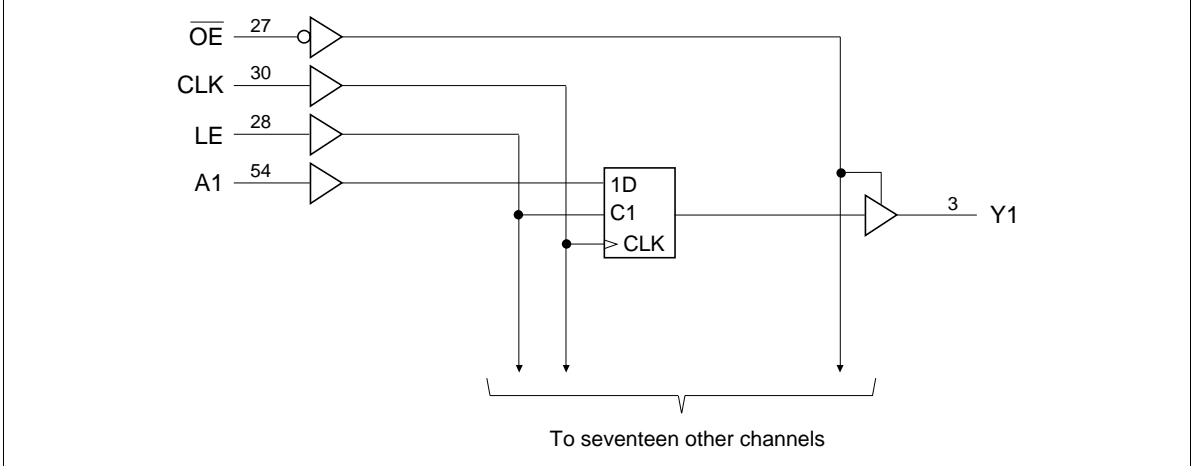
- Notes:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp current ratings are observed.
  2. The input and output positive-voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
  3. The maximum power dissipation is calculated using a junction temperature of 150 $^\circ\text{C}$  and board trace length of 750 mils.

## Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	$V_{CC}$	2.3	3.6	V	
Input voltage	$V_I$	0	$V_{CC}$	V	
Output voltage	$V_O$	0	$V_{CC}$	V	
High-level output current	$I_{OH}$	—	-6	mA	$V_{CC} = 2.3\text{ V}$
		—	-8		$V_{CC} = 2.7\text{ V}$
		—	-12		$V_{CC} = 3.0\text{ V}$
Low-level output current	$I_{OL}$	—	6	mA	$V_{CC} = 2.3\text{ V}$
		—	8		$V_{CC} = 2.7\text{ V}$
		—	12		$V_{CC} = 3.0\text{ V}$
Input transition rise or fall rate	$\Delta t/\Delta v$	0	10	ns/V	
Operating free-air temperature	$T_a$	-40	85	$^\circ\text{C}$	

Note: Unused or floating control pins must be held high or low.

Logic Diagram



## Electrical Characteristics

Item	Symbol	$V_{CC}$ (V)	$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions			
			Min	Max					
Input voltage	$V_{IH}$	2.3 to 2.7	1.7	—	V				
		2.7 to 3.6	2.0	—					
	$V_{IL}$	2.3 to 2.7	—	0.7	V				
		2.7 to 3.6	—	0.8					
Output voltage	$V_{OH}$	2.3 to 3.6	$V_{CC}-0.2$	—	V	$I_{OH} = -100 \mu\text{A}$			
		2.3	1.9	—		$I_{OH} = -4 \text{ mA}, V_{IH} = 1.7 \text{ V}$			
		2.3	1.7	—		$I_{OH} = -6 \text{ mA}, V_{IH} = 1.7 \text{ V}$			
		3.0	2.4	—		$I_{OH} = -6 \text{ mA}, V_{IH} = 2.0 \text{ V}$			
		2.7	2.0	—		$I_{OH} = -8 \text{ mA}, V_{IH} = 2.0 \text{ V}$			
		3.0	2.0	—		$I_{OH} = -12 \text{ mA}, V_{IH} = 2.0 \text{ V}$			
	$V_{OL}$	2.3 to 3.6	—	0.2	V	$I_{OL} = 100 \mu\text{A}$			
		2.3	—	0.4		$I_{OL} = 4 \text{ mA}, V_{IL} = 0.7 \text{ V}$			
		2.3	—	0.55		$I_{OL} = 6 \text{ mA}, V_{IL} = 0.7 \text{ V}$			
		3.0	—	0.55		$I_{OL} = 6 \text{ mA}, V_{IL} = 0.8 \text{ V}$			
		2.7	—	0.6		$I_{OL} = 8 \text{ mA}, V_{IL} = 0.8 \text{ V}$			
		3.0	—	0.8		$I_{OL} = 12 \text{ mA}, V_{IL} = 0.8 \text{ V}$			
		Input current	$I_{IN}$	3.6		—	$\pm 5.0$	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND
		Off state output current	$I_{OZ}$	3.6		—	$\pm 10$	$\mu\text{A}$	$V_{OUT} = V_{CC}$ or GND
Quiescent supply current	$I_{CC}$	3.6	—	40	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND			
	$\Delta I_{CC}$	3.0 to 3.6	—	750	$\mu\text{A}$	One input at $(V_{CC}-0.6)\text{V}$ , other inputs at $V_{CC}$ or GND			

**Switching Characteristics** (Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	From (Input)	To (Output)	
Maximum clock frequency	f <sub>max</sub>	2.5±0.2	150	—	—	MHz			
		2.7	150	—	—				
		3.3±0.3	150	—	—				
Propagation delay time	t <sub>PLH</sub>	2.5±0.2	1.0	—	5.0	ns	A	Y	
		2.7	—	—	5.0				
		3.3±0.3	1.0	—	4.2				
	t <sub>PHL</sub>	2.5±0.2	1.3	—	5.9		LE	Y	
		2.7	—	—	5.8				
		3.3±0.3	1.3	—	5.1				
			2.5±0.2	1.4	—	6.3		CLK	Y
			2.7	—	—	6.1			
			3.3±0.3	1.4	—	5.4			
Output enable time	t <sub>ZH</sub>	2.5±0.2	1.4	—	6.3	ns	OE	Y	
		2.7	—	—	6.5				
		3.3±0.3	1.1	—	5.5				
Output disable time	t <sub>ZL</sub>	2.5±0.2	1.0	—	4.7	ns	OE	Y	
		2.7	—	—	4.9				
		3.3±0.3	1.3	—	4.5				
Input capacitance	C <sub>IN</sub>	3.3	3.3	4.0	4.5	pF	Control inputs		
		3.3	3.0	6.0	9.0		Data inputs		
Output capacitance	C <sub>O</sub>	3.3	3.0	7.0	9.0	pF	Y ports		

## Switching Characteristics (Ta = -40 to 85°C) (cont)

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	From (Input)
Setup time	t <sub>su</sub>	2.5±0.2	2.2	—	—	ns	Data before CLK↑
		2.7	2.1	—	—		
		3.3±0.3	1.7	—	—		
		2.5±0.2	1.9	—	—	ns	Data before LE↓
		2.7	1.6	—	—		CLK "H"
		3.3±0.3	1.5	—	—		
		2.5±0.2	1.3	—	—	ns	Data before LE↓
		2.7	1.1	—	—		CLK "L"
3.3±0.3	1.0	—	—				
Hold time	t <sub>h</sub>	2.5±0.2	0.6	—	—	ns	Data after CLK↑
		2.7	0.6	—	—		
		3.3±0.3	0.7	—	—		
		2.5±0.2	1.4	—	—	ns	Data after LE↓
		2.7	1.7	—	—		CLK "H" or "L"
		3.3±0.3	1.4	—	—		
Pulse width	t <sub>w</sub>	2.5±0.2	3.3	—	—	ns	LE "H"
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		
		2.5±0.2	3.3	—	—	ns	CLK "H" or "L"
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		

## Switching Characteristics (Ta = 0 to 85°C)

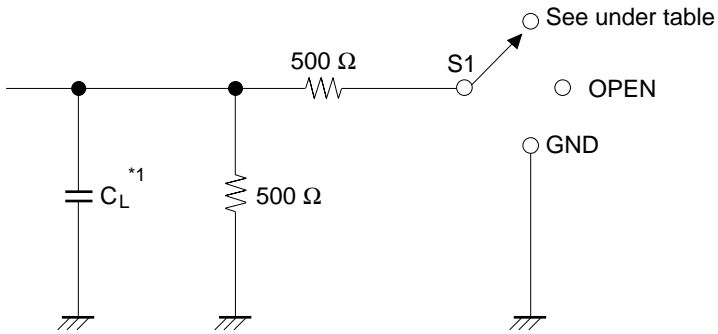
Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)	
Propagation delay time	C <sub>L</sub> =50pF	t <sub>PLH</sub> , t <sub>PHL</sub>	3.3±0.3	1.4	—	3.5	ns	CLK	Y
			3.3±0.3	0.7	—	2.5		CLK	Y
Setup time	t <sub>su</sub>	3.3±0.3	1.0	—	—	ns	Data before CLK↑		
Hold time	t <sub>h</sub>	3.3±0.3	0.6	—	—	ns	Data after CLK↑		



**Operating Characteristics** ( $T_a = 25^\circ\text{C}$ )

Item	Symbol	$V_{CC} = 2.5 \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \pm 0.3 \text{ V}$	Unit	Test Conditions
		Typ	Typ		
Power dissipation capacitance	Outputs enable	22.0	24.5	pF	$C_L = 0, f = 10 \text{ MHz}$
	Outputs disable	5.0	6.0		

## Test Circuit

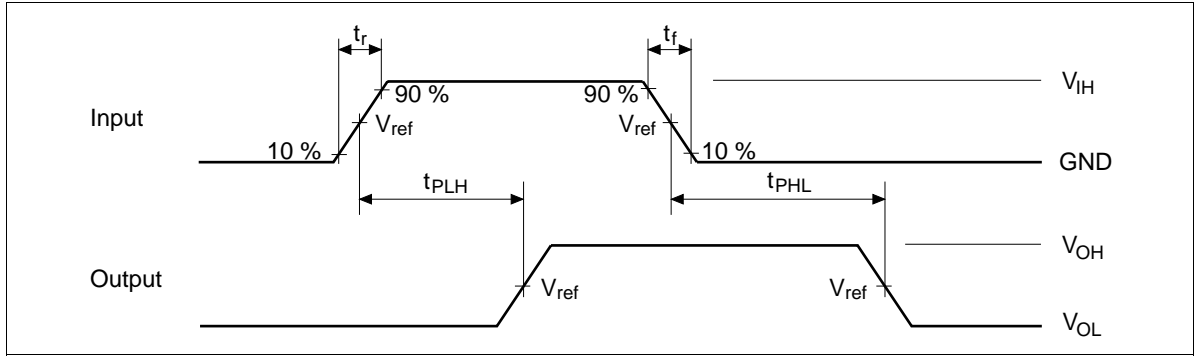


Load Circuit for Outputs

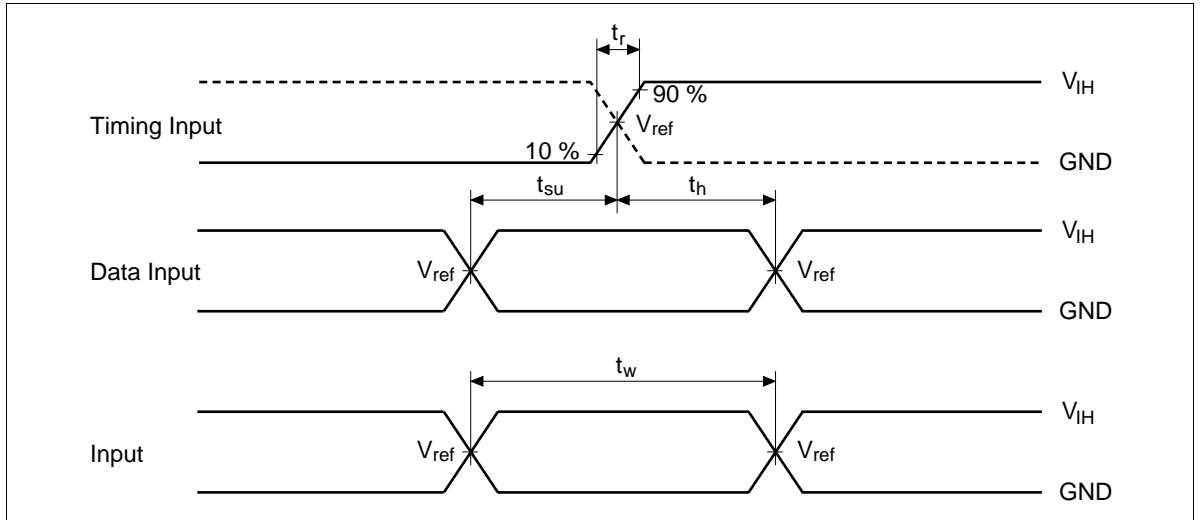
Symbol	$V_{CC}=2.5\pm 0.2V$	$V_{CC}=2.7V,$ $3.3\pm 0.3V$
$t_{PLH}/t_{PHL}$	OPEN	OPEN
$t_{su}/t_h/t_w$	OPEN	OPEN
$t_{ZH}/t_{HZ}$	GND	GND
$t_{ZL}/t_{LZ}$	$2 \times V_{CC}$	6.0 V
$C_L$	30 pF	50 pF

Note: 1.  $C_L$  includes probe and jig capacitance.

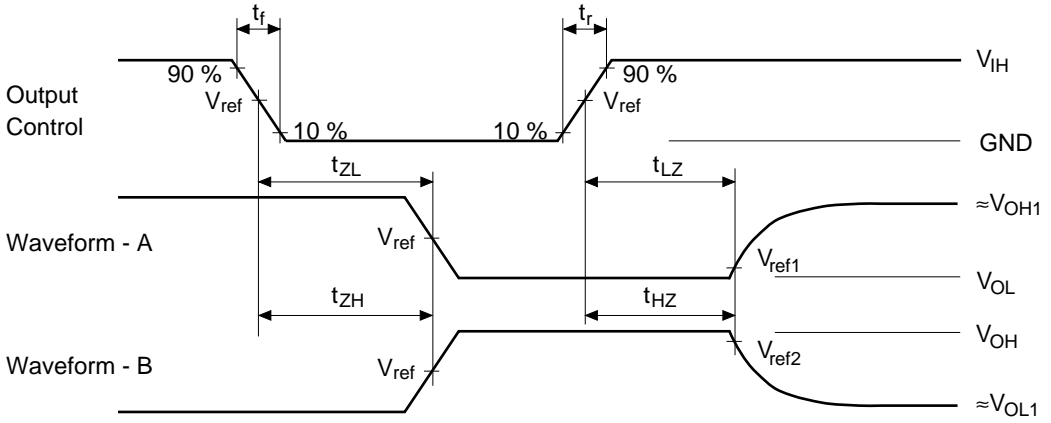
Waveforms – 1



Waveforms – 2



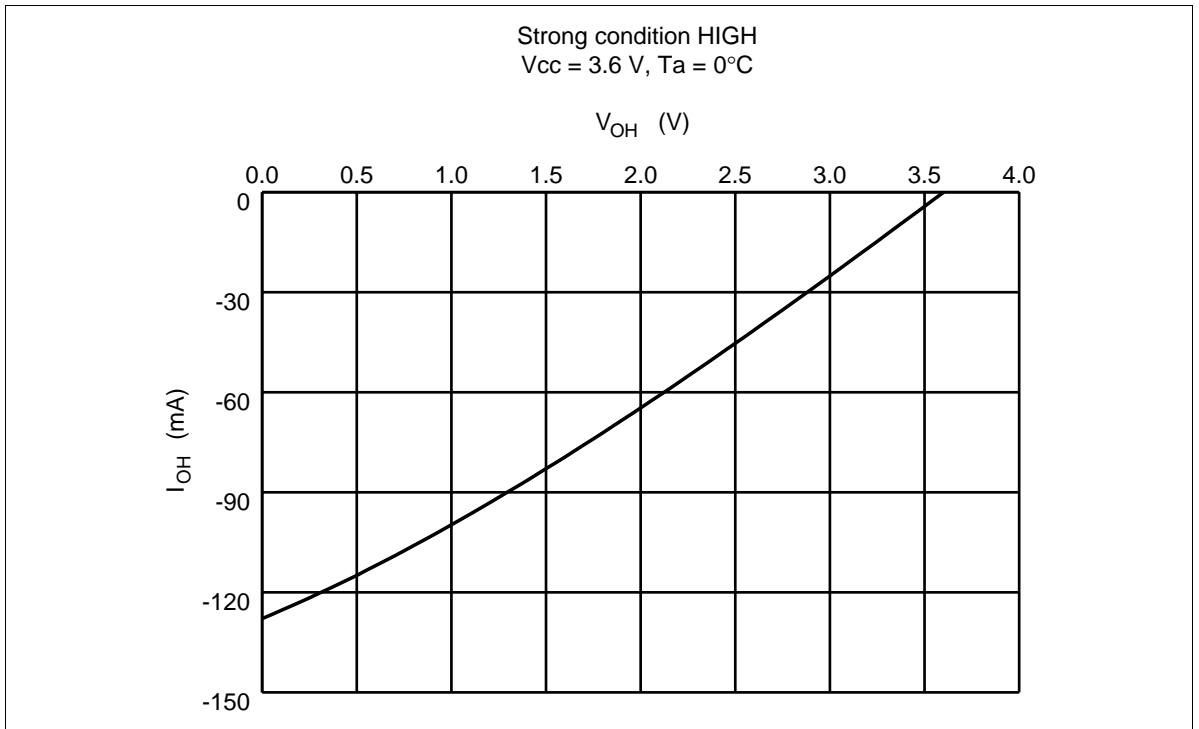
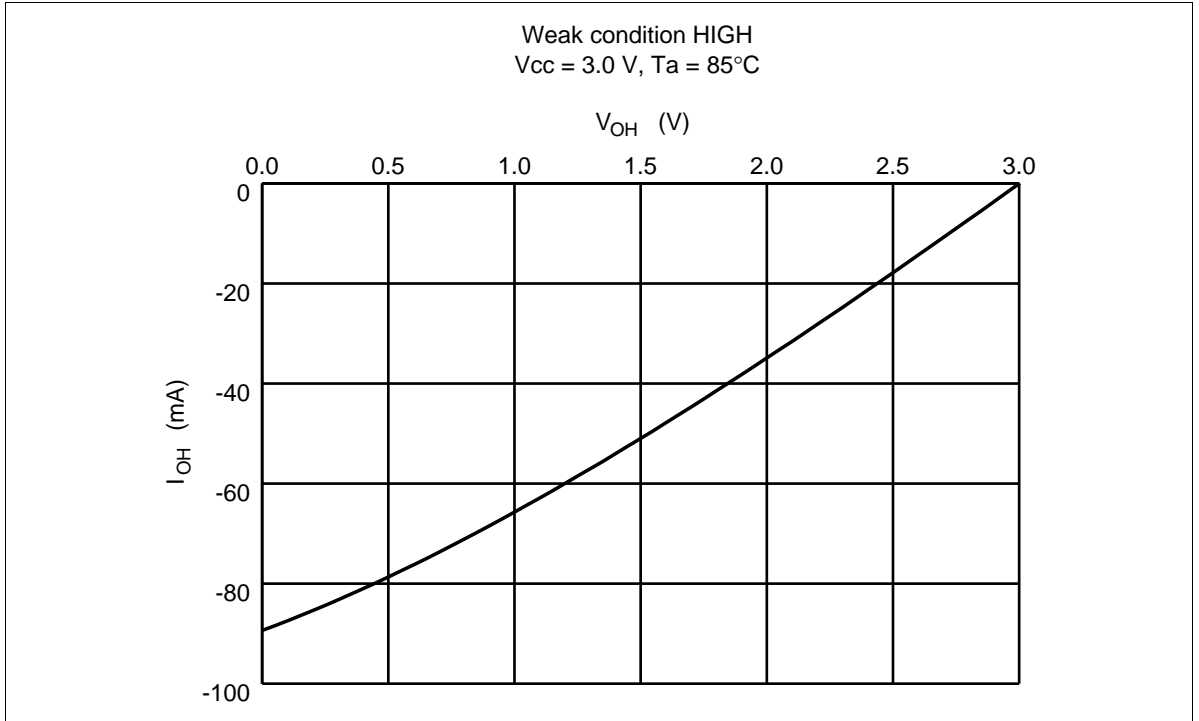
## Waveforms – 3



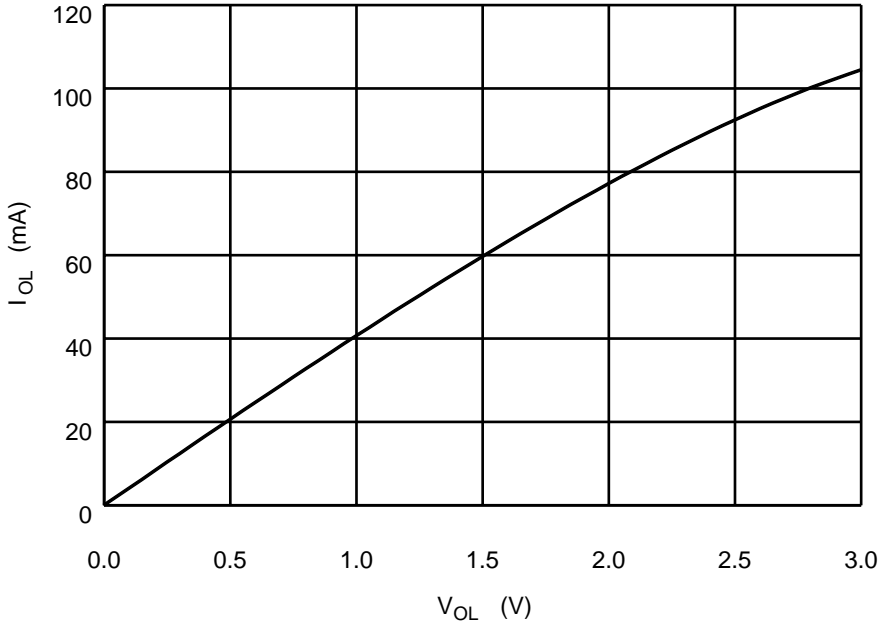
TEST	$V_{CC}=2.5\pm 0.2V$	$V_{CC}=2.7V, 3.3\pm 0.3V$
$V_{IH}$	$V_{CC}$	2.7 V
$V_{ref}$	$1/2 V_{CC}$	1.5 V
$V_{ref1}$	$V_{OL} + 0.15 V$	$V_{OL} + 0.3 V$
$V_{ref2}$	$V_{OH} - 0.15 V$	$V_{OH} - 0.3 V$
$V_{OH1}$	$V_{CC}$	3.0 V
$V_{OL1}$	GND	GND

- Notes:
1. All input pulses are supplied by generators having the following characteristics :  
 $PRR \leq 10 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 2.0 \text{ ns}$ ,  $t_f \leq 2.0 \text{ ns}$ . ( $V_{CC} = 2.5\pm 0.2 \text{ V}$ )  
 $PRR \leq 10 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ . ( $V_{CC} = 2.7 \text{ V}, 3.3\pm 0.3 \text{ V}$ )
  2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
  3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
  4. The output are measured one at a time with one transition per measurement.

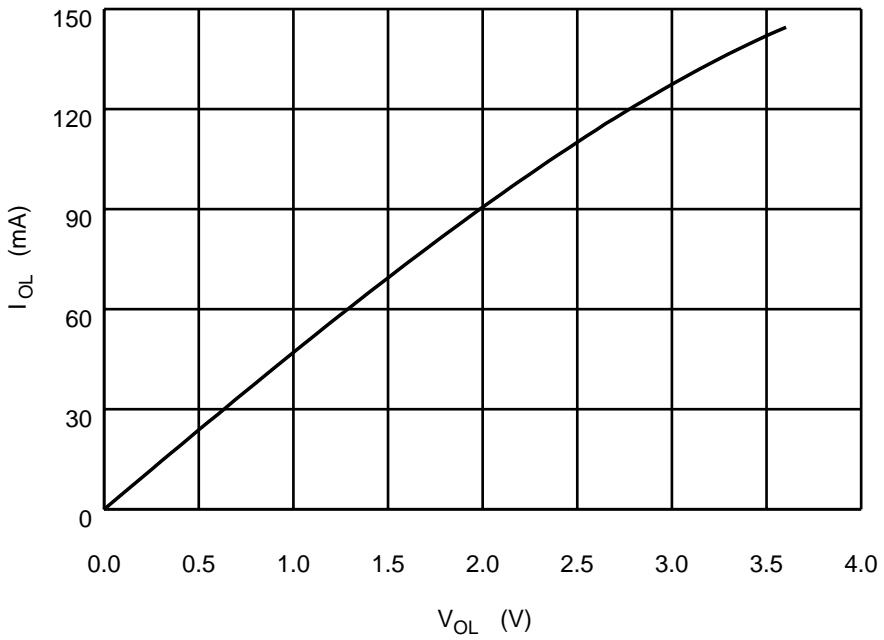
IV Characteristics for Register Output (Measured value)



Weak condition LOW  
 $V_{CC} = 3.0\text{ V}$ ,  $T_a = 85^\circ\text{C}$

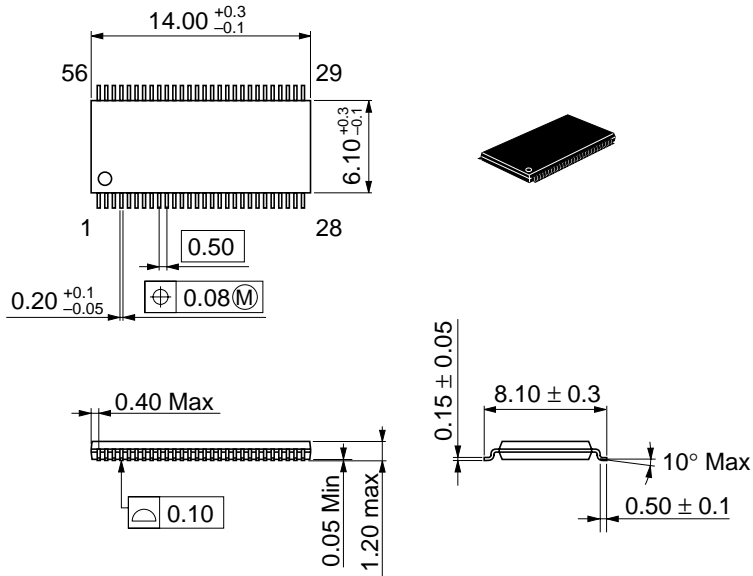


Strong condition LOW  
 $V_{CC} = 3.6\text{ V}$ ,  $T_a = 0^\circ\text{C}$



Package Dimensions

Unit : mm



Hitachi code	TTP-56D
EIAJ code	—
JEDEC code	—

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# HITACHI

## Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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## For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive,  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1> (408) 433-0223

Hitachi Europe GmbH  
Electronic components Group  
Dornacher Straße 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Group.  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.  
16 Collyer Quay #20-00  
Hitachi Tower  
Singapore 049318  
Tel: 535-2100  
Fax: 535-1533

Hitachi Asia Ltd.  
Taipei Branch Office  
3F, Hung Kuo Building, No.167,  
Tun-Hwa North Road, Taipei (105)  
Tel: <886> (2) 2718-3666  
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower, World Finance Centre,  
Harbour City, Canton Road, Tsim Sha Tsui,  
Kowloon, Hong Kong  
Tel: <852> (2) 735 9218  
Fax: <852> (2) 730 0281  
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