LinkSwitch®-HF
Design Guide
Application Note AN-38

Introduction

The *LinkSwitch-HF* family is designed for low power adapters and chargers (cell/cordless phones, PDAs, digital cameras, portable audio etc), as well as auxiliary supplies employed in applications such as white goods.

LinkSwitch-HF combines a high voltage power MOSFET switch with an ON/OFF controller in one device. It is completely self-powered from the DRAIN pin, has a jittered switching frequency for low EMI and is fully fault protected. Auto-restart limits device and circuit dissipation during overload and output short circuit conditions while hysteretic over-temperature protection disables the internal MOSFET during thermal faults. *EcoSmart®* technology enables designs to easily attain <300 mW no-load consumption, meeting worldwide energy efficiency requirements.

Scope

This application note is for engineers designing an isolated AC-DC flyback power supply using the *LinkSwitch-HF* family of devices. It provides guidelines to enable an engineer to quickly select key components and complete a transformer design for an application requiring either a constant voltage (CV) or constant voltage and constant current (CV/CC) output. To simplify the task of transformer design, this application note refers directly to the *PIXls* design spreadsheet that is part of the *PI Expert™* design software suite.

In addition to this application note the reader may also find the *LinkSwitch-HF* Design Accelerator Kit (DAK) containing an engineering prototype board, engineering report and device samples useful as an example of a working CV/CC supply. Further details on downloading *PI Expert*, obtaining a DAK and updates to this document can be found at *www.powerint.com.*

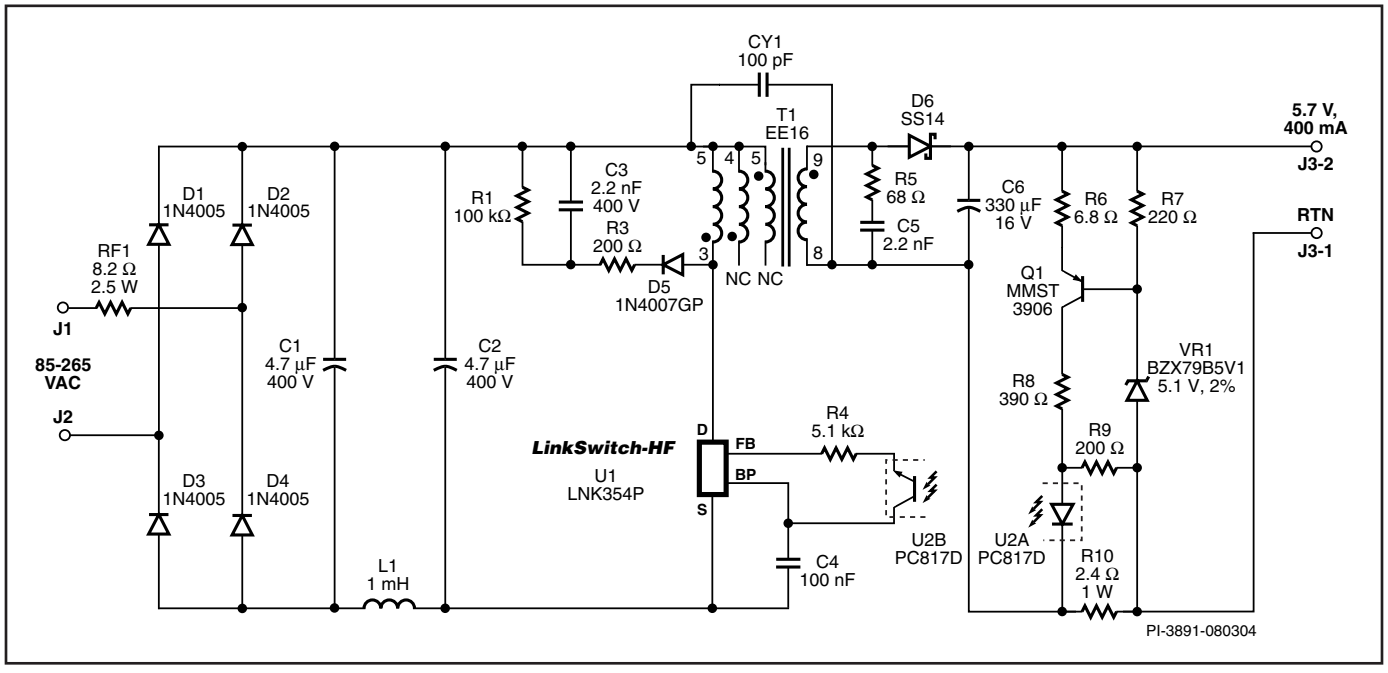


Figure 1. Basic Configuration Using LinkSwitch-HF in a CV/CC Application.

Quick Start

Readers wanting to start immediately can use the following information to quickly produce the first transformer design and select the components for a first prototype. Only the information below needs to be entered into the spreadsheet. Other parameters will be automatically filled in based on a typical design.

- Enter AC input voltage range
- Enter output voltage
- Enter output current
  $I_{O(TYP)}$ for CV/CC designs
  $I_{O(MAX)}$ for CV only designs
- Enter CC sense threshold voltage
  0.6 V for transistor V_{BE} sense where CC control to 0 V is not required
  1.1 V for optocoupler V_F sense or V_{BE} sense where CC control to 0 V is required
  0 for CV only designs
- Enter efficiency estimate
  0.57 for CV/CC designs
  0.7 for CV only designs
- Enter C_{IN}
  1 µF/W single 230 VAC
  3 µF/W universal or 100/115 VAC
- Select *LinkSwitch-HF*
  3 W universal / 4 W 230 VAC: LNK353
  4.5 W universal / 5 W 230 VAC: LNK354
- Enter V_D
  0.5 V for Schottky diode
  1 V for PN diode
- Enter core type if suggested core is not suitable
  Select using Table 3 guidance
- Build transformer
- Select key components
  See Steps 5 through 10.
- Build prototype and iterate design as necessary, entering measured values into spreadsheet where estimates were used (e.g. efficiency).

Step-by-Step Transformer Design Procedure

Step 1 – Enter Application Variables VAC_{MIN}, VAC_{MAX}, f_L, V_O, I_O, CC Threshold, η, Z, t_C, C_{IN}

Determine the input voltage range from Table 1.

Nominal Input Voltage	VAC_{MIN}	VAC_{MAX}
100/115	85	132
230	195	265
Universal	85	265

Table 1. Standard Worldwide Input Line Voltage Ranges.

Line Frequency, f_L (50 Hz or 60 Hz)
For half-wave rectification use $f_L/2$.

Output Current, I_O (A)
For CV/CC designs this should be the maximum output current at the maximum peak power point in the output characteristic (see Figure 3). For CV only outputs this should be the maximum output current. In multiple output designs, the output current of the main output (typically the output from which feedback is taken) should be increased such that P_O matches the sum of the output power from all the outputs in the design. The individual output voltages and currents should then be entered at the bottom of the spreadsheet (see Figure 4).

Output Voltage, V_O (V)
For CV/CC designs this should be the typical output voltage at the nominal peak power point in the output characteristic (see Figure 3). For CV only outputs this should be the specified output voltage.

CC Threshold Voltage (V)
For CV only designs this is not applicable; enter 0. For CV/CC designs this is the expected voltage developed across the current sense resistor at the nominal CC point. Typically this value is in the range of 1 V to 1.3 V, even for designs using the V_{BE} of a bipolar transistor (0.6 V to 0.7 V) as the CC reference voltage. In this case, to maintain CC control, the opto LED has to stay forward biased, requiring an additional resistor to be added in series with the CC sense resistor to increase the overall voltage drop. For the exact forward drop of the opto LED consult the manufacturer's data sheet.

	A	B	D	F	G	I
2	**ENTER APPLICATION VARIABLES**					
3	VACMIN	85			Volts	Minimum AC Input Voltage
4	VACMAX	265			Volts	Maximum AC Input Voltage
5	fL	50			Hertz	AC Mains Frequency
6	VO	5.5			Volts	Output Voltage
7	IO	0.5			Amps	Power Supply Output Current
8	CC Threshold Voltage	1			Volts	Voltage drop across sense resistor. For CV only circuits enter "0"
9	PO			3.25	Watts	Output Power
10	n	0.57				Efficiency Estimate. For CV only designs enter 0.7 if no better data available
11	Z			0.75		Loss Allocation Factor
12	tC	3			mSeconds	Bridge Rectifier Conduction Time Estimate
13	CIN	9.4			uFarads	Input Capacitance

Figure 2. Application Variable Section of LinkSwitch-HF Design Spreadsheet.

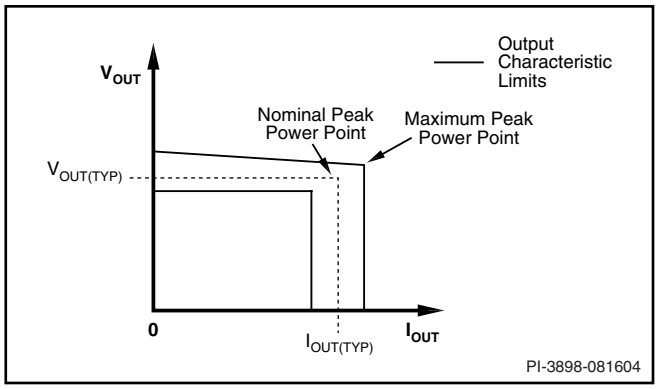


Figure 3. Diagram Showing Correct Values of I_o and V_o to Enter for CV/CC Designs.

Power Supply Efficiency, η

This is the complete power supply efficiency measured at the point of load, therefore including any CC sense and cable losses. For a CV/CC design with a nominal peak power point at a voltage of 5.5 V and current of 0.5 A, use a value of 0.57. Use a value of 0.7 for a 5.5 V CV only design if no better data is available.

Power Supply Loss Allocation Factor, Z

This factor represents the proportion of losses between the primary and the secondary of the power supply. If no better data is available this entry may be left empty and default values of 0.5 for CV only designs and 0.75 for CV/CC will be used. The higher number indicates larger secondary-side losses associated with the current sense resistor.

Bridge Diode Conduction Time, t_C (ms)

Enter a bridge diode conduction time of 3 ms if no other data is available.

Total Input Capacitance, C_{IN} (µF)

Enter total input capacitance using Table 2 for guidance.

	Total Input Capacitance per Watt of Output Power (µF/W)	
AC Input Voltage (VAC)	**Half Wave Rectification**	**Full Wave Rectification**
100/115	6-8	3-4
230	1-2	1
85-265	6-8	3-4

Table 2. Suggested Total Input Capacitance for Different Input Voltage Ranges.

	A	B	D	F	G	I
82	**TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)**					
83	**1st output**					
84	VO1			5.5	Volts	Output Voltage (if unused, defaults to single output design)
85	IO1			0.591	Amps	Output DC Current
86	PO1			3.25	Watts	Output Power
87	VD1			0.5	Volts	Output Diode Forward Voltage Drop
88	NS1			12.83		Output Winding Number of Turns
89	ISRMS1			1.273	Amps	Output Winding RMS Current
90	IRIPPLE1			1.13	Amps	Output Capacitor RMS Ripple Current
91	PIVS1			36	Volts	Output Rectifier Maximum Peak Inverse Voltage
92						
93	CMS1			255	Cmils	Output Winding Bare Conductor minimum circular mils
94	AWGS1			26	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
95	DIAS1			0.41	mm	Minimum Bare Conductor Diameter
96	ODS1			0.67	mm	Maximum Outside Diameter for Triple Insulated Wire
97						
98	**2nd output**					
99	VO2				Volts	Output Voltage
100	IO2				Amps	Output DC Current
101	PO2			0.00	Watts	Output Power
102	VD2				Volts	Output Diode Forward Voltage Drop
103	NS2			0.00		Output Winding Number of Turns
104	ISRMS2			0.000	Amps	Output Winding RMS Current
105	IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
106	PIVS2			0	Volts	Output Rectifier Maximum Peak Inverse Voltage
107						
108	CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
109	AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
110	DIAS2			N/A	mm	Minimum Bare Conductor Diameter
111	ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
112						
113	**3rd output**					
114	VO3				Volts	Output Voltage
115	IO3				Amps	Output DC Current
116	PO3			0.00	Watts	Output Power
117	VD3				Volts	Output Diode Forward Voltage Drop
118	NS3			0.00		Output Winding Number of Turns
119	ISRMS3			0.000	Amps	Output Winding RMS Current
120	IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
121	PIVS3			0	Volts	Output Rectifier Maximum Peak Inverse Voltage
122						
123	CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
124	AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
125	DIAS3			N/A	mm	Minimum Bare Conductor Diameter
126	ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
127						
128	**Total power**			3.25	Watts	Total Output Power

Figure 4. Multiple Output Transformer Secondary Design Parameters.

	A	B	D	F	G	I
39	**DC INPUT VOLTAGE PARAMETERS**					
40	VMIN			82	Volts	Minimum DC Input Voltage
41	VMAX			375	Volts	Maximum DC Input Voltage

Figure 5. DC-Input Voltage Parameters Showing Grey Override Cells for DC Input Designs.

	A	B	D	F	G	I
15	**ENTER LinkSwitch-HF VARIABLES**					
16	**LinkSwitch-HF**	LNK354			*Universal*	*115 Doubled/230V*
17	*Chosen Device*		*LNK354*	*Power Out*	*4.5 W*	*5 W*
18	ILIMITMIN			*0.233*	Amps	Minimum Current Limit
19	ILIMITMAX			*0.268*	Amps	Maximum Current Limit
20	fS			*186000*	Hertz	Minimum Device Switching Frequency
21	fS Full Load			186000	Hertz	
22	VOR			80	Volts	Reflected Output Voltage
23	VDS			10	Volts	LinkSwitch-HF on-state Drain to Source Voltage
24	VD			0.5	Volts	Output Winding Diode Forward Voltage Drop
25	KP			0.72		Ripple to Peak Current Ratio (0.6<KRP<1.0 : 1.0<KDP<6.0)

Figure 6. LinkSwitch-HF Section of Design Spreadsheet.

The capacitance should be selected to keep the minimum DC input voltage, V_{MIN} >70 V and ideally >90 V.

Note: For designs that have a DC rather than an AC input, the value of the minimum and maximum DC input voltages, V_{MIN} and V_{MAX}, may be entered directly into the override cells on the design spreadsheet (see Figure 5).

Step 2 – Enter *LinkSwitch-HF* Variables: *LinkSwitch-HF* Device, f_S Full Load, V_{OR}, V_{DS}, V_D, K_P

To select the correct *LinkSwitch-HF* device, refer to the *LinkSwitch-HF* data sheet power table and select based on the output power of the design.

f_S Full Load Switching Frequency (Hz)
This parameter is the worst-case maximum effective switching frequency at full load. By default, if the grey override cell is left empty, a value of 186 kHz is assumed. This value is the minimum data sheet switching frequency and should be used to obtain the maximum power from the selected device.

For designs that require an output power below the maximum capability of the selected *LinkSwitch-HF* device, entering a lower value for full load switching frequency can simplify design or size of EMI filter components. Reducing the effective full load frequency increases the calculated value of the primary inductance and also increases the maximum overload power. This should be considered especially in CV only designs where the overload power is not limited by a secondary-side current limit.

In general, start the design with the default value of 186 kHz. At the end of the design reduce the value until a limit of another parameter is reached (typically K_P, CMA or B_M if a fixed number of secondary turns, N_S, has been entered).

Reflected Output Voltage, V_{OR} (V)
This parameter is the secondary winding voltage during the diode conduction time reflected back to the primary through the turns ratio of the transformer. The default value is 80 V, however this can be increased up to 120 V to achieve the maximum power capability from the selected *LinkSwitch-HF* device. In general, start with the default value of 80 V, increasing the value when necessary to maintain K_P above its lower limit of 0.6.

***LinkSwitch-HF* On-State Drain to Source Voltage, V_{DS} (V)**
This parameter is the average on-state voltage developed across the DRAIN and SOURCE pins of *LinkSwitch-HF*. By default, if the grey override cell is left empty, a value of 10 V is assumed. Use the default value if no better data is available.

Output Diode Forward Voltage Drop, V_D (V)
Enter the average forward voltage drop of the (main) output diode. Use 0.5 V for a Schottky diode or 1 V for a PN diode if no better data is available. By default, a value of 0.5 V is assumed.

Calculated Ripple to Peak Current Ratio, K_P
Below a value of 1, indicating continous conduction mode, K_P is the ratio of ripple to peak primary current (K_{RP}). Above a value of 1, indicating discontinuous conduction mode, K_P is the ratio of primary MOSFET off-time to the secondary diode conduction time (K_{DP}). The value of K_P should be in the range of $0.6 < K_P < 6$ and guidance is given in the comments cell if the value is outside this range.

Step 3 – Choose Core and Bobbin Based on Output Power and Enter A_e, L_e, A_L, BW, M, L, N_S

Core Effective Cross-Sectional Area, A_e (cm^2)
Core Effective Path Length, L_e (cm)
Core Ungapped Effective Inductance, A_L ($nH/turn^2$)
Bobbin Width, BW (mm)

By default, if the Core Type cell is left empty, the spreadsheet will select the smallest commonly available core suitable for the output power as shown in Table 3. The values shown are

	A	B	D	F	G	I
27	**ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES**					
28	**Core Type**			EE16		Suggested smallest commonly available core
29	*Core*		*EE16*		*P/N:*	PC40EE16-Z
30	*Bobbin*		*EE16_BOBBIN*		*P/N:*	EE16_BOBBIN
31	AE			0.192	cm^2	Core Effective Cross Sectional Area
32	LE			3.5	cm	Core Effective Path Length
33	AL			1140	nH/T^2	Ungapped Core Effective Inductance
34	BW			8.6	mm	Bobbin Physical Winding Width
35	M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
36	L			3		Number of Primary Layers
37	NS			14		Number of Secondary Turns

Figure 7. Transformer Core and Construction Variables Section of Spreadsheet.

based on an assumed output voltage of 5.5 V, 4 primary layers and the default input parameters as described in Step 1. Changes to these values will change the power capability of a given core size, therefore Table 3 should be used for guidance only.

Core Size	Commonly Used	Suggested Power Range	
		100/115 or 85-265 VAC	230 VAC Only
EE8	No	< 1.5 W	< 2 W
EP10	No	< 1.75 W	< 3 W
EE10	No	< 2.5 W	< 3.75 W
EF12.6	Yes	< 2.5 W	< 4 W
EE13	Yes	< 3.5 W	< 4.5 W
EE16	Yes	< 3.9 W	< 5 W
EE1616	Yes	< 4 W	< 5 W
EE19	Yes	< 4.25 W	< 5 W
EF20	Yes	< 5 W	< 5 W
EF25	Yes	< 5 W	< 5 W

Table 3. Suggested Power Levels for Typical Core Sizes Used in a LinkSwitch-HF Design.

The gray override cells can be used to enter the core and bobbin parameters directly. This is useful if a core is selected that is not on the list or the specific core or bobbin information differs from that recalled by the spreadsheet (see Figure 7).

Safety Margin, M (mm)
For designs that require isolation but are not using triple insulated wire for the secondary winding, the width of the safety margin to be used on each side of the bobbin should be entered here. Typically, for universal input designs, a total margin of 6.2 mm would be required, therefore a value of 3.1 mm would be entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical.

As the margin reduces the available area for the windings, margin construction may not be suitable for small core sizes. If after entering the margin more than 4 primary layers (L) are required, it is suggested that either a larger core be selected or switch to a zero margin design using triple insulated wire for the secondary winding.

Primary Layers, L
By default, if the override cell is empty, a value of 3 is assumed. Primary layers should be in the range of $1 < L < 4$, and in general it should be the lowest number that meets the primary current density limit (CMA) of 200 Cmils/Amp. Values above 4 layers are possible, but the increased leakage inductance and physical fit of the windings should be considered.

Secondary Turns, N_S
By default, if the grey override cell is left blank, the minimum number of secondary turns is calculated such that the maximum operating flux density, B_M, is kept below the recommended maximum. In general, it is not necessary to enter a number in the override cell except in designs where a higher operating flux density is acceptable (see Audible Nose section for an explanation of B_M limits).

Step 4 – Iterate Transformer Design and Generate Transformer Design Output

Iterate the design making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column.

Once all warnings have been cleared, the output transformer design parameters can be used to either wind a prototype transformer or send to a vendor for samples.

The Key Transformer Electrical Parameters Are:

Primary Inductance, L_P (µH)
This is the target nominal primary inductance of the transformer.

Primary Inductance Tolerance, $L_{P\_TOLERANCE}$ (%)
This is the assumed primary inductance tolerance. A value of 12% is used by default, however if specific information is known from the transformer vendor, then this may be overridden by entering a new value in the grey override cell.

Number of Primary Turns, N_P
Primary Wire Size, DIA (mm)
Primary Wire Gauge, AWG
Number of Primary Layers, L

	A	B	D	F	G	I
50	**TRANSFORMER PRIMARY DESIGN PARAMETERS**					
51	LP			1207	uHenries	Typical Primary Inductance. +/- 12%
52	LP TOLERANCE			12	%	
53	NP			160		Primary Winding Number of Turns
54	ALG			47	nH/T^2	Gapped Core Effective Inductance
55	BM			1218	Gauss	Maximum Operating Flux Density, BM<1250 is recommended
56	BAC			511	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
57	ur			1654		Relative Permeability of Ungapped Core
58	LG			0.49	mm	Gap Length (Lg > 0.1 mm)
59	BWE			25.8	mm	Effective Bobbin Width
60	OD			0.16	mm	Maximum Primary Wire Diameter including insulation
61	INS			0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
62	DIA			0.12	mm	Bare conductor diameter
63	AWG			37	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
64	CM			20	Cmils	Bare conductor effective area in circular mils
65	CMA			203	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)

Figure 8. Transformer Primary Design Parameters Section of Spreadsheet.

	A	B	D	F	G	I
67	**TRANSFORMER SECONDARY DESIGN PARAMETERS**					
68	**Lumped parameters**					
69	ISP			2.66	Amps	Peak Secondary Current
70	ISRMS			1.08	Amps	Secondary RMS Current
71	IRIPPLE			0.95	Amps	Output Capacitor RMS Ripple Current
72	CMS			215	Cmils	Secondary Bare Conductor minimum circular mils
73	AWGS			26	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
74	DIAS			0.41	mm	Secondary Minimum Bare Conductor Diameter
75	ODS			0.61	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
76	INSS			0.10	mm	Maximum Secondary Insulation Wall Thickness

Figure 9. Transformer Secondary Design Parameters Section of Spreadsheet.

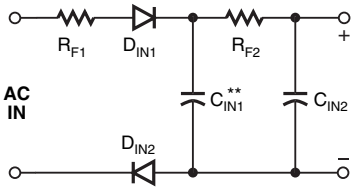
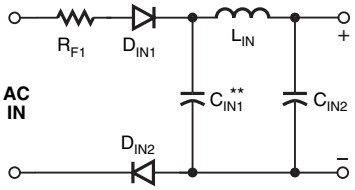
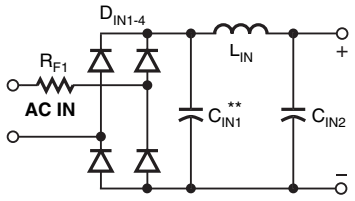
P_{OUT}	≤ 1 W	> 1 W	
Suggested 85-265 VAC Input Stage	 PI-3772-121603	 PI-3773-121603	 PI-3774-121603
Component Selection Guide	R_{F1}: 8.2 Ω, 1 W Fusible R_{F2}: 100 Ω, 0.5 W, Flame-proof C_{IN1}, C_{IN2}: ≥ 3.3 µF, 400 V each D_{IN1}, D_{IN2}: 1N4007, 1 A, 1000 V	R_{F1}: 8.2 Ω, 1 W Fusible L_{IN}: 470 µH-2.2 mH, 0.05 A-0.3 A C_{IN1}, C_{IN2}: ≥ 4 µF/W_{OUT}, 400 V each D_{IN1}, D_{IN2}: 1N4007, 1 A, 1000 V	R_{F1}: 8.2 Ω, 1 W Fusible L_{IN}: 470 µH-2.2 mH, 0.05 A-0.3 A C_{IN1}, C_{IN2}: ≥ 2 µF/W_{OUT}, 400 V each D_{IN1}-D_{IN4}: 1N4007, 1 A, 1000 V
Comments	**Increase value to meet required differential line surge performance.		

Table 4. Suggested AC Input Stages.

Gapped Core Effective Inductance, A_{LG} (nH/T^2)
Estimated Core Center Leg Gap Length: L_g (mm)
Number of Secondary Turns, N_s
Secondary Wire Size, DIA_S (mm)
Secondary Wire Gauge, AWG_S

Step 5 – Selection of Input Stage

The input stage comprises fusible resistor(s), input rectification diodes and line filter network. The fusible resistor should be chosen as flame-proof and depending on the differential line input surge requirements, a wire-wound type may be required. The fusible resistor(s) provides fuse safety, inrush current limiting and differential mode noise attenuation.

The differential mode EMI filter impedance (either a resistor or inductor) is placed such that there is no impedance between the input stage, the Y capacitor and the secondary (assuming Y capacitor placement between the secondary return and the DC rail).

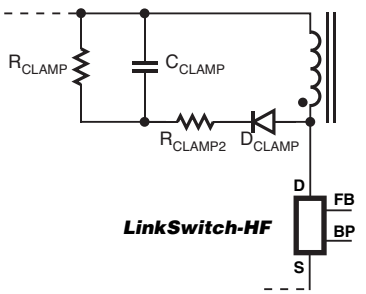
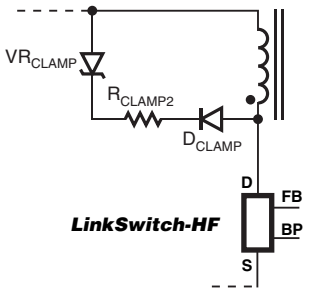
Type	RCD	Zener
Suggested Primary Clamp	 PI-3893-062504	 PI-3894-062504
Advantages	• Lower cost • Lower EMI	• Lower parts count • Lower no-load consumption
Component Selection Guide	• D_{CLAMP} (1 A, 600 V) - UF4005, 1N3947 or 1N4007GP - 1N4007 improves EMI and efficiency but must be glass passivate type (1N4007GP) • R_{CLAMP2} - Not necessary when using ultra-fast (UF4005) or fast diode (1N3947) - A value in the range of 50 Ω to 330 Ω, 1/4 W should be used with a slow diode (1N4007GP) to limit reverse pull out current	
	• R_{CLAMP} - 47 kΩ to 200 kΩ, 1/4 W or 1/2 W • C_{CLAMP} - 390 pF to 2.2 nF, ≥ 400 V ceramic or film (Note ceramic capacitors may create audible noise)	• VR_{CLAMP} - Select voltage to be 1.5 • V_{OR} with a power rating of 0.5 W to 1 W (P6Kexxx and BZY97Cxxx series are good examples of suitable Zener diodes)

Table 5. Suggested Primary Clamp Configurations.

For designs ≤1 W it is lower cost to use half-wave rectification and >1 W, full-wave rectification (smaller input capacitors). The EMI performance of half-wave rectified designs is improved by adding a second diode in the lower return rail. This provides EMI gating (EMI currents only flow when the diode is conducting) and also doubles the differential surge withstand as the surge voltage is shared across two diodes. Table 4 shows the recommended input stage based on output power for a universal input design while Table 2 shows how to adjust the input capacitance for other input voltage ranges.

Step 6 – Selection of *LinkSwitch-HF* External Components

- For the BYPASS pin capacitor use a 0.1 µF, 50 V ceramic capacitor.
- To prevent load transients from saturating the feedback loop and discharging the BP pin capacitor, place a 5.1 kΩ, 5%, 1/8 W resistor in series between the BP pin and the optocoupler transistor (see Figure 1).

Step 7 – Selection of Primary Clamp Components

Select the initial clamp components using Table 5 as a guide. If an RCD clamp is selected then some empirical adjustment of the values is normally required to take account of the actual V_{OR} and transformer leakage inductance of the design. As a general rule minimize the value of the capacitor and maximize the value of the resistor. For both RCD and Zener clamps, verify that the V_{DS} does not exceed 675 V at the highest input voltage and peak (overload) output power.

Step 8 – Select Output Rectifier Per Table 6

$V_R \geq 1.25 \cdot PIV_S$: where PIV_S is taken from the Voltage Stress Parameters section of the spreadsheet and Transformer Secondary Design Parameters (Multiple Outputs).

$I_D \geq 2 \cdot I_O$: where I_D is the diode rated DC current and I_O is the output current.

Series Number	Type	V_R Range	I_F	Package	Manufacturer
		V	A		
1N5817 to 1N5819	Schottky	20-40	1	Leaded	Vishay
SB120 to SB1100	Schottky	20-100	1	Leaded	Vishay/Fairchild
11DQ50 to 11DQ60	Schottky	50-60	1	Leaded	IR
1N5820 to 1N5822	Schottky	20-40	3	Leaded	Vishay
MBR320 to MBR360	Schottky	20-60	3	Leaded	IR/On Semi
SS12 to SS16	Schottky	20-60	1	SMD	Vishay
SS32 to SS36	Schottky	20-60	3	SMD	Vishay
UF4002 to UF4006	Ultrafast	100-600	1	Leaded	Vishay
MUR110 to MUR160	Ultrafast	100-600	1	Leaded	On Semi
UF5401 to UF5408	Ultrafast	100-800	3	Leaded	Vishay
ES1A to ES1D	Ultrafast	50-200	1	SMD	Vishay
ES2A to ES2D	Ultrafast	50-200	2	SMD	Vishay

Table 6. List of Diodes Suitable for use as the Output Rectifier.

Step 9 – Select Output Capacitor

Ripple Current Specification at Maximum Capacitor Operating Temperature (200 kHz)
Should be ≥ I_{RIPPLE} value from the design spreadsheet Transformer Secondary Parameters section or, in multiple output designs, the Transformer Secondary Design Parameters (Multiple Outputs) section. Many capacitor manufacturers provide factors that increase the ripple current rating as the capacitor operating temperature is reduced from its data sheet maximum. This should be considered to ensure that the capacitor is not oversized for cost reasons.

ESR Specification
Use a low ESR, electrolytic capacitor. Output switching ripple is I_{SP} • ESR, where the value for I_{SP} is taken from the spreadsheet Transformer Secondary Parameters section or, in multiple output designs, the Transformer Secondary Design Parameters (Multiple Outputs) section.

Step 10 – Select Feedback Circuit Components

Applicable Reference Circuits
Refer to Table 7 for an example of a CV/CC and a CV only configuration. For additional examples see application circuits on the website at *www.powerint.com.*

Other Information

Audible Noise
The cycle skipping mode of operation used in *LinkSwitch-HF* can generate audio frequency components in the transformer. To limit this audible noise generation, the transformer should be designed such that the peak core flux density (B_M) is below 1250 Gauss (125 mT). Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. Higher flux densities are possible, however careful evaluation of the audible noise performance should be made using production transformer samples before approving the design.

Ceramic capacitors that use dielectrics, such as Z5U, when used in clamp circuits may also generate audio noise. If this is the case, try replacing them with a capacitor having a different dielectric, for example a polyester film type.

Tips for Reducing No-Load Consumption
To obtain the lowest no-load consumption follow these tips:

- Design for low V_{OR}
  - High values of V_{OR} (>80 V) will increase no-load consumption by increasing energy dissipation due to stray capacitance.
- Minimize transformer capacitance
  - Use double-coated (also known as heavy nyleze, or grade 2) magnetic wire for the primary winding. The thicker insulation increases the space between adjacent primary layers and therefore reduces the winding capacitance.
  - Add tape between the primary layers. The increased spacing reduces the capacitance between adjacent primary layers.
  - Do not vacuum impregnate. Use dip varnishing. The increase dielectric formed by the varnish when vacuum impregnated dramatically increases transformer capacitance.

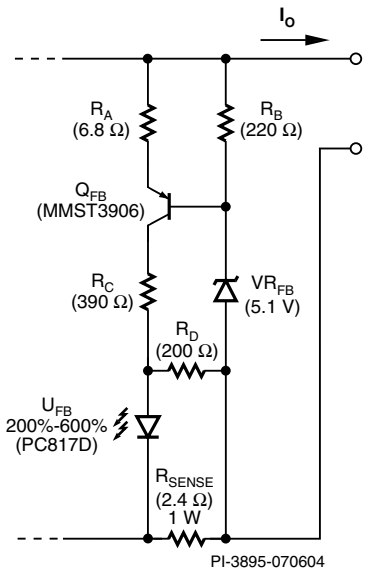
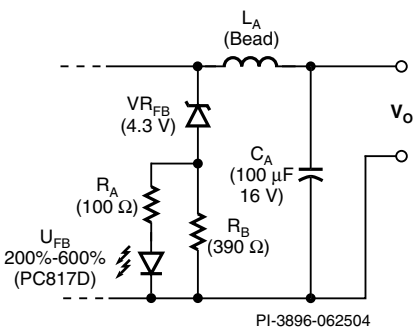
Output Type	CV/CC	CV Only
Suggested Feedback		
Notes	R_{SENSE}: $V_{F(UFB)}/I_O$ VR_{FB}: V_O-$V_{BE(QFB)}$ (Use a Zener with a low I_{ZT} such as the BZX79 series) R_B: $V_{BE(QFB)}/I_{ZT(VRFB)}$ R_A: Limits base-emitter current of Q_{FB} R_C and R_D: Limits U_{FB} current U_{FB}: Use high CTR device (200% - 600%) Q_{FB}: Any small signal PNP transistor (Values shown for a 5.5 V, 500 mA output)	VR_{FB}: V_O-$V_{F(UFB)}$ (Use a Zener with a low I_{ZT} such as the BZX79 series) R_B: $V_{F(UFB)}/I_{ZT(VRFB)}$ R_A: Limits U_{FB} current during transients and allows small output voltage adjustments. U_{FB}: Use high CTR device (200% - 600%) L_A: Optional for lower output switching noise (Use ferrite bead or low value (1-3 µH) inductor rated for I_O) C_A: Optional for lower output switching noise (Use low ESR, 100 µF with voltage rating >1.25 • V_O) (Values shown are for a 5 V output)

Table 7. Examples of Feedback Configurations.

- Optimize the primary clamp
  - If using an RCD clamp ensure that the smallest value of capacitor and largest value of resistor have been used while still keeping the peak drain voltage safely below BV_{DSS}. Consider using a Zener clamp.

Layout Guidelines

See data sheet for layout guidelines.

Quick Design Checklist

See data sheet for quick design checklist.

Tolerancing Assumptions

By default the design spreadsheet calculates the value for primary inductance assuming the following tolerances.

- Minimum *LinkSwitch-HF* data sheet current limit at lower di/dt value
- Minimum *LinkSwitch-HF* data sheet switching frequency
- Worst case transformer primary inductance tolerance ($L_{P\_TOLERANCE}$)
- Typical V_O and maximum I_O in designs with secondary CC control, typical V_O and maximum I_O in CV only designs

These are suggested as being suitable for most cost effective CV/CC designs and all CV designs. If further design margin is required in CV/CC designs then the maximum V_O value should be used.

Notes

Notes

Revision	Notes	Date
A	-	10/04

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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

CHINA (SHANGHAI)
Rm 807-808A, Pacheer
Commercial Centre
555 Nanjing West Road
Shanghai, 200041, China
Phone: +86-21-6215-5548
Fax: +86-21-6215-2468
e-mail: chinasales@powerint.com

CHINA (SHENZHEN)
Rm 2206-2207, Block A,
Electronics Science & Technology Bldg.,
2070 Shennan Zhong Road,
Shenzhen, Guangdong,
China, 518031
Phone: +86-755-8379-3243
Fax: +86-755-8379-5828
e-mail: chinasales@powerint.com

GERMANY
Rueckertstrasse 3
D-80336, Muenchen, Germany
Phone: +49-895-527-3910
Fax: +49-895-527-3920
e-mail: eurosales@powerint.com

INDIA (TECHNICAL SUPPORT)
Innovatech
261/A, Ground Floor
7th Main, 17th Cross,
Sadashivanagar
Bangalore, India 560080
Phone: +91-80-5113-8020
Fax: +91-80-5113-8023
e-mail: indiasales@powerint.com

ITALY
Via Vittorio Veneto 12,
Bresso
Milano, 20091, Italy
Phone: +39-028-928-6001
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

JAPAN
Keihin-Tatemono 1st Bldg.
12-20 Shin-Yokohama
2-Chome,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033, Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

KOREA
RM 602, 6th Floor
Korea City Air Terminal B/D, 159-6,
Samsung-Dong, Kangnam-Gu,
Seoul, Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@powerint.com

SINGAPORE
51 Newton Road
#15-08/10 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

TAIWAN
5F-1, No. 316, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei, Taiwan 114, R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@powerint.com

UK (EUROPE & AFRICA HEADQUARTERS)
1st Floor, St. James's House
East Street
Farnham, Surrey GU9 7TJ
United Kingdom
Phone: +44 (0) 1252-730-140
Fax: +44 (0) 1252-727-689
e-mail: eurosales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760