

# Application Note AN-42

## TinySwitch-PK Family



### Design Guide

#### Introduction

The TinySwitch-PK family is a highly integrated monolithic off-line switcher IC designed for off-line power supplies where short duration peak power is required. By increasing the current limit and switching frequency during peak loads, the designer is able to meet the output power requirement without requiring a larger device or transformer. Examples applications include DVD players, set-top decoders, active speakers (e.g., MP3 docking stations), audio amplifiers, modems, and photo and thermal printers. Innovative features such as on-time extension, latching output overvoltage shut down, selectable current limit, and line undervoltage greatly simplify the design, reducing engineering design time and system cost while providing complete system level protection.

The ICs combine a high voltage power MOSFET switch with an ON/OFF controller in one device. Internal start-up bias current is drawn from the DRAIN pin, eliminating the need for external start-up components. Additional features include selectable internal current limit for design flexibility, jittered switching frequency for low EMI, and line undervoltage lock out to prevent output glitches during power up and down. Safety and reliability features include

auto-restart to limit device and overall circuit dissipation during overload, output short circuit and open loop conditions, latching output over voltage shutdown to protect the load, and hysteretic over-temperature protection to disable the supply during a thermal fault. On-time extension improves power delivery at low line as well as the hold-up time.

EcoSmart® technology enables designs to easily attain <170 mW no-load consumption without a bias winding or <60 mW, with both measured at 265 VAC. Together with a flat efficiency characteristic vs load, this makes meeting energy efficiency standards straightforward, including programs from Energy Star and California Energy Commission.

#### Scope

This application note is intended for engineers designing an isolated AC-DC flyback power supply using the TinySwitch-PK family of devices. It provides guidelines to enable an engineer to quickly select key components and also complete a suitable transformer design. To simplify the task, this application note refers directly to the PI XIs design spreadsheet that is part of the PI Expert™ design software suite.

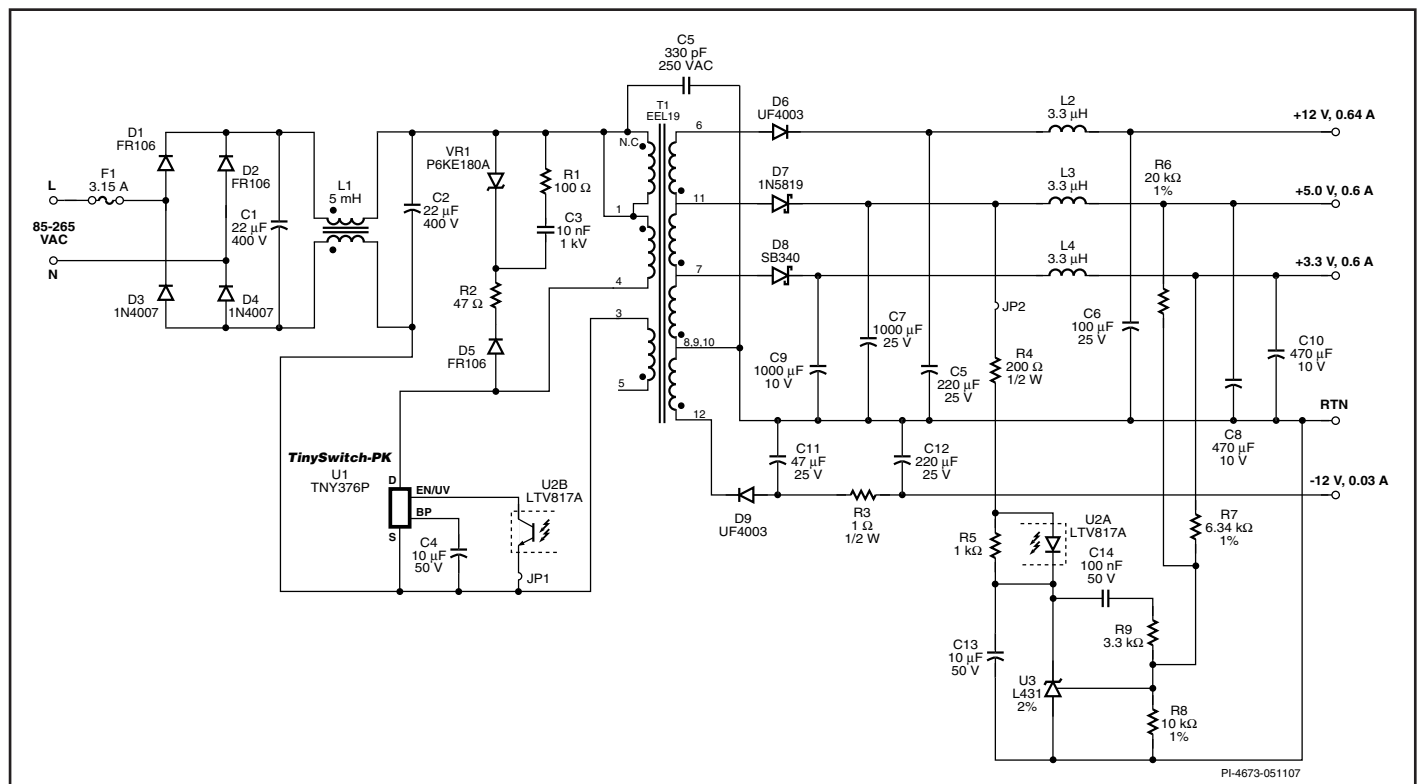


Figure 1. Four Output 7.5 W (13 W peak) Power Supply Using TinySwitch-PK.

In addition to this application note, the reader may also find the TinySwitch-PK Reference Design Kit (RDK), containing an engineering prototype board, engineering report, and device samples useful as an example of a working power supply. Further details on downloading PI Expert, obtaining a RDK, and updates to this document can be found at [www.powerint.com](http://www.powerint.com).

**Quick Start**

Readers willing to start immediately can use the following information to quickly design the transformer and select the components for a first prototype. Only the information described below needs to be entered into the spreadsheet. Other parameters will be automatically selected based on a typical design. References to spreadsheet cell locations are provided in brackets [ ].

- Enter AC input voltage range  $V_{AC_{MIN}}$ ,  $V_{AC_{MAX}}$  and minimum line frequency  $f_L$  [B3, B4, B5].
- Enter nominal output voltage  $V_o$  [B6].
- Enter peak load current [B7].
- Enter Continuous Power [B9].
- Enter efficiency estimate [B10]:  
0.7 for universal input voltage (85-265 VAC) or single 100/115 VAC (85-132 VAC) and 0.75 for a single 230 VAC (185-265 VAC) design. Adjust the number accordingly after measuring the efficiency of the first prototype-board at peak load and  $V_{AC_{MIN}}$ .
- Enter loss allocation factor Z [B11]:  
0.6 for typical application (adjust the number accordingly after first proto-board evaluation).
- Enter  $C_{IN}$  input capacitance [B13]:  
2  $\mu F/W_{PK}$  for universal (85-265 VAC) or single (100/115 VAC) line if output voltage droop is acceptable or 3  $\mu F/W_{PK}$  if output voltage droop is unacceptable during peak load. Use 1  $\mu F/W$  for single 230 VAC (185-265 VAC) line input. If this cell is left blank then the capacitance value for a  $V_{MIN}$  of 70 V (universal input) or 150 V (single 230 VAC) is calculated.

**Output Power Table**

Product <sup>3</sup>	230 VAC ± 15%			85-265 VAC		
	Adapter	Open Frame <sup>2</sup>	Peak	Adapter	Open Frame <sup>2</sup>	Peak
<b>TNY375 P</b>	8.5 W	15 W	16.5 W	6 W	11.5 W	12.5 W
<b>TNY376 P</b>	10 W	19 W	22 W	7 W	15 W	17 W
<b>TNY377 P</b>	13 W	23.5 W	28 W	8 W	18 W	23 W
<b>TNY378 P</b>	16 W	28 W	34 W	10 W	21.5 W	27 W
<b>TNY379 P</b>	18 W	32 W	39 W	12 W	25 W	31 W
<b>TNY380 P</b>	20 W	36.5 W	45 W	14 W	28.5 W	35 W

Table 1. Output Power Table. (see data sheet for notes)

- Select TinySwitch-PK from drop down list or enter directly [B16]:  
Select the device in the table below according to output power and line input voltage.

- Enter configuration current limit [B18]:  
STD for standard current limit  
RED for reduced current limit  
INC for increased current limit
- Enter core type (if desired) from drop down menu [B45]  
A suggested core size will be selected automatically if none is entered.
- Build transformer.
- Select key components (see Steps 7 through 12).
- Build prototype and iterate design as necessary, entering measured values into spreadsheet where estimates were used (e.g. efficiency,  $V_{MIN}$ ).

**Step-by-Step Transformer Design Procedure**

**Introduction**

TinySwitch-PK is optimized for use in applications that demand short duration, high peak power levels, but a significantly lower continuous or average power. During peak load conditions, the current limit and switching frequency of TinySwitch-PK are increased. This typically allows a smaller core size and TinySwitch-PK device to be selected to deliver the peak power, but the short duration prevents excessive device dissipation and oversizing of the transformer. Typical peak to continuous ratios are  $P_{PEAK} \leq 2 \times P_{AVE}$ .

As average power increases, based on the measured transformer and device temperature, it may be necessary to select a larger transformer to allow increased copper area for the windings or increase the amount of device heatsinking.

**Peak Output Power Table**

Product	230 VAC ± 15%			85-265 VAC		
	$I_{LIMIT-PEAKred}$	$I_{LIMITPEAK}$	$I_{LIMIT-PEAKinc}$	$I_{LIMIT-PEAKred}$	$I_{LIMITPEAK}$	$I_{LIMIT-PEAKinc}$
<b>•TNY375 P</b>	8.5 W	14.5 W	16.5 W	5.5 W	11.5 W	12.5 W
<b>TNY376 P</b>	10 W	19 W	22 W	6 W	15 W	17 W
<b>TNY377 P</b>	13 W	23 W	28 W	8 W	18 W	23 W
<b>TNY378 P</b>	16 W	27.5 W	34 W	10 W	21.5 W	27 W
<b>TNY379 P</b>	18 W	31.5 W	39 W	12 W	25 W	31 W
<b>TNY380 P</b>	20 W	36 W	45 W	14 W	28 W	35 W

Table 2. Peak Output Power Capability of TinySwitch-PK Family vs. Selected Current Limit

Table 1 provides both continuous (average) and peak power levels for each TinySwitch-PK family member at two line voltage ranges.

The values for Adapter and Open Frame represent practical, thermally limited, continuous output powers in two common thermal environments.

The values shown for Peak are limited electrically, based on minimum device  $I^2t$  and  $I_{LIMITPEAKinc}$  current limit mode.

For a complete list of the assumptions used, see the Applications section of the data sheet.

Table 2 provides peak power values at the two additional selectable current limit modes ( $I_{LIMITPEAKred}$  and  $I_{LIMITPEAK}$ ). The values for Adapter and Open Frame (Table 1) are still applicable when using these current limit modes. However, where the peak value in Table 2 is greater than the Adapter or Open Frame value (as applicable) in Table 1, then the peak value should be used.

As the continuous power is thermally limited, it will vary depending on the specific application. For example, if the peak power condition is of very low duty cycle, say a 1-second peak to close the door in a DVD player, then the thermal rise of the device (and transformer) is only a function of the continuous power. However if the peak power is repetitive and of significant duty cycle, then it is the average power that will determine the thermal performance and influence the device and core selection.

Figure 2 shows how to calculate the average power requirements for a design with two different peak load conditions.

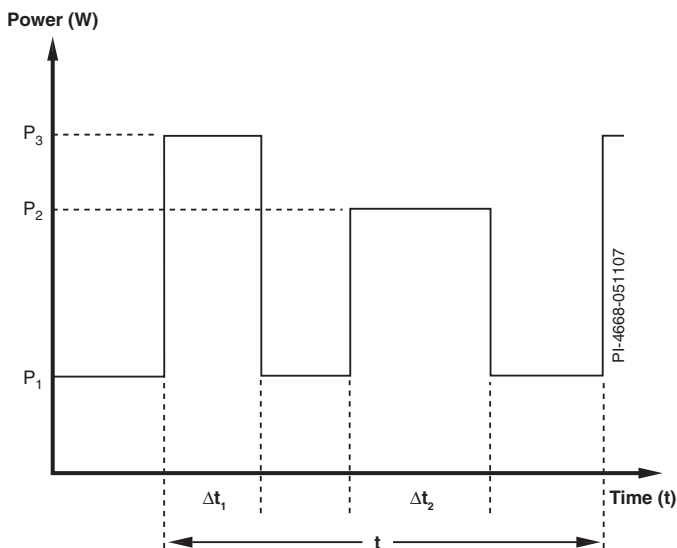


Figure 2. Continuous (Average) Output Power Calculation Example.

$$P_{AVE} = P_1 + (P_3 - P_1) \cdot \delta_1 + (P_2 - P_1) \cdot \delta_2$$

$$\delta_1 = \frac{\Delta t_1}{t}, \delta_2 = \frac{\Delta t_2}{t}$$

Where  $P_x$  are the different output power conditions,  $\Delta t_x$  are the durations of each peak power condition, and  $t$  is the period of one cycle of the pulsed load condition

The design procedure requires both peak and continuous powers to be specified. The peak power is used to select the TinySwitch-PK device and design the transformer for power delivery at minimum input line voltage, while continuous (or average power if the peak load is periodic) is used for thermal design and may affect the size of the transformer and the heat sink.

**Step 1. Enter Application Variables VAC<sub>MIN</sub>, VAC<sub>MAX</sub>, f<sub>L</sub>, V<sub>O</sub>, I<sub>O</sub>, V<sub>O</sub>, η, Z, t<sub>C</sub>, C<sub>IN</sub>**

Determine the input voltage range from Table 3.

Nominal Input Voltage (VAC)	VAC <sub>MIN</sub>	VAC <sub>MAX</sub>
100/115	85	132
230	195	265
Universal	85	265

Table 3. Standard Worldwide Input Line Voltage Ranges.

**Line Frequency, f<sub>L</sub>**

50 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC input. 50 Hz for single 230 VAC input. These values represent typical line frequencies rather than minimum. For most applications this gives adequate overall design margin. For absolute worst case or based on the product specification, reduce these numbers by 6% (47 Hz or 56 Hz). For half-wave rectification, use  $f_L/2$ . For DC input, enter the voltage directly into Cells B57 and B87.

**Nominal Output Voltage, V<sub>O</sub> (V)**

Enter the nominal output voltage of the main output. Generally the main output is the output from which feedback is derived.

**Peak Load Current, I<sub>O</sub> (A)**

Enter the maximum output current under peak load conditions.

ENTER APPLICATION VARIABLES		Customer	
VACMIN	85	Volts	Minimum AC Input Voltage
VACMAX	265	Volts	Maximum AC Input Voltage
fL	50	Hertz	AC Mains Frequency
VO	5.00	Volts	Output Voltage (at continuous power)
Peak Load Current, IO	2.60	Amps	Power Supply Output Current (corresponding to peak power)
Peak Power		13.00 Watts	Peak Output Power. Used to calculate primary inductance value
Continuous / Average Power	7.5	7.5 Watts	Continuous/Average Output Power. Used in estimation of Core size
η	0.67		Efficiency Estimate at output terminals. Use 0.7 if no better data available
Z		0.6	Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.6 if no better data available
tC	3.00	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	44.00	44 uFarads	Input Capacitance

Figure 3. Application Variable Section of TinySwitch-PK Design Spreadsheet.

If the design does not have a peak load condition, then enter the maximum continuous output current. In multiple output designs, the output current of the main output (typically the output from which feedback is taken) should be increased such that the peak power (or maximum continuous output current, as applicable) matches the sum of the output power from all the outputs in the design. The individual output voltages and currents should then be entered at the bottom of the spreadsheet (cells B99 to B145).

**Continuous / Average Output Power (W)**

Enter the continuous or average output power (as applicable). If this entry is left blank, then the design spreadsheet assumes that the continuous power is equal to  $P_{O(132\text{ kHz})}$ . This value is used by the design spreadsheet to suggest the core size.

**Peak Power (W)**

This is a calculated value based on the Output Voltage and Peak Load Current and is used to calculate the primary inductance value.

**Power Supply Efficiency,  $\eta$**

Enter the estimated efficiency of the complete power supply measured at the output terminals under peak load conditions and worst-case line (generally lowest input voltage). Start with a value of 0.7, typical for a design where the majority of the output power is drawn from an output voltage of 12 V or greater, and no current sensing is present on the secondary. Once a prototype has been constructed, then the measured efficiency should be entered and another transformer iteration created if required.

**Power Supply Loss Allocation Factor, Z**

This factor represents the proportion of losses between the primary and the secondary of the power supply. Z factor is used together with the efficiency number to determine the actual power that must be delivered by the power stage. For example,

losses in the input stage (EMI filter, rectification etc) are not processed by the power stage (transferred through the transformer) and therefore, although they reduce efficiency the transformer design are not impacted.

$$Z = \frac{\text{Secondary Side Losses}}{\text{Total Losses}}$$

For designs that do not have a secondary current sense circuit, enter 0.65; for those that do use a value of 0.7 until measurements can be made on a prototype. The higher number indicates larger secondary side losses associated with the current sense resistor.

**Bridge Diode Conduction Time,  $t_c$  (ms)**

Enter a bridge diode conduction time of 3.00 ms if there is no better data available.

**Total Input Capacitance,  $C_{IN}$  ( $\mu\text{F}$ )**

Enter total input capacitance using Table 4 for guidance.

AC Input Voltage (VAC)	Total Input Capacitance per Watt Output Power ( $\mu\text{F}/\text{W}$ )
100/115	3
230	1
85-265	3
85-265	3

Table 4. Suggested Total Input Capacitance for Different Input Voltage Ranges.

The capacitance is used to calculate the minimum and maximum DC voltage across the bulk capacitor and should be selected to keep the minimum DC input voltage,  $V_{MIN} > 70\text{ V}$ . For designs that have a DC rather than an AC input, the value of

DC INPUT VOLTAGE PARAMETERS					
VMIN			91	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage

Figure 4. DC Input Voltage Parameters Showing Grey Override Cells for DC Input Designs.

ENTER TinySwitch-PK VARIABLES					
TinySwitch-PK	TNY376		TNY376		User defined TinySwitch-PK
Chosen Device		TNY376			
Chose Configuration	INC		Increased Current Limit		Choose "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.465	Amps	Minimum Current Limit
ILIMITTYP			0.500	Amps	Typical Current Limit
ILIMITMAX			0.550	Amps	Maximum Current Limit
fSmin			248000	Hertz	Minimum Device Switching Frequency
I^2fmin			59.40	A^2kHz	Minimum I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
PO_132kHz			9.51	Watts	Estimated Maximum Power while still in 132 kHz operation
VOR	135.00		135	Volts	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10	Volts	TinySwitch-PK on-state Drain to Source Voltage
VD			0.5	Volts	Output Winding Diode Forward Voltage Drop
KP			0.53		Ripple to Peak Current Ratio (KP < 6)
KP_TRANSIENT			0.35		Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25

Figure 5. TinySwitch-PK Section of Design Spreadsheet.

the minimum and maximum DC input voltages,  $V_{MIN}$  and  $V_{MAX}$ , may be entered directly into the override cells on the design spreadsheet shown below (Figure 4).

### Step 2 – Enter TinySwitch-PK Variables: TinySwitch-PK Device, Current Limit, $V_{OR}$ , $V_{DS}$ , $V_D$

#### Select the correct TinySwitch-PK device

Refer to the TinySwitch-PK power table and first select a device based on the peak output power of the design. Then compare the continuous power to adapter column numbers in the power table. If the continuous power exceeds the value given in the power table, then the next largest device should be selected. Similarly, if the continuous power is close to the adapter power levels given in the power table, then it may be necessary to switch to a larger device based on the measured thermal performance of the prototype.

#### Select The Current Limit Configuration

Via the value of the BYPASS pin capacitor, TinySwitch-PK allows the internal current limit to be selected between 3 levels,  $I_{LIMITPEAKred}$ ,  $I_{LIMITPEAK}$  and  $I_{LIMITPEAKinc}$ . The choice can be selected in the spreadsheet by entering RED, STD or INC in cell [B18].

Selecting the correct current limit level depends on the thermal environment, the amount of board area or use of an external heatsink, and the average output power.

Entering RED gives the lowest current limit and results in lowest device dissipation due to lower  $I^2R_{DS(ON)}$  losses. This minimizes the amount of heat sinking needed even in high ambient conditions. An example where RED would be selected is in a sealed adapter with minimal heat sinking and/or where the ratio of average-to-peak output power is low.

Entering INC gives the highest current limit and therefore maximum power from a given device but increases  $I^2R_{DS(ON)}$  losses. This is ideal for open frame designs, adapters where an external heatsink sink is attached to the SOURCE pins of the device, or where the ratio of average-to-peak output power is high.

Entering STD is optimum for most applications, balancing dissipation and efficiency.

#### $f_{s(min)}$ Minimum Switching Frequency (Hz)

This parameter is the data sheet minimum switching frequency.

#### $I^2f_{(min)}$ Minimum Device Power Coefficient

This value is the minimum data sheet  $I^2f$  parameter for the selected device and current limit mode. The calculation for primary inductance is based on this value.

#### Output Power Operating at 132 kHz, $P_{O(132kHz)}$

This value indicates the maximum output power at which operation at a switching frequency of 132 kHz or below will occur. As conducted EMI measurements generally start at 150 kHz, it may be advantageous to keep the switching frequency below this value to minimize EMI filtering required.

Performance Goal	$V_{OR}$ Value Suggestion	Comment
Maximum output power / smallest TinySwitch-PK device	135 V	Maximizes power from a given device
Highest efficiency	100 V to 120 V	Gives lowest overall losses between conduction, output diode and leakage inductance
Multiple output design	90 V to 110 V	Improves cross regulation by reducing transformer leakage inductance and peak secondary currents

Table 5. Suggested Values for  $V_{OR}$ .

The specific load condition at which EMI measurements are made will determine if there is a benefit in adjusting the design so that the continuous output power is below  $P_{O(132kHz)}$ . For example, if the peak load occurs once at startup, then keeping the continuous power below  $P_{O(132kHz)}$  will give a potential EMI improvement. However, if the peak load is periodic during normal operation, then there is less of a benefit, as EMI will be measured while TinySwitch-PK is operating at 264 kHz.

The value for  $P_{O(132kHz)}$  is calculated at  $V_{MIN}$ ,  $I^2f_{MIN}$ ,  $L_{P(MIN)}$  and assumes that the TinySwitch-PK device is operating in Peak Mode (264 kHz) with alternate cycles being skipped, therefore giving an effective switching frequency of 132 kHz.

#### Reflected Output Voltage, $V_{OR}$ (V)

This parameter is the secondary winding voltage during the diode conduction time reflected back to the primary through the turns ratio of the transformer. The default value is 135 V; however the acceptable range for  $V_{OR}$  is between 80 V and 135 V, providing no warnings in the spreadsheet are triggered. For design optimization purposes, the following should be kept in mind:

1. Higher  $V_{OR}$  allows increased power delivery at  $V_{MIN}$ , which minimizes the value of the input capacitor and maximizes power delivery from a given TinySwitch-PK device.
2. Higher  $V_{OR}$  reduces the voltage stress on the output diodes, which in some cases may allow a lower forward drop Schottky diode for higher efficiency.
3. Higher  $V_{OR}$  increases primary turns and therefore leakage inductance that reduces efficiency of the power supply.
4. Higher  $V_{OR}$  increases peak and RMS current on the secondary side, which may increase secondary side copper and diode losses.

Optimal selection of the  $V_{OR}$  value depends on the specific application and is based on a compromise between the factors mentioned above. Table 5 provides suggested values based on design goals.

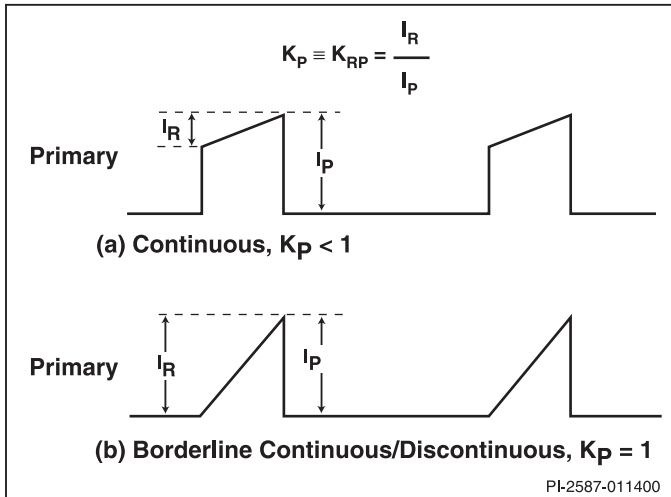


Figure 6. Continuous Mode Current Waveform,  $K_p \leq 1$ .

Values below 80 V are not recommended. Low  $V_{OR}$  may cause repeated triggering of the MOSFET self protection feature during startup, especially in designs where all outputs are  $>5$  V.

**TinySwitch-PK On-State Drain to Source Voltage,  $V_{DS}$  (V)**

This parameter is the average on state voltage developed across the DRAIN and SOURCE pins of TinySwitch-PK. By default, if the grey override cell is left empty, a value of 10 V is assumed. Use the default value if no better data are available.

**Output Diode Forward Voltage Drop,  $V_D$  (V)**

Enter the average forward voltage drop of the (main) output diode. Use 0.5 V for a Schottky diode or 0.7 V for a PN diode if no better data are available. By default, a value of 0.5 V is assumed.

**Ripple to Peak Current Ratio,  $K_{P(STEADYSTATE)}$  and  $K_{P(TRANSIENT)}$**

Below a value of 1, indicating continuous conduction mode,  $K_p$  is the ratio of ripple to peak primary current (Figure 7).

Above a value of 1, indicating discontinuous conduction mode,  $K_p$  is the ratio of primary MOSFET off time to the secondary diode conduction time.

$$K_p \equiv K_{DP} = \frac{(1 - D) \times T}{t} = \frac{V_{OR} \times (1 - D_{MAX})}{(V_{MIN} - V_{DS}) \times D_{MAX}}$$

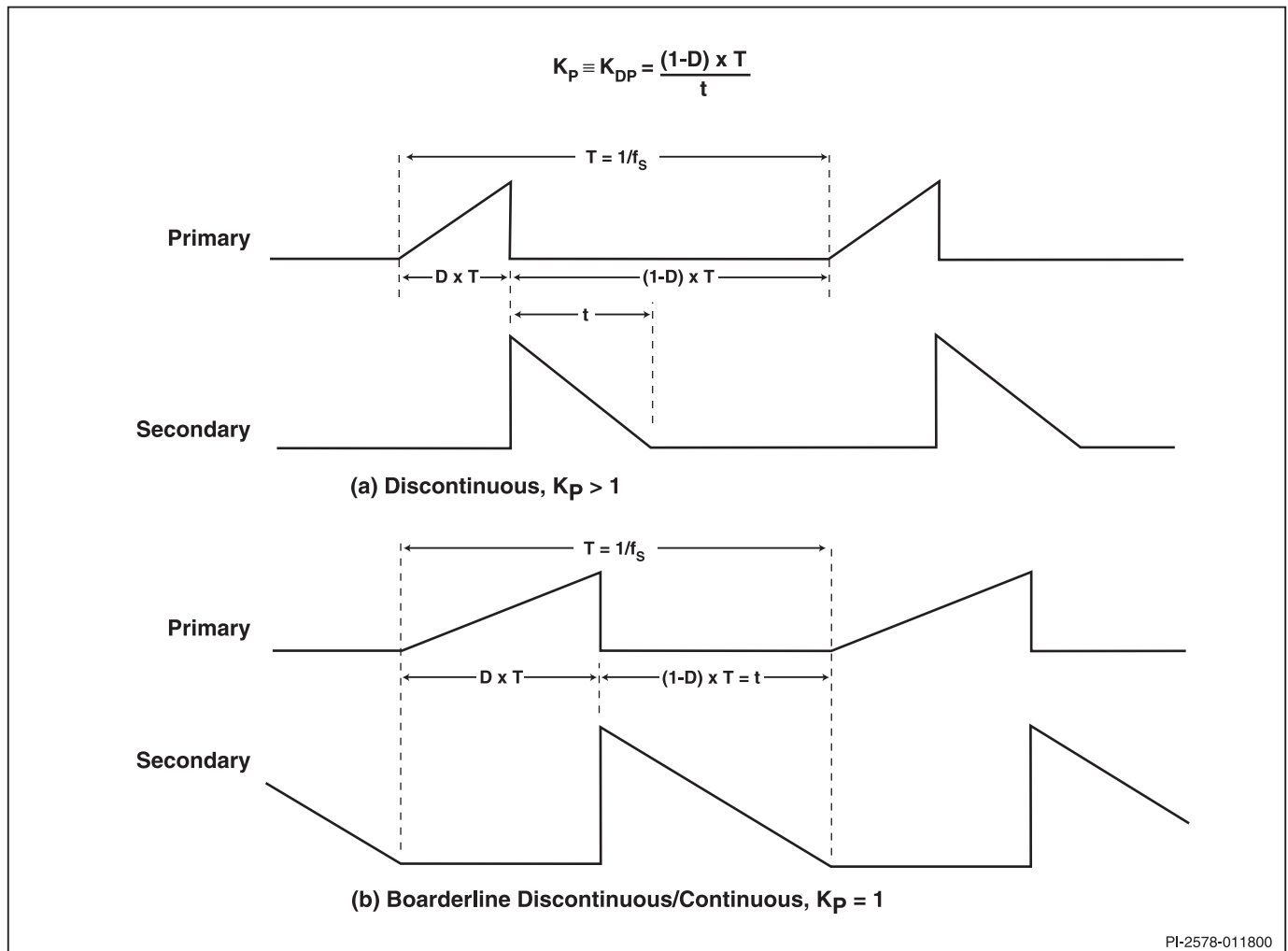


Figure 7. Discontinuous Mode Current Waveform,  $K_p \geq 1$ .

The value of  $K_p$  should be in the range of  $0.25 < K_p < 6$ , and guidance is given in the comments cell if the value is outside this range.

$K_{P(\text{STEADY STATE})}$  is the calculated  $K_p$  value under the condition where several switching cycles have occurred consecutively.

$K_{P(\text{TRANSIENT})}$  is the calculated minimum  $K_p$  value that occurs after a switching cycle has been skipped. As the drain current starts from zero, ramping to current limit, the on-time for this first cycle is much longer than during steady state. This reduces the off-time, lowering the time for the magnetizing inductance to reset and causing the next cycle to start with a much higher initial current, lower ripple current, and lower value of  $K_p$ .

$K_{P(\text{TRANSIENT})}$  should be above a value of 0.25 to prevent the large initial current pedestal from falsely triggering current limit at the end of the leading edge blanking time and limiting power delivery.

### Step 3 – Choose Bias Winding Output Voltage, $V_B$ (V)

By default, if the grey override cell is left empty, a value of 22 V is assumed. The user can override this value as needed; a value in the range of  $15 \text{ V} < V_B < 30 \text{ V}$  is recommended. The lower limit is to ensure adequate headroom for supplying current into the BYPASS pin, and the upper limit is to limit no-load input power due to bias winding power consumption. The number of bias winding turns,  $N_B$ , is used for transformer construction, and an ultra-fast diode with a voltage rating above the PIVB value should be selected (1N4148 or BAV20 diodes are ideal). The  $V_{Z(\text{OV})}$  value is an estimate for the Zener diode voltage rating used for output over voltage protection. When the

Zener diode conducts 7 mA of current, the latching shutdown feature of TinySwitch-PK is triggered, and the power supply latches off.

The use of a bias winding is optional for the two smallest family members, TNY375 and TNY376, but must be used with all other devices. The resistor value  $R_{\text{BIAS}}$  is calculated to provide the maximum data sheet IC supply current ( $I_{S2} + I_{\text{DIS}}$ ).

### Step 4 – Enter Under Voltage Lock Out (UVLO) Variables, $V_{\text{UV\_TARGET}}$ (V)

The line undervoltage lockout feature of TinySwitch-PK defines the startup voltage of the supply. This prevents the power supply output from glitching when the input voltage is below the normal operating range. Connecting a resistor from an input capacitor to the EN/UV pin enables this feature. Enter the desired DC voltage across the input capacitor at which the power supply should operate. The spreadsheet calculates both the ideal resistor value and closest preferred value together with the typical actual start-up voltage based on the closest standard value. The resistor voltage rating (or sum of ratings if two series resistor are used) should exceed  $V_{\text{MAX}}$ .

The undervoltage threshold also resets the output overvoltage latching shutdown. After AC removal, once the voltage of the DC bus falls below the undervoltage threshold, the OV latch is reset.

### Step 5 – Choose Core and Bobbin Based on Output

#### Power and Enter $A_E$ , $L_E$ , $A_L$ , BW, M, L, $N_S$

Core effective cross-sectional area,  $A_E$ : (cm<sup>2</sup>)

Core effective path length,  $L_E$ : (cm)

ENTER BIAS WINDING VARIABLES					
VB			22.00	Volts	Bias Winding Voltage
VDB			0.70	Volts	Bias Winding Diode Forward Voltage Drop
NB			12.00		Bias Winding Number of Turns
R_BIAS			21.00	kohm	Bias winding resistor to externally power TinySwitch-PK
VZOV			28.00	Volts	Over Voltage Protection Zener Diode

Figure 8. Bias Winding Variables Section of Design Spreadsheet.

ENTER UVLO VARIABLES					
V_UV_TARGET			100.07	Volts	Target undervoltage threshold, above which the power supply will start
V_UV_ACTUAL			100.20	Volts	Typical start-up voltage based on standard value of RUV_ACTUAL
RUV_IDEAL			3.91	Mohms	Calculated value for UV Lockout resistor
RUV_ACTUAL			3.92	Mohms	Closest standard value of resistor to RUV_IDEAL

Figure 9. Undervoltage Variables Section of Design Spreadsheet.

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EEL19		EEL19		User defined Core Size (Verify thermal performance under continuous/average load conditions)
Core		EEL19		P/N:	PC40EE19/27/5-Z
Bobbin		EEL19_BOBBIN		P/N:	EEL19_BOBBIN
AE			0.2454	cm <sup>2</sup>	Core Effective Cross Sectional Area
LE			6.185	cm	Core Effective Path Length
AL			720	nH/T <sup>2</sup>	Ungapped Core Effective Inductance
BW			19.7	mm	Bobbin Physical Winding Width
M	3.00		3	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	2.00		2		Number of Primary Layers
NS			3		Number of Secondary Turns

Figure 10. Transformer Core and Construction Variables Section of Spreadsheet.

Core ungapped effective inductance,  $A_L$ : (nH/turn<sup>2</sup>)  
 Bobbin width, BW: (mm)  
 Tape margin width equal to half the total margin, M (mm)  
 Primary Layers, L  
 Secondary Turns,  $N_s$

### Core Type

By default, if the core type cell is left empty, the spreadsheet will select the smallest commonly available core suitable for the continuous output power specified. The entire list of cores available can be selected from the drop down list in the tool bar of the PI Xls design software. The grey override cells can be used to enter the core and bobbin parameter directly by user. This is useful if a core is selected that is not on the list, or the specific core or bobbin information differs from that recalled by the spreadsheet.

### Safety Margin, M (mm)

For designs that require isolation but are not using triple insulated wire, the width of the safety margin to be used on each side of the bobbin should be entered here. Typically, for universal input designs, a total margin of 6.2 mm would be required, and a value of 3.1 mm would be entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical. However if a total margin of 6.2 mm were required, then 3.1 mm would still be entered even if the physical margin were on one side of the bobbin.

For designs using triple insulated wire, it may still be necessary to enter a small margin in order to meet the required safety creepage distances. Typically many bobbins exist for each core size, and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance from your safety expert or transformer vendor to determine what specific margin is required. As the margin reduces the available area for the windings, margin construction may not be suitable for small core sizes. If after entering the margin more than 3 primary layers (L) are required, it is suggested that either a larger core be selected or switch to a zero margin design using triple insulated wire.

### Primary Layers, L

By default, if the override cell is empty, a value of 3 is assumed. Primary layers should be in the range of  $1 < L < 3$ , and in general it should be the lowest number that meets the primary current density limit (CMA) of 200 Cmil/Amp. Values above 3 layers are possible, but the increased leakage inductance and physical fit of the windings should be considered. Due to the high switching frequency of TinySwitch-PK designs, it is important to minimize transformer leakage inductance. A split primary construction may be helpful for designs where primary clamp dissipation is unacceptably high. Here half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement.

### Secondary Turns, $N_s$

By default, if the grey override cell is left blank, the minimum number of secondary turns is calculated such that the maximum operating flux density BM is kept below the recommended maximum of 3000 Gauss (300 mT). In general, it is not necessary to enter a number in the override cell except

in designs where a lower operating flux density is desired (see the explanation of BM limits).

## Step 6 – Iterate Transformer Design and Generate Initial Design

Iterate the design making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right-hand column.

Once all warnings have been cleared, the output transformer design parameters can be used to either wind a prototype transformer or sent to a vendor for samples.

### The Key Transformer Electrical Parameters Are:

#### Primary inductance, $L_p$ ( $\mu$ H)

This is the target nominal primary inductance of the transformer.

#### Primary inductance tolerance, $L_{p\_TOLERANCE}$ (%)

This is the assumed primary inductance tolerance. A value of 12% is used by default; however if specific information is known from the transformer vendor, then this may be entered in the grey override cell.

#### Number of Primary Turns, $N_p$

Total number of primary turns. For low leakage inductance applications, a split primary construction may be used.

#### Gapped core effective inductance, $A_{LG}$ : (nH/t<sup>2</sup>)

Used by the transformer vendor to specify the core (gap).

#### Target $B_M$ , (Gauss)

The value entered here is used to calculate the number of secondary turns. By default a value of 2800 Gauss is used, slightly below the recommended maximum BM value of 3000 Gauss. This accounts for rounding down of the number of calculated secondary turns in some designs.

#### Maximum Operating Flux Density, $B_M$ (Gauss)

A maximum value of 3000 Gauss during normal operation is recommended to limit the maximum flux density under startup and output short circuit. Under these conditions the output voltage is low, and little reset of the transformer occurs during the MOSFET off time. This allows the transformer flux density to staircase above the normal operating level. A value of 3000 Gauss at the peak current limit of the selected device, together with the built-in protection features of TinySwitch-PK, provides sufficient margin to prevent core saturation under startup or output short circuit conditions.

The cycle skipping mode of operation used in TinySwitch-PK can generate audio frequency components in the transformer. To limit this audible noise generation, the transformer should be designed such that the peak core flux density is below 3000 Gauss (300 mT). Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. A careful evaluation of the audible noise performance should be made using production transformer samples before approving the design. Ceramic capacitors that use dielectrics, such as Z5U, when used in



clamp circuits, may also generate audio noise. If this is the case, try replacing them with a capacitors having a different dielectric, for example a polyester film type.

#### Maximum Primary Wire Diameter, OD (mm)

By default, if the override cell is empty, double insulated wire is assumed, and the standard wire diameter is chosen. The grey override cells can be used to enter the wire diameter directly by the user if the wire used is different from the standard double coated/heavy nylze types.

#### Estimated Total Insulation Thickness, INS (mm)

Primary wire size, DIA: (mm)

Primary wire gauge, AWG

Number of primary layers, L

Estimated core center leg gap length:  $L_g$ : (mm)

Number of secondary turns,  $N_s$

Secondary wire size, DIAs: (mm)

Secondary wire gauge, AWG

In multiple output designs, NSx, CMSx, AWGSx (where x is the output number) should also be used.

TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			813	uHenries	Typical Primary Inductance. +/- 12% to ensure a minimum primary inductance of 725 uH
LP_TOLERANCE			12	%	Primary inductance tolerance
NP			74		Primary Winding Number of Turns
ALG			150	nH/T^2	Gapped Core Effective Inductance
BM			2807	Gauss	Maximum Operating Flux Density at LP_TYP and I_LIMITMAX, BM<3000 is recommended
BAC			747	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1444		Relative Permeability of Ungapped Core
LG			0.16	mm	Gap Length (Lg > 0.1 mm)
BWE			27.4	mm	Effective Bobbin Width
OD			0.37	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.31	mm	Bare conductor diameter
AWG			29	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			128	Cmils	Bare conductor effective area in circular mils
CMA_PEAK			393	Cmils	Primary Winding Current Capacity under peak load condition (200 < CMA < 500)
CMA		Info	554	Cmils/Am	CAN DECREASE CMA < 500 (decrease L(primary layers),increase NS,use smaller Core)

Figure 11. Transformer Primary Design Parameters Section of Spreadsheet.

TRANSFORMER SECONDARY DESIGN PARAMETERS					
<b>Lumped parameters</b>					
ISP			11.41	Amps	Peak Secondary Current
ISRMS			6.20	Amps	Secondary RMS Current
IRIPPLE			5.63	Amps	Output Capacitor RMS Ripple Current
CMS			1239	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			19	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)

Figure 12. Transformer Secondary Design Parameters Section of Spreadsheet – Lumped Into Single Outputs.

TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
<b>1st output</b>					
VO1			5	Volts	Main Output Voltage (if unused, defaults to single output design)
IO1			2.600	Amps	Output DC Current (Enter Peak Value)
PO1			13.00	Watts	Output Power
VD1			0.5	Volts	Output Diode Forward Voltage Drop
NS1			3.00		Output Winding Number of Turns
ISRMS1			6.197	Amps	Output Winding RMS Current
IRIPPLE1			5.63	Amps	Output Capacitor RMS Ripple Current
PIVS1			20	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diodes			90SQ030		Recommended Diodes for this output
CMS1			1239	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			19	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.91	mm	Minimum Bare Conductor Diameter
ODS1			4.57	mm	Maximum Outside Diameter for Triple Insulated Wire
<b>2nd output</b>					
VO2				Volts	Output Voltage
IO2				Amps	Output DC Current (Enter Peak Value)
PO2			0.00	Watts	Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			0.38		Output Winding Number of Turns
ISRMS2			0.000	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode					Recommended Diodes for this output
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
<b>3rd output</b>					
VO3				Volts	Output Voltage
IO3				Amps	Output DC Current (Enter Peak Value)
PO3			0.00	Watts	Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.38		Output Winding Number of Turns
ISRMS3			0.000	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode					Recommended Diodes for this output
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
<b>Total power</b>			13	Watts	Total Output Power
Negative Output			N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

Figure 13. Transformer Secondary Design Parameters Section of Spreadsheet – Multiple Outputs.

**Step 7 – Selection of TinySwitch-PK External Components**

**Bypass/Multi-Function pin capacitor**

The capacitor connected to the Bypass/Multi-Function pin is used for both local supply decoupling and selection of one of three current limit levels.

A value of 0.1 μF selects  $I_{LIMITPEAK}$ , 1 μF selects  $I_{LIMITPEAKred}$ , and 10 μF selects  $I_{LIMITPEAKinc}$ .

For flexibility in device selection, the current limit values overlap between adjacent family members. A 1 μF BP/M pin capacitor will select a lower current limit equal to the standard current limit of the next smaller device. A 10 μF capacitor BP/M pin capacitor will select a higher current limit equal to the standard current limit of the next larger device. This makes switching

from one family member to another as simple as changing the value of the BP/M pin capacitor. For example, a design using the TNY375 in  $I_{LIMIT}$  mode can also use a TNY376 in  $I_{LIMITPEAKred}$  mode to reduce device dissipation. The TNY375 and TNY376 MOSFET do not have the capability to match the next larger devices in the family. The current limit is therefore increased to the maximum capability of their respective MOSFET.

The standard current limit,  $I_{LIMIT}$ , is tailored to the power capability of the device package assuming heatsinking via a copper area on the PC board. The maximum practical copper area is 3 square inches (19.4 cm<sup>2</sup>) of 2 ounce copper (610 g/m<sup>2</sup>). Larger areas can be used, but the reduction in device temperature is small. The maximum recommended source pin temperature is 110 °C under worst case operating conditions, generally highest ambient and low line.

Operating in  $I_{LIMITPEAKine}$ , increases the output power capability without requiring a larger device but, depending on the continuous or average output power, may require an external heatsink attached to the SOURCE pins of the device.

Operating in  $I_{LIMITPEAKred}$  decreases output power from a given device but reduces dissipation and therefore increases efficiency.

The type of capacitor can be either ceramic or electrolytic rated above the maximum BP/M pin voltage of 6.15 V.

When using a 1  $\mu\text{F}$  or 10  $\mu\text{F}$  capacitor, it is recommended that a 0.1  $\mu\text{F}$  ceramic capacitor is placed directly between BP/M and SOURCE pin for high frequency decoupling.

The limits for correct value detection are  $C_{BP} \leq 0.2 \mu\text{F}$  for a 0.1  $\mu\text{F}$  capacitor,  $0.5 \mu\text{F} \leq C_{BP} \leq 2 \mu\text{F}$  for a 1  $\mu\text{F}$  capacitor, and  $C_{BP} \geq 5 \mu\text{F}$  for a 10  $\mu\text{F}$  capacitor.

### Step 8 – Selection of Undervoltage Components

Line undervoltage prevents the supply from starting until the input voltage is above a defined level. During power-up or when the switching of the power MOSFET is disabled in auto-restart, the current into the EN/UV pin must exceed 25  $\mu\text{A}$  to initiate switching. As a resistor from the DC rail to the EN/UV pin is used to sense the input voltage, the supply voltage that causes the current into the EN/UV to exceed 25  $\mu\text{A}$  defines the undervoltage threshold.

If no resistors are fitted, then the TinySwitch-PK device senses this condition (less than  $\sim 1 \mu\text{A}$  into the EN/UV pin), and the UV function is disabled.

In high pollution degree and /or high humidity environments, leakage currents into the EN/UV may exceed this level. Typically this is the result of using contaminated no-clean-flux during manufacture. Following the flux manufacturer's guidelines to prevent contamination or adding a 100 k $\Omega$  (5%) resistor between BP/M and EN/UV pins (to feed a current of  $> I_{UV(MAX)}$  into the EN/UV pin) prevents this problem.

The sense resistor should be rated above 400 V, generally requiring either a single 0.5 W or two 0.25 W devices connected in series.

### Step 9 – Selection of Primary Clamp Components

It is recommended that either a Zener clamp or an RCD combined with a Zener clamp be used in TinySwitch-PK designs. This is to ensure that the peak drain voltage is limited to below the  $BV_{DSS}$  of the internal MOSFET while still maximizing efficiency and minimizing no-load consumption.

A standard RCD clamp designed to limit the peak drain voltage under peak load conditions represents a significant load as the output power is reduced resulting in lower light load efficiency and higher no load consumption.

Figure 1 shows an example of an optimized clamp arrangement. The addition of VR1 in parallel with C3 and R1 prevents C3 from discharging below 180 V as the effective switching frequency reduces as the load is reduced. The value of R1 is selected so that the peak drain voltage is limited to an acceptable level under worst case conditions of maximum input voltage, maximum overload power or output short circuit and maximum ambient temperature. A maximum voltage of 650 V is recommended to provide margin due to component variation.

The clamp diode (D5) must be a fast or an ultra-fast recovery type with a reverse recovery time  $\leq 500$  ns. Under no circumstances should a slow recovery rectifier diode be used. The high dissipation that may result during startup or an output short circuit can cause failure of the diode. Resistor R2 damps ringing for reduced EMI, and is typically in the range of 22  $\Omega$  to 100  $\Omega$ .

Supplies using different TinySwitch-PK devices in the family will have different peak primary currents, leakage inductances, and therefore, leakage energy. Capacitor C3 and R1 will therefore be optimized for each design. As a general rule, minimize the value of capacitor C3 and maximize the value of resistor R1 while still maintaining  $< 650$  V on drain.

### Step 10 – Select Output Rectifier Diode

For each output, use the values of peak inverse voltage ( $V_R$ ) and output current ( $I_D$ ) provided in the design spreadsheet to select the output diodes. Table 6 shows some commonly available types.

Product <sup>3</sup>	Type	$V_R$	$I_D$	Pkg	Manufacturer
		V	A		
IN5817 to 1N5819	Schottky	20-40	1	Leaded	Vishay
SB120 to SB1100	Schottky	20-100	1	Leaded	Vishay/Fairchild
11DQ50 to 11DQ60	Schottky	50-60	1	Leaded	IR
1N5820 to 1N5822	Schottky	20-40	3	Leaded	Vishay
MBR320 to MBR360	Schottky	20-60	3	Leaded	IR/On Semi
SS12 to SS16	Schottky	20-60	1	SMD	Vishay
SS32 to SS36	Schottky	20-60	3	SMD	Vishay
SB540 to SB560	Schottky	40-60	5	Leaded	Vishay
UF4002 to UF4006	Ultrafast	100-600	1	Leaded	Vishay
MUR110 to MUR160	Ultrafast	100-600	1	Leaded	On Semi
UF5401 to UF5408	Ultrafast	100-800	3	Leaded	Vishay
ES1A to ES1D	Ultrafast	50-200	1	SMD	Vishay
ES2A to ES2D	Ultrafast	50-200	2	SMD	Vishay
BYV28-200	Ultrafast	200	3.5	Leaded	Vishay
MBR745 to MBR760	Schottky	40-60	7.5	TO220	Vishay
MBR1045 to MBR10100	Schottky	45-100	10	TO220	Vishay
BYW29-100 to BYW29-200	Ultrafast	100-200	8	TO220	Vishay

Table 6. List of Diodes Suitable for Use as the Output Rectifier.

$V_R \geq 1.25 \times \text{PIVS}$ : where PIVS is taken from the Voltage Stress Parameters section of the spreadsheet and Transformer Secondary Design Parameters (Multiple Outputs).

$I_D \geq 2 \times I_O$ : where  $I_D$  is the diode rated DC current, and  $I_O$  is the average output current. Depending on the thermal rise and the duration of the peak load condition, it may be necessary to increase the diode current rating once a prototype has been built. This also applies to the amount of heatsinking necessary.

**Step 11 – Select Output Capacitor**

**Ripple Current Rating**

The spreadsheet calculates the output capacitor ripple current at the peak load condition. Therefore the actual rating of the capacitor will depend on the peak-to-average power ratio of the design. For conservative design select the output capacitor(s) such that the ripple rating is greater than the calculated value,  $I_{\text{RIPPLE}}$  from the spreadsheet, calculated at the peak load condition. However in designs with high peak-to-continuous (average) power, the capacitor rating can be reduced based on the measured capacitor temperature rise under worst case load and ambient temperature. If a suitable individual capacitor cannot be found, then two or more capacitors may be used in

parallel to achieve a combined ripple current rating equal to the sum of the individual capacitor ratings.

Many capacitor manufacturers provide factors that increase the ripple current rating as the capacitor operating temperature is reduced from its data sheet maximum. This should be considered to ensure that the capacitor is not oversized.

**ESR Specification**

The switching ripple voltage is equal to the peak secondary current multiplied by the ESR of the output capacitor. It is therefore important to select low ESR capacitor types to reduce the ripple voltage. In general, selecting a high ripple current rated capacitor results in an acceptable value of ESR.

**Voltage Rating**

Select a voltage rating such that  $V_{\text{RATED}} \geq 1.25 V_O$ .

**Step 12 – Select feedback circuit components**

Table 7 shows a typical implementation of Zener feedback. The series drops across  $D_{\text{FB}}$ ,  $V_{\text{RFB}}$ ,  $R_{\text{FB1}}$  and the forward drop of the LED  $U_{\text{FB2}}$  determine the output voltage. Diode  $D_{\text{FB}}$  is optional depending on the availability of a suitable Zener voltage. Resistor  $R_{\text{BIAS}}$  provides a 1 mA bias current so that  $V_{\text{RFB}}$  is

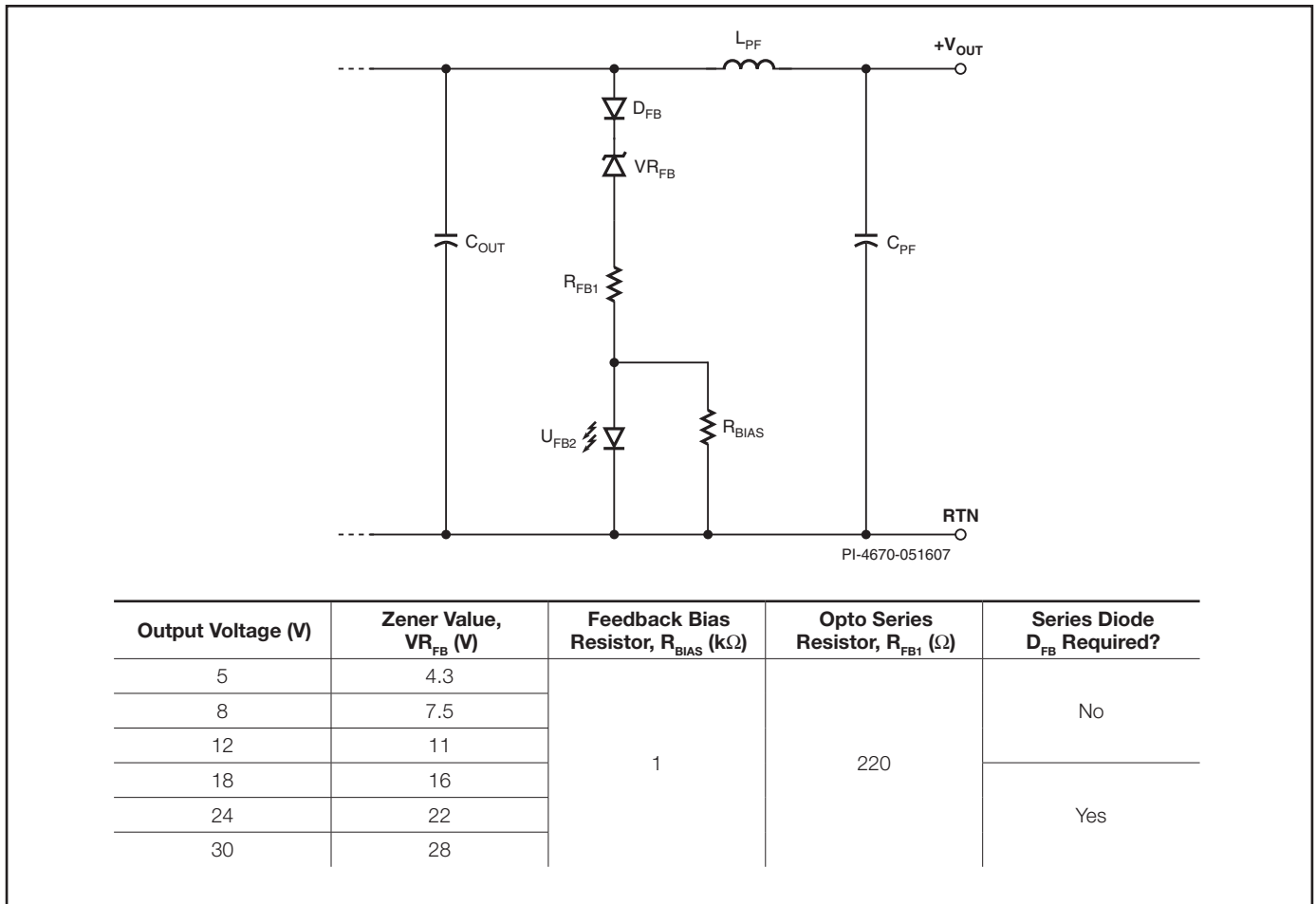


Table 7. Typical Component Values.

operated close to its knee voltage. Resistor  $R_{FB1}$  sets the DC gain of the feedback. Both of these can be 0.125 W or 0.25 W, 5% types. Selecting a Zener with a low test current (5 mA) is recommended to minimize the current needed to bias the feedback network, reducing no-load input power consumption. Table 7 shows values for common output voltages.

For improved accuracy, Table 8 shows a typical implementation using a reference IC. Reference  $U_{FB2}$  is used to set the output voltage programmed via the resistor divider  $R_{S1}$  and  $R_{S2}$ . Resistor  $R_{BIAS}$  provides the minimum operating current for  $U_{FB2}$  while  $R_{FB1}$  sets the DC gain. Capacitor  $C_{FB2}$  rolls off the gain of  $U_{FB2}$  so that it does not respond to the cycle-by-cycle output ripple voltage. AC feedback is provided directly through the optocoupler. Table 8 shows component values for common output voltages.

If necessary a post filter ( $L_{PF}$  and  $C_{PF}$ ) can be added to reduce high frequency switching noise and ripple. Inductor  $L_{PF}$  should be in the range of 1  $\mu$ H – 3.3  $\mu$ H with a current rating above the peak output current. Capacitor  $C_{PF}$  should be in the range of 100  $\mu$ F to 330  $\mu$ F with a voltage rating  $\geq 1.25 \times V_{OUT}$ . If a post filter is used, then the optocoupler should be connected as

shown before the post filter inductor, and the sense resistors after the post filter inductor.

### Tips for Designs

#### Output Overvoltage Latching Shutdown

The latching shutdown feature can be used to protect the load from a catastrophic open loop fault, such as failure of the optocoupler.

To trigger the latching shutdown feature of TinySwitch-PK, a current ( $I_{SD}$ )  $>7$  mA must flow into the BP/M pin. This can be achieved by sensing the bias winding voltage. In Figure 14, the bias voltage across C7 is typically 22 V. During an open loop condition, the bias voltage will rise in proportion to the output voltage. Once this rises above the sum of the BP/M pin voltage (6.4 V) and the rating of VR2 (22 V), then current will flow into the BP/M pin. When this exceeds  $I_{SD}$  then the part will latch off. To reset the latch, either the EN/UV pin current must fall below the UV threshold current (25  $\mu$ A), or the BP/M pin voltage falls below 4.8 V. Typically this would occur after the AC input is removed, and the input bulk capacitor discharges. This may take significant time ( $>1$  minute) to occur; therefore in designs where a faster reset is required, then a separate AC sense circuit can be used to feed the EN/UV pin.

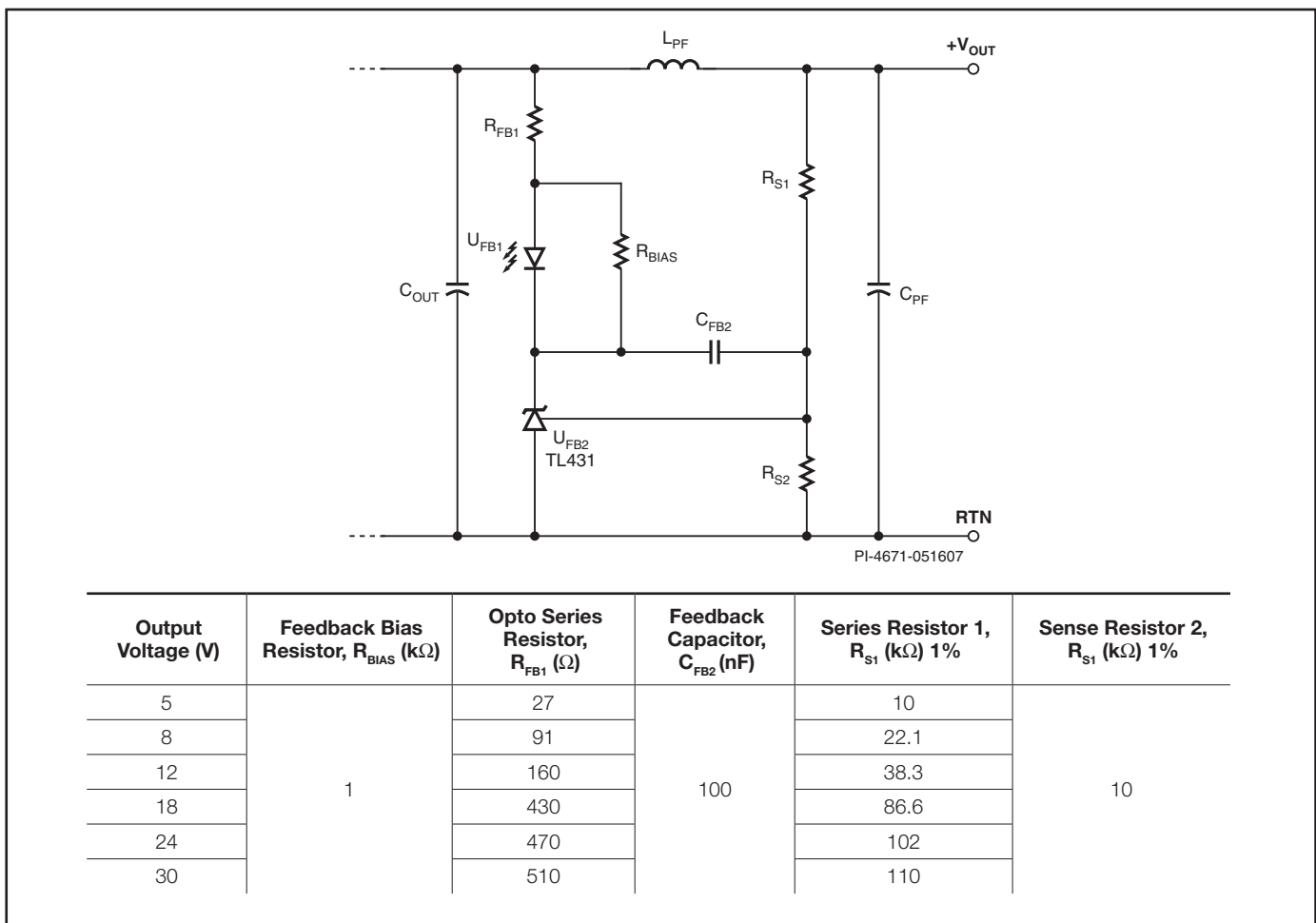


Table 8. Component Values for Common Output Voltages.

The bias voltage also varies with load due to the effect of leakage inductance, and therefore R4 provides filtering. Resistor R5 can be used to fine tune the trigger point. It is important that the trigger point is sufficiently away from the normal regulation range such that it is not falsely triggered.

To test a design, monitor the bias voltage and find the worst-case condition (highest bias voltage across C7). This is generally either startup into no load at high line input or full (peak) load operation at low line input.

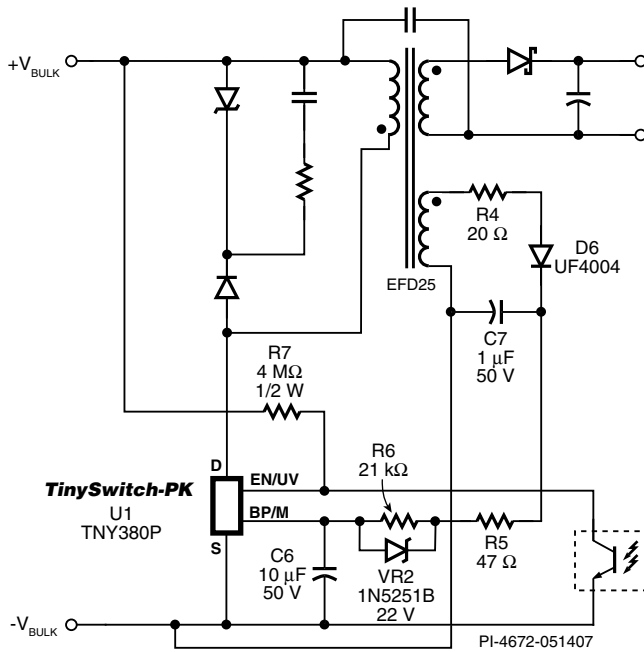


Figure 14. Example Schematic Showing Implementation of OV Shut-down and External Bias Current.

### IC Supply Current

During normal operation, TinySwitch-PK must have an external supply current equal to  $I_{S2(MAX)} + |I_{DIS(MAX)}|$ . In Figure 14, resistor R6 provides this current from the bias voltage across C7. As the switching frequency can be low during light or no-load conditions, it is recommended that a 1  $\mu$ F capacitor is used for the bias winding to prevent excessive droop. This can be either ceramic or electrolytic rated above the maximum bias voltage.

### Transformer Core Sizing

The high switching frequency of TinySwitch-PK allows the selection of small core sizes that will adequately process the peak power. However, the small core size reduces the amount of winding window area available. This reduces the amount of copper for the windings, increasing winding losses if operated with peak load continuously.

As most applications have a large peak-to-continuous power ratio, the value for primary winding current capacity (CMA) is determined using the continuous / average output power rather than peak power. However, as the ratio of peak to continuous power approaches 1, the transformer core size may need to be increased to reduce losses and transformer heating by increasing the available winding area. Determine if the temperature rise of the transformer is acceptable at worst-case ambient temperature and maximum load.

### On-time Extension

The On-time extension feature of TinySwitch-PK maximizes the power delivered to the load when the DC input (bulk capacitor) voltage is low. This may allow the use of a smaller input capacitor in designs where the output can droop under peak load, especially in applications where the supply must pass line brown-outs or missing AC cycle tests. On-time extension also increases the typical hold-up time. Figure 15 shows the effect of on-time extension on hold-up time.

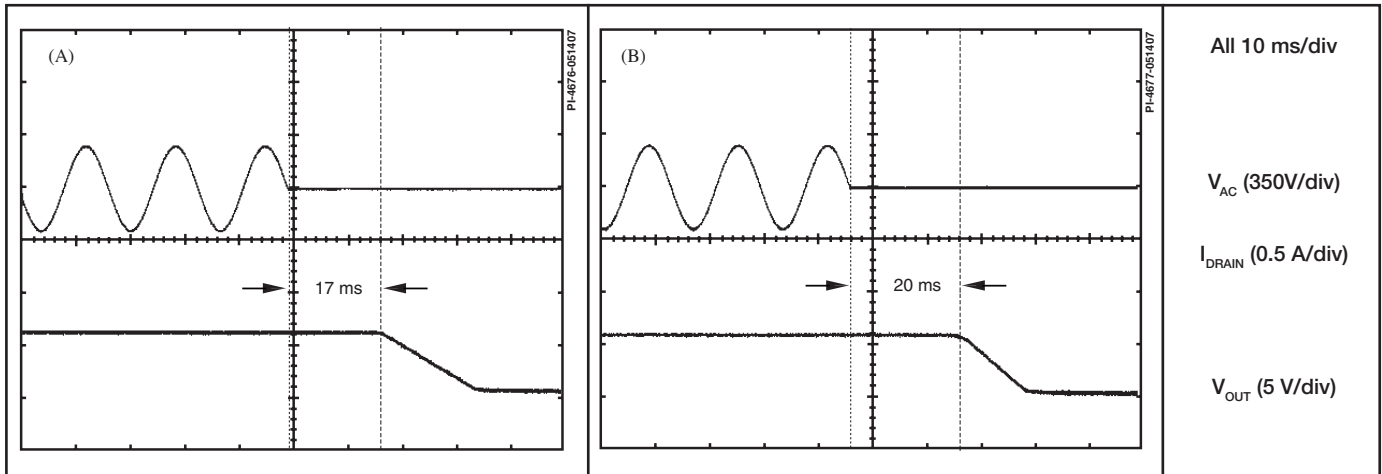


Figure 16. Effect of On-Time Extension Operation on Hold-up Time. (A) Without On-Time Extension Regulation is Lost at 17 ms. (B) With On-Time Regulation is Lost at 20 ms.

On-time Extension is enabled once the output has reached regulation and the EN/UV pin has been pulled low. It remains enabled until auto-restart. While enabled, the maximum duty cycle limit is disabled, and switching cycles are terminated by current limit or a maximum on-time of 15  $\mu$ s. While a useful DC bus voltage exists, the MOSFET on-time is only determined by the time for the primary current to reach current limit. The off-time of the MOSFET remain fixed at  $(1-D_{MAX}) \times 1/f_s$ , where  $D_{MAX}$  is the maximum duty cycle and  $f_s$  the switching frequency. The 15  $\mu$ s maximum on time prevents the MOSFET being left on indefinitely at very low DC bulk voltage ( $< \sim 30$  V), where the drain current may fail to reach current limit.

### Layout Guidelines

See data sheet for layout guidelines.

### Quick Design Checklist

See data sheet for quick design checklist.

Revision	Notes	Date
A	Final Release	5/07

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## Power Integrations Worldwide Sales Support Locations

### World Headquarters

5245 Hellyer Avenue  
San Jose, CA 95138, USA.  
Main: +1-408-414-9200  
Customer Service:  
Phone: +1-408-414-9665  
Fax: +1-408-414-9765  
e-mail: [usasales@powerint.com](mailto:usasales@powerint.com)

### China (Shanghai)

Rm 807-808A  
Pacheer Commercial Centre,  
555 Nanjing Rd. West  
Shanghai, P.R.C. 200041  
Phone: +86-21-6215-5548  
Fax: +86-21-6215-2468  
e-mail: [chinasales@powerint.com](mailto:chinasales@powerint.com)

### China (Shenzhen)

Rm 2206-2207, Block A,  
Electronics Science and  
Technology Bldg.  
2070 Shennan Zhong Rd.  
Shenzhen, Guangdong,  
China, 518031  
Phone: +86-755-8379-3243  
Fax: +86-755-8379-5828  
e-mail: [chinasales@powerint.com](mailto:chinasales@powerint.com)

### Germany

Rueckertstrasse 3  
D-80336, Munich  
Germany  
Phone: +49-89-5527-3910  
Fax: +49-89-5527-3920  
e-mail: [eurosales@powerint.com](mailto:eurosales@powerint.com)

### India

#1, 14th Main Road  
Vasanthanagar  
Bangalore-560052 India  
Phone: +91-80-4113-8020  
Fax: +91-80-4113-8023  
e-mail: [indiasales@powerint.com](mailto:indiasales@powerint.com)

### Italy

Via De Amicis 2  
20091 Bresso MI  
Italy  
Phone: +39-028-928-6000  
Fax: +39-028-928-6009  
e-mail: [eurosales@powerint.com](mailto:eurosales@powerint.com)

### Japan

1st Bldg Shin-Yokohama  
2-12-20 Kohoku-ku,  
Yokohama-shi, Kanagawa  
ken, Japan 222-0033  
Phone: +81-45-471-1021  
Fax: +81-45-471-3717  
e-mail: [japansales@powerint.com](mailto:japansales@powerint.com)

### Korea

RM 602, 6FL  
Korea City Air Terminal B/D, 159-6  
Samsung-Dong, Kangnam-Gu,  
Seoul, 135-728, Korea  
Phone: +82-2-2016-6610  
Fax: +82-2-2016-6630  
e-mail: [koreasales@powerint.com](mailto:koreasales@powerint.com)

### Singapore

51 Newton Road  
#15-08/10 Goldhill Plaza  
Singapore, 308900  
Phone: +65-6358-2160  
Fax: +65-6358-2015  
e-mail: [singaporesales@powerint.com](mailto:singaporesales@powerint.com)

### Taiwan

5F, No. 318, Nei Hu Rd., Sec. 1  
Nei Hu Dist.  
Taipei, Taiwan 114, R.O.C.  
Phone: +886-2-2659-4570  
Fax: +886-2-2659-4550  
e-mail: [taiwansales@powerint.com](mailto:taiwansales@powerint.com)

### Europe HQ

1st Floor, St. James's House  
East Street, Farnham  
Surrey GU9 7TJ  
United Kingdom  
Phone: +44 (0) 1252-730-140  
Fax: +44 (0) 1252-727-689  
e-mail: [eurosales@powerint.com](mailto:eurosales@powerint.com)

### Applications Hotline

World Wide +1-408-414-9660

### Applications Fax

World Wide +1-408-414-9760