Design Example Report

Title	***15 W Power Supply with <30 mW No-load Input Power Using TinySwitch-III (TNY278P)***
Specification	85 VAC – 265 VAC Input; 12 V, 1.25 A Output
Application	*TinySwitch-III* Reference Design
Author	Applications Engineering Department
Document Number	DER-228
Date	November 19, 2009
Revision	1.0

Summary and Features

- *EcoSmart*® – Meets all existing and proposed harmonized energy efficiency standards including: CECP (China), CEC, EPA, AGO, European Commission
  - No-load consumption < 30 mW at 230 VAC
  - > 81% active-mode efficiency
    - Exceeds ENERGY STAR v2 / EuP tier 2 requirements of 79%
- BP/M capacitor value selects MOSFET current limit for greater design flexibility
- Tightly toleranced I^2f parameter (–10%, +12%) reduces system cost:
  - Increases MOSFET and magnetics power delivery
  - Reduces overload power, which lowers output diode and capacitor costs
- Integrated *TinySwitch-III* Safety/Reliability features:
  - Accurate (± 5%), auto-recovering, hysteretic thermal shutdown function maintains safe PCB temperatures under all conditions
  - Auto-restart protects against output short circuit and open loop fault conditions
  - > 3.2 mm creepage on package enables reliable operation in high humidity and high pollution environments
- Meets EN550022 and CISPR-22 Class B conducted EMI with >12 dB margin

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Important Note:
Although this board was designed to satisfy safety isolation requirements, it has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the power supply.

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1 Introduction

This report describes a universal input, 12 V, 1.25 A flyback power supply using a TNY278P device from the *TinySwitch-III* family of ICs. The goal of the design was to demonstrate the very low no-load input power that is achievable with *TinySwitch-III* devices

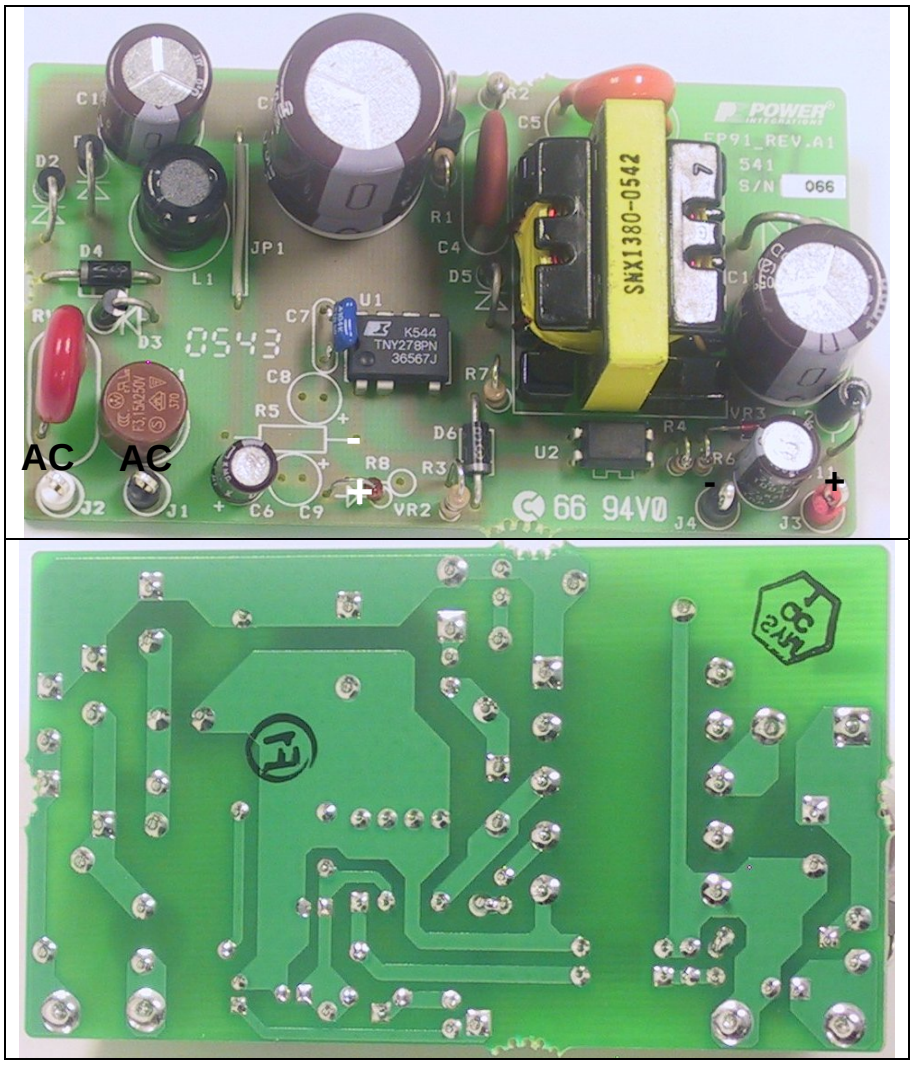

Figure 1 – DER-228 Populated Circuit Board Photographs (3.2 × 1.8 inches).

The design was based on the EP91 reference design board with the only changes being optimization of the bias winding components that supply the operating current into the BYPASS pin of the TNY278P IC and changing the output diode from a PN ultra fast to Schottky barrier type.

The report contains the complete specification of the power supply, a detailed circuit diagram, the entire bill of materials required to build the supply, extensive documentation of the power transformer, along with test data and oscillographs of the most important electrical waveforms. The board provides a number of user configurable options which are designed to demonstrate the features and flexibility of the *TinySwitch-III* family. These include easy adjustment of the device current limit for increased output power or higher efficiency operation, and a latched output overvoltage shutdown.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.03	W	w/o UVLO resistor or bias winding
Output						
Output Voltage	V_{OUT}	11	12	13	V	± 8%
Output Ripple Voltage	V_{RIPPLE}			100	mV	20 MHz bandwidth
Output Current	I_{OUT}	1.25			A	
Total Output Power						
Continuous Output Power	P_{OUT}	15			W	
Efficiency						
Full Load	η	81			%	Measured at P_{OUT} 25 °C
Required average efficiency at 25, 50, 75 and 100 % of P_{OUT}	η_{ES2} η_{EuP}	79			%	Per Energy Star 2.0 standard
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Board size		3.2 x 1.8 81.3 x 45.7			Inches mm	Length x width
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level

3 Circuit Diagram

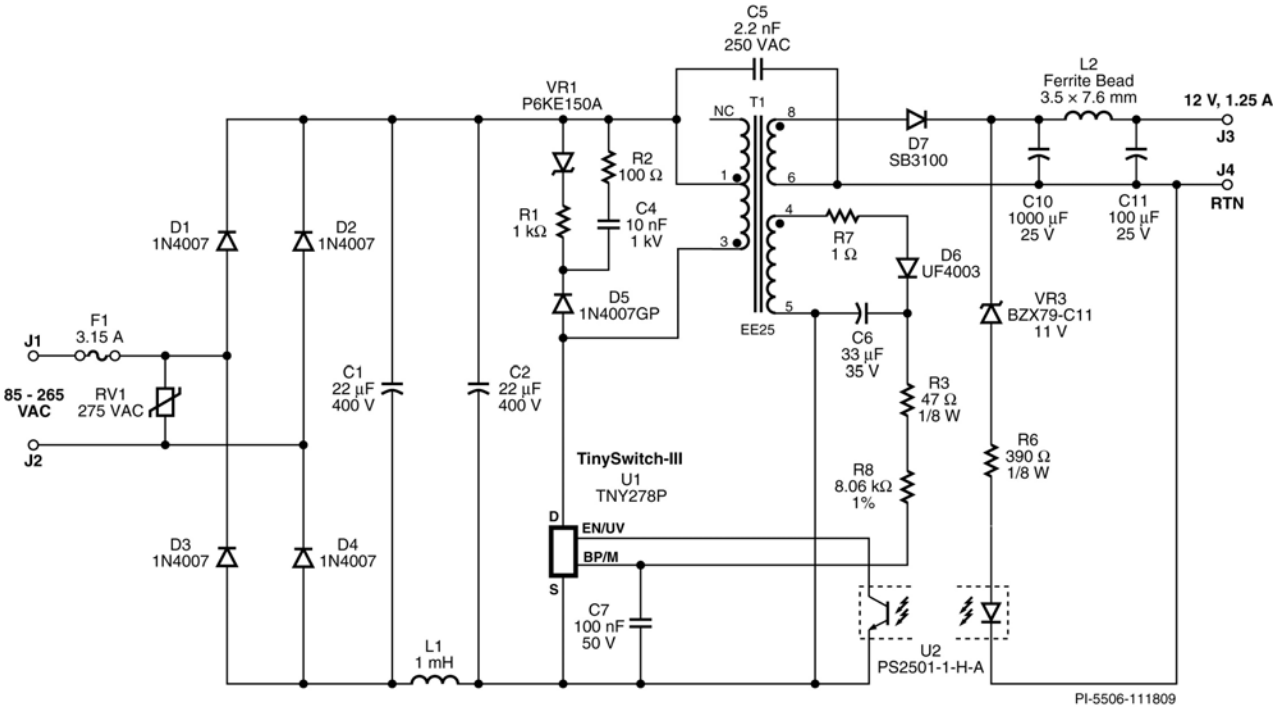

Figure 2 – DER-228 Circuit Diagram.

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4 Circuit Description

This flyback power supply was designed around the TNY278PN (U1 in Figure 2). The output voltage is sensed and fed back to U1 through optocoupler U2. The feedback signal is used to maintain constant voltage (CV) regulation of the output via ON/OFF control.

4.1 Input Rectification and Filtering

Diodes D1–D4 rectify the AC input. Capacitors C1 and C2 filter the rectified DC. Inductor L1, C1 and C2 form a pi filter that attenuates differential mode conducted EMI.

4.2 TNY278PN Operation

The TNY278PN device (U1) integrates an oscillator, a switch controller, startup and protection circuitry, and a power MOSFET, all on one monolithic IC.

One side of the power transformer (T1) primary winding is connected to the positive leg of C2, and the other side is connected to the DRAIN pin of U1. At the start of a switching cycle, the controller turns the MOSFET on and current ramps up in the primary winding, which stores energy in the core of the transformer. When that current reaches the current limit threshold, the controller turns the MOSFET off. Due to the phasing of the transformer windings and the orientation of the output diode, the stored energy then induces a voltage across the secondary winding, which forward biases the output diode, and the stored energy is delivered to the output capacitor.

During MOSFET turns off, the leakage inductance of the transformer induces a voltage spike on the drain node. The amplitude of that spike is limited by an RCDZ clamp network that consists of D5, C4, R2, R1 and VR1. Resistor R2 also limits the reverse current that flows through D5 when the MOSFET turns on. This allows a slow, low-cost, glass passivated diode (with a recovery time of ≤2 μs.) to be used for D5, which improves conducted EMI and efficiency. Alternately a fast diode like that FR106 may be used in place of D5 with a slight reduction in efficiency.

Using ON/OFF control, U1 skips switching cycles to regulate the output voltage, based on feedback to its EN/UV pin. The EN/UV pin current is sampled, just prior to each switching cycle, to determine if that switching cycle should be enabled or disabled. If the EN/UV pin current is <115 μA, the next switching cycle begins, and is terminated when the current through the MOSFET reaches the internal current limit threshold. To evenly spread switching cycles, preventing group pulsing, the EN pin threshold current is modulated between 115 μA and 60 μA based on the state during the previous cycle.

A state-machine within the controller adjusts the MOSFET current limit threshold to one of four levels, depending on the load being demanded from the supply. As the load on the supply drops, the current limit threshold is reduced. This ensures that the effective switching frequency stays above the audible range until the transformer flux density is

low. When the standard production technique of dip varnishing is used for the transformer, audible noise is practically eliminated.

4.3 Bias Winding Design

Although a bias winding is not necessary for the operation of the TinySwitch-III family, its use greatly reduces the no load consumption of a power supply. During steady state operation the bias winding supplies the IC bias current. Resistors R3 and R8 were adjusted to minimize the no-load input power by providing the supply current required by U1 at no-load.

4.4 Output Rectification and Filtering

Diode D7 rectifies the output of T1. A schottky barrier type was selected to improve efficiency. Output voltage ripple was minimized by using a low ESR capacitor for C10 (see Section 6 for component part numbers and values). A post filter (ferrite bead L2 and C11) attenuates the high frequency switching noise.

4.5 Feedback and Output Voltage Regulation

The supply's output voltage regulation set-point is set by the voltage that develops across Zener diode VR3, R6 and the LED in opto-coupler U2. Resistor R6 limits the maximum current through U2 during load transients. The value of resistor R6 can be varied slightly to fine-tune the output regulation set point. When the output voltage rises above the set point, the LED in U2 becomes forward biased. On the primary side, the photo-transistor of U2 turns on and draws current out of the EN/UV pin of U1. Just before the start of each switching cycle, the controller checks the EN/UV pin current. If the current flowing out of the EN/UV pin is greater than 115 μA, that switching cycle will be disabled. As switching cycles are enabled and disabled, the output voltage is kept very close to the regulation set point. For greater output voltage regulation accuracy, a reference IC such as a TL431 can be used in place of Zener diode VR3.

4.6 EMI Design Aspects

An input pi filter (C1, L1 and C2) attenuates conducted, differential mode EMI noise. Shielding techniques (*E-Shield*™) were used in the construction of T1 to reduce common mode EMI displacement currents. When combined with the IC's frequency jitter function, these techniques produce excellent conducted EMI performance.

4.7 Peak Primary Current Limit Selection

The value of the capacitor installed on the BP/M pin allows the current limit of U1 to be selected. The power supply designer can change the current limit of the MOSFET by simply changing the capacitance value connected to the BP/M pin (see the *TinySwitch-III* data sheet for more details).

- Installing a 0.1 μF capacitor on the BP/M pin selects the standard current limit of the IC, and is the normal choice for enclosed adapter applications.

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- Installing a 1 μF capacitor on the BP/M pin reduces the MOSFET current limit, which lowers conduction losses and improves efficiency (at the expense of reducing the maximum power capability of the IC).

- A 10 μF capacitor on the BP/M pin will raise the MOSFET current limit and extend the power capability of the IC (for higher power applications that do not have the thermal constraints of an enclosed adapter, or to supply short-duration, peak load demands).

The DER-228 board comes with a 0.1 μF capacitor installed as C7, which causes U1 to select the standard current limit specified in the *TinySwitch-III* data sheet. If C7 were replaced by a 1 μF capacitor (C8 in the BOM, section 6), the current limit of U1 would be the same as the standard current limit for a TNY277 device. If a 10 μF capacitor is installed, the current limit of U1 will be the same as the standard current limit for a TNY279 device. The flexibility of this option enables the designer to do three things. First, it allows the designer to measure the effect of switching to an adjacent device without actually removing and replacing the IC. Second, it allows a larger device to be used with a lower current limit, for higher efficiency. Third, it allows a smaller device to be used with a higher current limit in a design when higher power is not required on a continual basis, which effectively lowers the cost of the supply.

5 PCB Layout

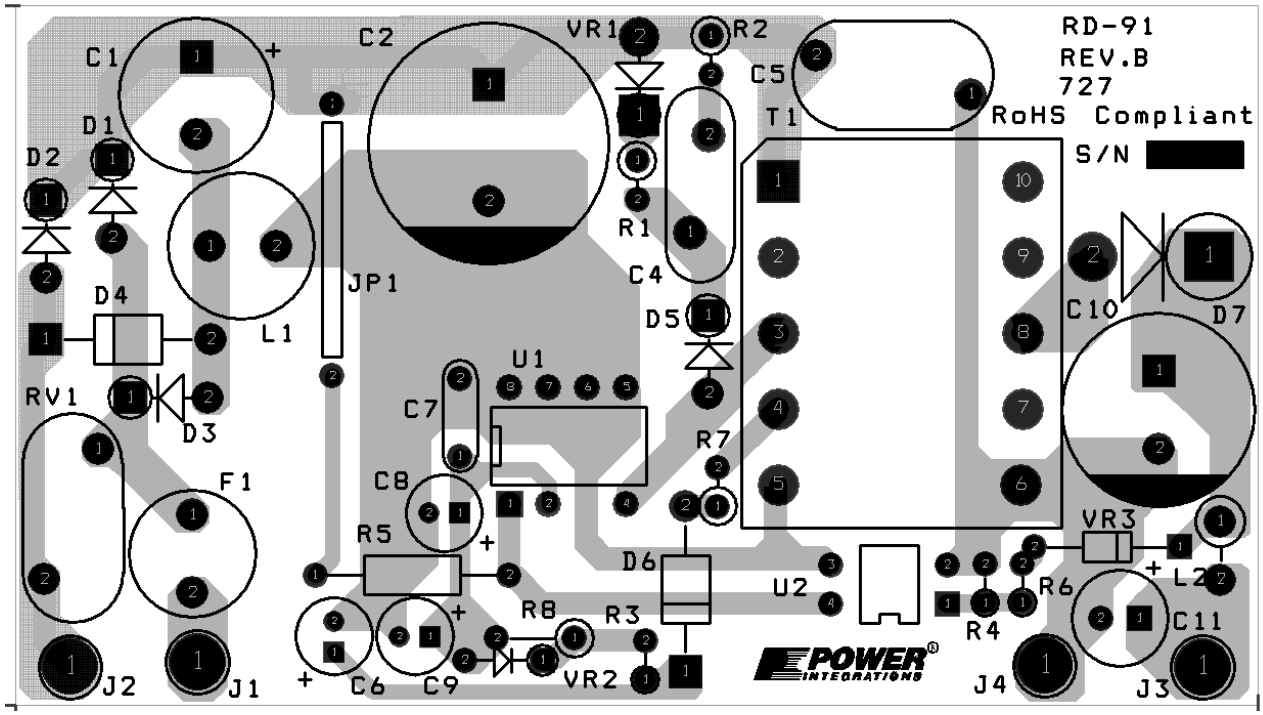

Figure 3 – Printed Circuit Board Layout (3.2 × 1.8 inches).

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg	Mfg Part Number
1	1	C1	22 µF, 400 V, Electrolytic, High Ripple, (12.5 x 25)	Panasonic	EEU-EB2G220
2	1	C2	22 µF, 400 V, Electrolytic, Low ESR, 901 mΩ, (16 x 20)	Nippon Chemi-Con	EKMX401ELL220ML20S
3	1	C4	OBSOLETE not RoHS compliant see 20-00634-00 10 nF, 1 kV, Disc Ceramic	Vishay	5HKMS10
4	1	C5	2.2 nF, Ceramic, Y1	Vishay	440LD22-R
5	1	C6	33 µF, 35 V, Electrolytic, Very Low ESR, 300 mΩ, (5 x 11)	Nippon Chemi-Con	EKZE350ELL330ME11D
6	1	C7	100 nF, 50 V, Ceramic, X7R	Epcos	B37987F5104K000
7	1	C10	1000 µF, 25 V, Electrolytic, Very Low ESR, 21 mΩ, (12.5 x 20)	Nippon Chemi-Con	EKZE250ELL102MK20S
8	1	C11	100 µF, 25 V, Electrolytic, Very Low ESR, 130 mΩ, (6.3 x 11)	Nippon Chemi-Con	EKZE250ELL101MF11D
9	4	D1 D2 D3 D4	1000 V, 1 A, Rectifier, DO-41	Vishay	1N4007
10	1	D5	1000 V, 1 A, Rectifier, Glass Passivated, 2 µs, DO-41	Vishay	1N4007GP
11	1	D6	200 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	Vishay	UF4003-E3
12	1	D7	100 V, 3 A, Schottky, DO-201AD	Vishay	SB3100
13	1	F1	3.15 A, 250V,Fast, TR5	Wickman	37013150410
14	2	J1 J4	Test Point, BLK,THRU-HOLE MOUNT	Keystone	5011
15	1	J2	Test Point, WHT,THRU-HOLE MOUNT	Keystone	5012
16	1	J3	Test Point, RED,THRU-HOLE MOUNT	Keystone	5010
17	1	JP1	Wire Jumper, Non insulated, 22 AWG, 0.7 in	Alpha	298
18	1	L1	1mH, 350m A		HTB2-102-281
19	1	L2	3.5 mm x 7.6 mm, 75 Ω at 25 MHz, 22 AWG hole, Ferrite Bead	Fair-Rite	2743004112
20	1	R1	1 kΩ, 5%, ¼ W, Carbon Film	Yageo	CFR-25JB-1K0
21	1	R2	100 Ω, 5%, 1/4 W, Carbon Film	Yageo	CFR-25JB-100R
22	1	R3	47 Ω, 5%, 1/8 W, Carbon Film	Yageo	CFR-12JB-47R
23	1	R6	390 Ω, 5%, 1/8 W, Carbon Film	Yageo	CFR-12JB-390R
24	1	R7	1 Ω, 5%, 1/4 W, Carbon Film	Yageo	CFR-25JB-1R0
25	1	R8	8.06 kΩ, 1/4 W, Metal Film	Yageo	MFR-25FBF-8K06
26	1	RV1	275 V, 45 J, 10 mm, RADIAL	Littlefuse	V275LA10
27	1	T1	Transformer, 10 Pins, Vertical	Yih-Hwa Enterprises	YW-360-02B
28	1	U1	TinySwitch-III, TNY278PN, DIP-8C	Power Integrations	TNY278PN
29	1	U2	Opto coupler, 80 V, CTR 80-160%, 4-DIP	NEC	PS2501-1-H-A
30	1	VR1	150 V, 6005 W, 5%, TVS, DO204AC (DO-15)	Littlelfuse	P6KE150A
31	1	VR3	11 V, 500 mW, 5%, DO-35	Vishay	BZX55-C11

* Optional components

Note – All parts are RoHS compliant

7 Transformer Specification

7.1 Electrical Diagram

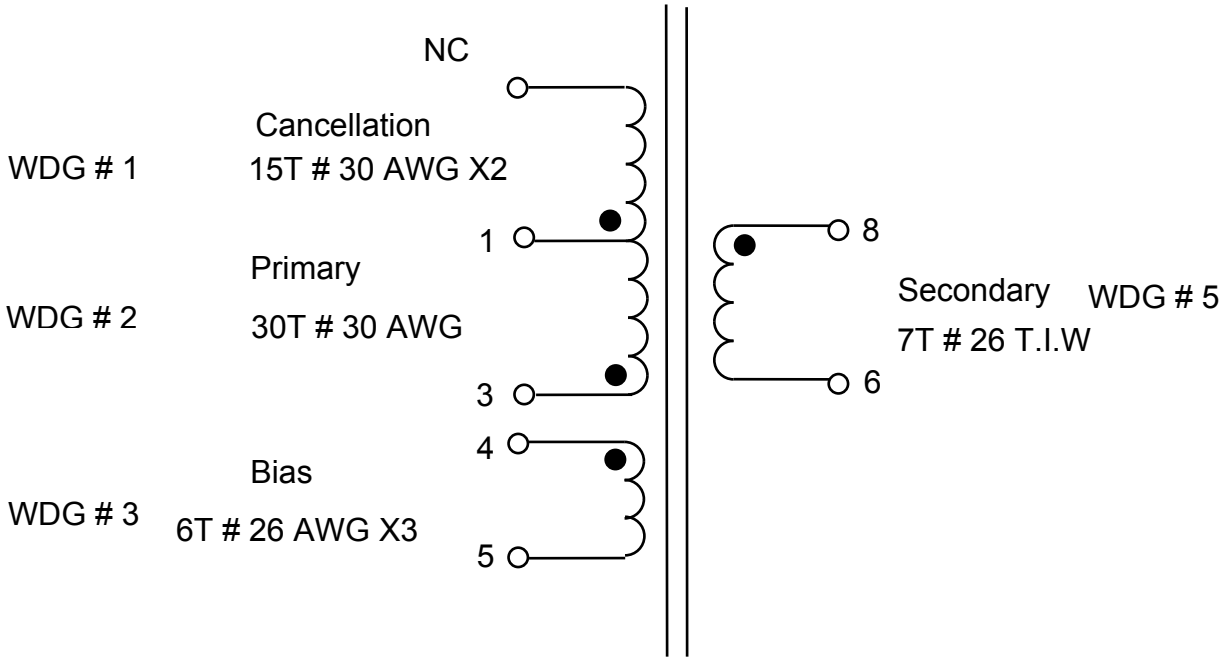

Figure 4 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-5 to pins 6-10	3000 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 V RMS	1170 μH, ±10%
Resonant Frequency	Pins 1-3, all other windings open	500 kHz (Min.)
Primary Leakage Inductance	Pins 1-3, with pins 6-8 shorted, measured at 100 kHz, 0.4 V RMS	50 μH (Max.)

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7.3 Materials

Item	Description
[1]	Core: PC40EE25-Z, TDK or equivalent gapped for A_L of 323 nH/T^2
[2]	Bobbin: EE25, Vertical, 10 pin – Yih-Hwa part # YW-360-02B
[3]	Magnet Wire: #30 AWG
[4]	Magnet Wire: #26 AWG
[5]	Triple Insulated Wire: #26 AWG.
[6]	Tape: 3M # 44 Polyester web. 2.0 mm wide
[7]	Tape: 3M 1298 Polyester Film, 2.0 mils thick, 8.6 mm wide
[8]	Tape: 3M 1298 Polyester Film, 2.0 mils thick, 10.7 mm wide
[9]	Tape: 3M 1298 Polyester Film, 2.0 mils thick, 4.0 mm wide
[10]	Varnish (applied by dipping only, not vacuum impregnation)

7.4 Transformer Build Diagram

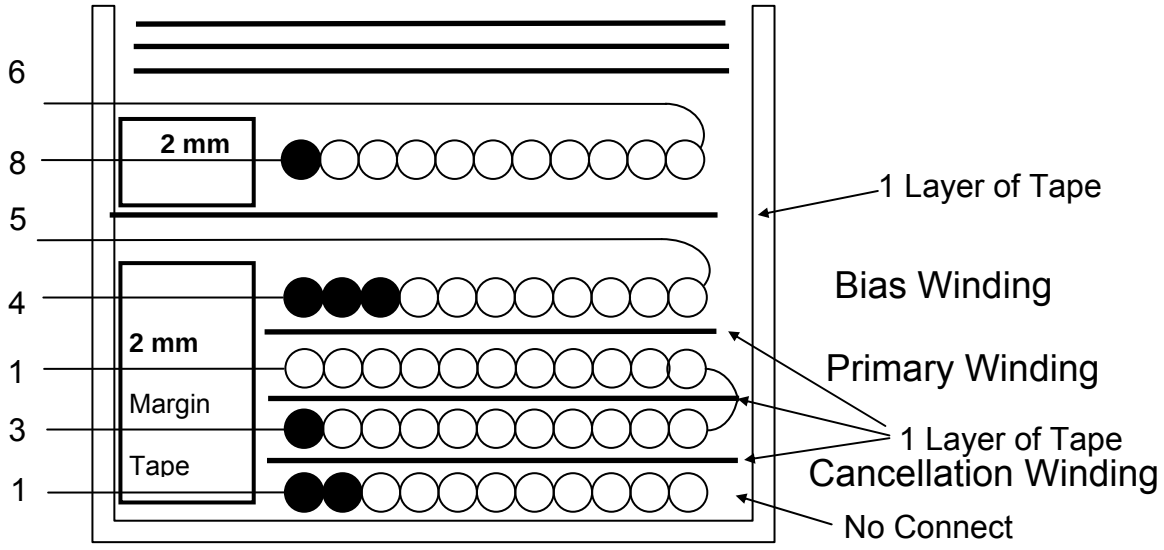

Figure 5 – Transformer Build Diagram.

7.5 Transformer Construction

Bobbin Set Up Orientation	Set up the bobbin with its pins oriented to the left hand side.
Margin Tape	Apply 2.0 mm margin at the pin side of bobbin using item [6]. Match combined height of shield, primary, and bias windings.
WD1 Cancellation Winding	Start at Pin 1. Wind 15 bifilar turns of item [3] from left to right. Wind with tight tension across entire bobbin evenly. Cut the ends of the bifilar and leave floating.
Insulation	1 Layer of tape [7] for insulation.
WD#2 Primary winding	Start at pin 3. Wind 30 turns of item [3] from left to right. Apply 1 Layer of tape [7] for insulation. Wind another 30 turns from right to left. Wind with tight tension across entire bobbin evenly. Finish at pin 1.
Insulation	1 Layer of tape [7] for insulation.
WD #3 Bias Winding	Start at pin 4, wind 6 trifilar turns of item [5]. Wind from left to right with tight tension. Wind uniformly, in a single layer across entire width of bobbin. Finish on pin 5.
Insulation	1 Layer of tape [8] for insulation.
Margin Tape	Apply 2.0 mm margin at the pin side of bobbin using item [6]. Match combined height of secondary windings.
WD #5 Secondary Winding	Start at pin 8, wind 7 turns of item [5] from left to right. Wind uniformly, in a single layer across entire bobbin evenly. Finish on pin 6.
Outer Insulation	3 Layers of tape [8] for insulation.
Core Assembly	Assemble and secure core halves using item [1] and item [9].
Varnish	Dip varnish using item [10] (do not vacuum impregnate.)

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8 Transformer Design Spreadsheet

ACDC_TinySwitch-III _032608; Rev.1.26; Copyright Power Integrations 2008	INPUT	INFO	OUTPUT	UNIT	ACDC_TinySwitch-III_032608_Rev1-26.xls; TinySwitch-III Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	12.00			Volts	Output Voltage (at continuous power)
IO	1.25			Amps	Power Supply Output Current (corresponding to peak power)
Power			15	Watts	Continuous Output Power
n	0.82				Efficiency Estimate at output terminals. Under 0.7 if no better data available
Z	0.50				Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC	3.00			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	44.00		44	uFarads	Input Capacitance
ENTER TinySwitch-III VARIABLES					
TinySwitch-III	TNY278		TNY278		User defined TinySwitch-III
Chosen Device		TNY278			
Chose Configuration	STD		Standard Current Limit		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.512	Amps	Minimum Current Limit
ILIMITTYP			0.550	Amps	Typical Current Limit
ILIMITMAX			0.588	Amps	Maximum Current Limit
fSmin			124000	Hertz	Minimum Device Switching Frequency
I^2fmin			35.937	A^2kHz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	108.00		108	Volts	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10	Volts	TinySwitch-III on-state Drain to Source Voltage
VD	0.55		0.55	Volts	Output Winding Diode Forward Voltage Drop
KP			0.64		Ripple to Peak Current Ratio (KP < 6)
KP_TRANSIENT			0.37		Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB	11		11.00	Volts	Bias Winding Voltage
VDB			0.70	Volts	Bias Winding Diode Forward Voltage Drop
NB			6.14		Bias Winding Number of Turns
VZOV			17.00	Volts	Over Voltage Protection zener diode voltage.
UVLO VARIABLES					
V_UV_TARGET	92		92.00	Volts	Target DC under-voltage threshold, above which the power supply with start
V_UV_ACTUAL			92.20	Volts	Typical DC start-up voltage based on standard value of RUV_ACTUAL
RUV_IDEAL			3.59	Mohms	Calculated value for UV Lockout resistor
RUV_ACTUAL			3.60	Mohms	Closest standard value of resistor to RUV_IDEAL
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EE25		EE25		Enter Transformer Core
Core		EE25			P/N:
Bobbin		EE25_BOBBIN		P/N:	EE25_BOBBIN
AE			0.404	cm^2	Core Effective Cross Sectional Area
LE			7.34	cm	Core Effective Path Length

AL			1420	nH/T^2	Ungapped Core Effective Inductance
BW			10.2	mm	Bobbin Physical Winding Width
M	1.00		1	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	2.00		2		Number of Primary Layers
NS	7		7		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			93	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.57		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.22	Amps	Average Primary Current
IP			0.51	Amps	Minimum Peak Primary Current
IR			0.33	Amps	Primary Ripple Current
IRMS			0.31	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			1170	uHenries	Typical Primary Inductance. +/- 10% to ensure a minimum primary inductance of 1064 Uh
LP_TOLERANCE	10.00		10	%	Primary inductance tolerance
NP			60		Primary Winding Number of Turns
ALG			323	nH/T^2	Gapped Core Effective Inductance
BM			2828	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
BAC			905	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			2053		Relative Permeability of Ungapped Core
LG			0.12	mm	Gap Length (Lg > 0.1 mm)
BWE			16.4	mm	Effective Bobbin Width
OD			0.27	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.22	mm	Bare conductor diameter
AWG			32	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			64	Cmils	Bare conductor effective area in circular mils
CMA			205	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			4.41	Amps	Peak Secondary Current
ISRMS			2.35	Amps	Secondary RMS Current
IRIPPLE			1.99	Amps	Output Capacitor RMS Ripple Current
CMS			470	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			23	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			622	Volts	Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance)

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9 Performance Data

The ON/OFF control scheme employed by *TinySwitch-III* yields virtually constant efficiency across the 25% to 100% load range required for compliance with ENERGY STAR and EuP energy efficiency standards for external power supplies (EPS). Even at loads below 10% of the supply's full rated output power, efficiency remains above 75%, providing excellent standby performance for applications that require it. This performance is automatic with ON/OFF control. There are no special burst modes that require the designer to consider specific thresholds within the load range in order to achieve compliance with global energy efficiency standards.

All measurements performed at room temperature, 60 Hz input frequency.

9.1 Active Mode Efficiency

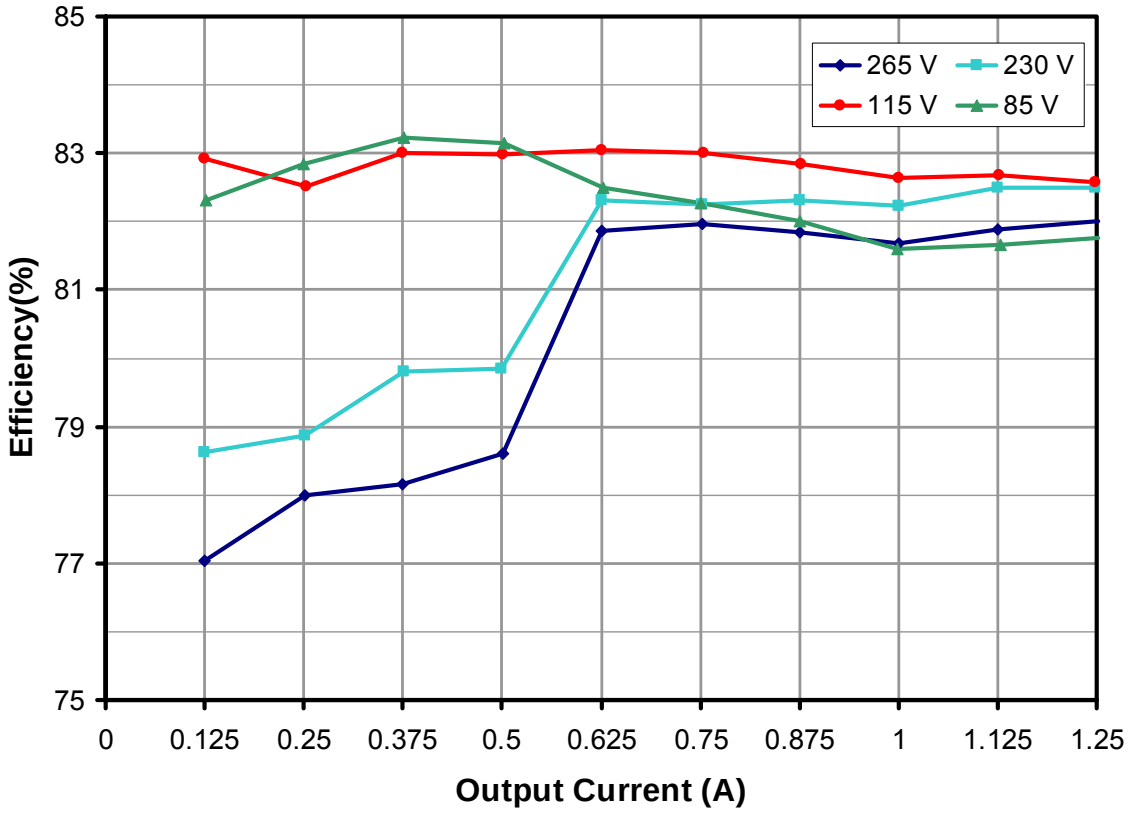

Figure 6 – Efficiency vs. Output Current, Room Temperature, 60 Hz..

Percent of Full Load	Efficiency (%)	
	115 VAC	230 VAC
25	82.4	79.2
50	82.7	81.8
75	82.6	82.0
100	82.5	82.4
Average	**82.5**	**81.4**
Requirements		
US EISA (2007)	74	
ENERGY STAR 2.0	79	
EuP (tier 2)	79	

9.2 Energy Efficiency Requirements

The external power supply requirements below all require meeting active mode efficiency and no-load input power limits. Minimum active mode efficiency is defined as the average efficiency of 25, 50, 75 and 100% of output current (based on the nameplate output current rating).

For adapters that are single input voltage only then the measurement is made at the rated single nominal input voltage (115 VAC or 230 VAC), for universal input adapters the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the standard.

The test method can be found here:

http://www.energystar.gov/ia/partners/prod_development/downloads/power_supplies/EPSupplyEffic_TestMethod_0804.pdf

For the latest up to date information please visit the PI Green Room:

http://www.powerint.com/greenroom/regulations.htm

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9.2.1 USA Energy Independence and Security Act 2007

This legislation mandates all single output single output adapters, including those provided with products, manufactured on or after July 1st, 2008 must meet minimum active mode efficiency and no load input power limits.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
< 1 W	$0.5 \times P_O$
≥ 1 W to ≤ 51 W	$0.09 \times \ln(P_O) + 0.5$
> 51 W	0.85

ln = natural logarithm

No-load Energy Consumption

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
All	≤ 0.5 W

This requirement supersedes the legislation from individual US States (for example CEC in California).

9.2.2 ENERGY STAR EPS Version 2.0

This specification takes effect on November 1st, 2008.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.48 \times P_O + 0.14$
> 1 W to ≤ 49 W	$0.0626 \times \ln(P_O) + 0.622$
> 49 W	0.87

ln = natural logarithm

Active Mode Efficiency Low Voltage Models (V_O<6 V and $I_O \geq 550$ mA)

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.497 \times P_O + 0.067$
> 1 W to ≤ 49 W	$0.075 \times \ln(P_O) + 0.561$
> 49 W	0.86

ln = natural logarithm

No-load Energy Consumption (both models)

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
0 to < 50 W	≤ 0.3 W
≥ 50 W to ≤ 250 W	≤ 0.5 W

9.3 No-load Input Power

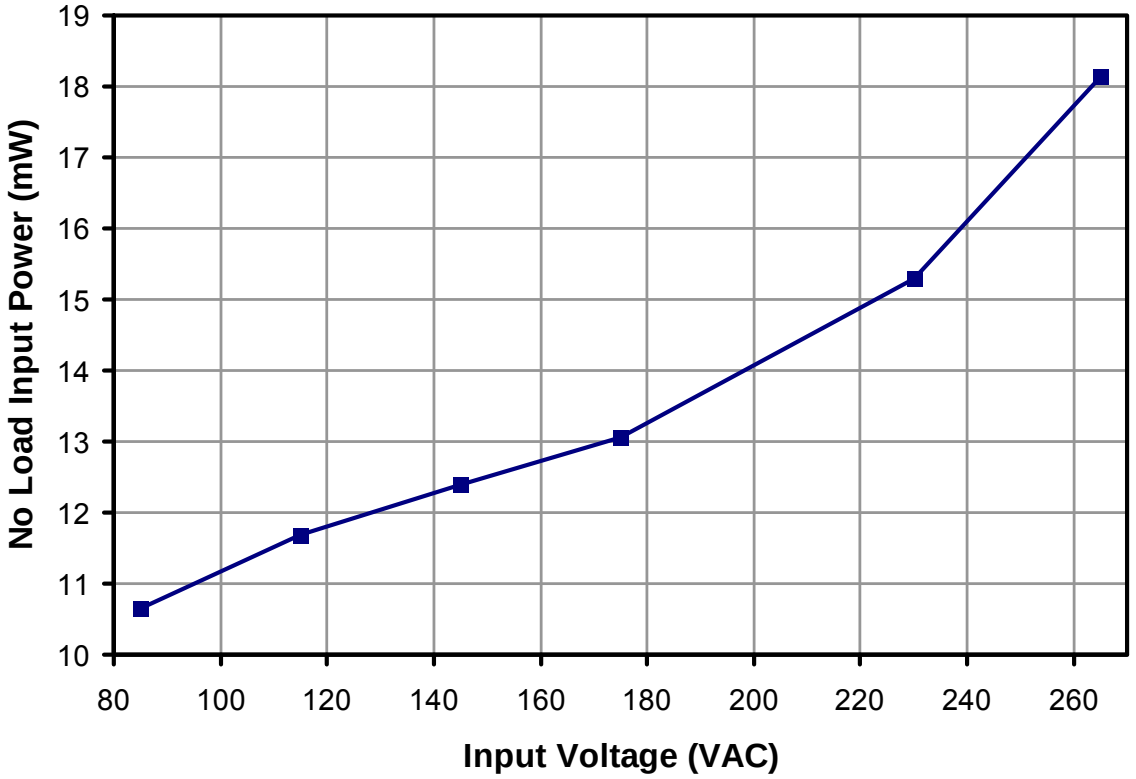

Figure 7 – No-load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

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9.4 Available Output Power vs Input Power (230 VAC)

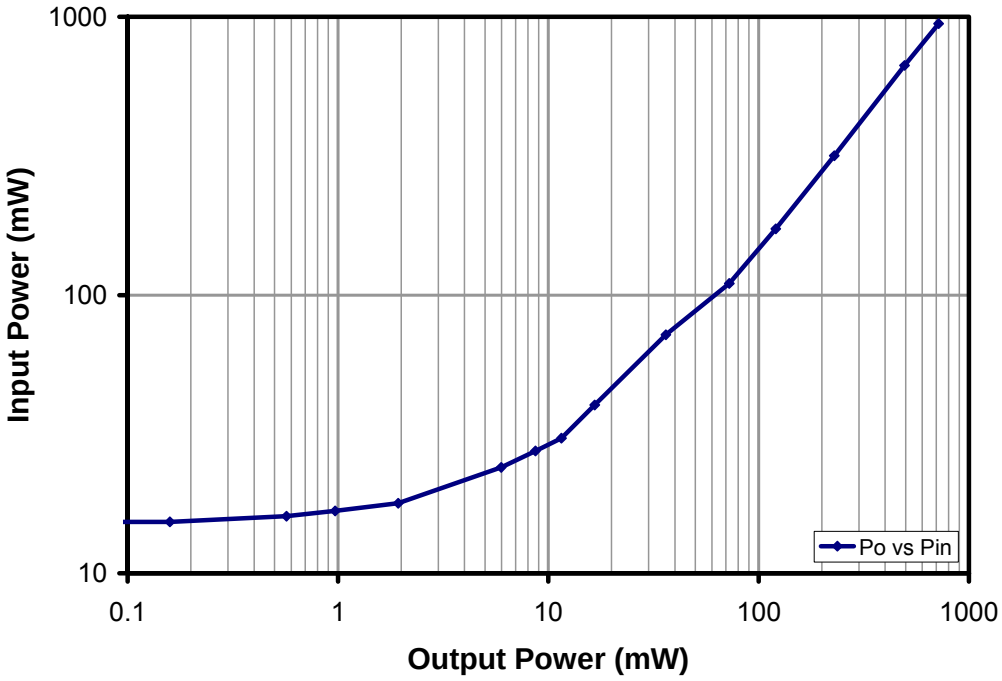

Figure 8a – Output Power vs Input Power at 230 VAC, Room Temperature, 60 Hz.
(No-load to 1 W Input.)

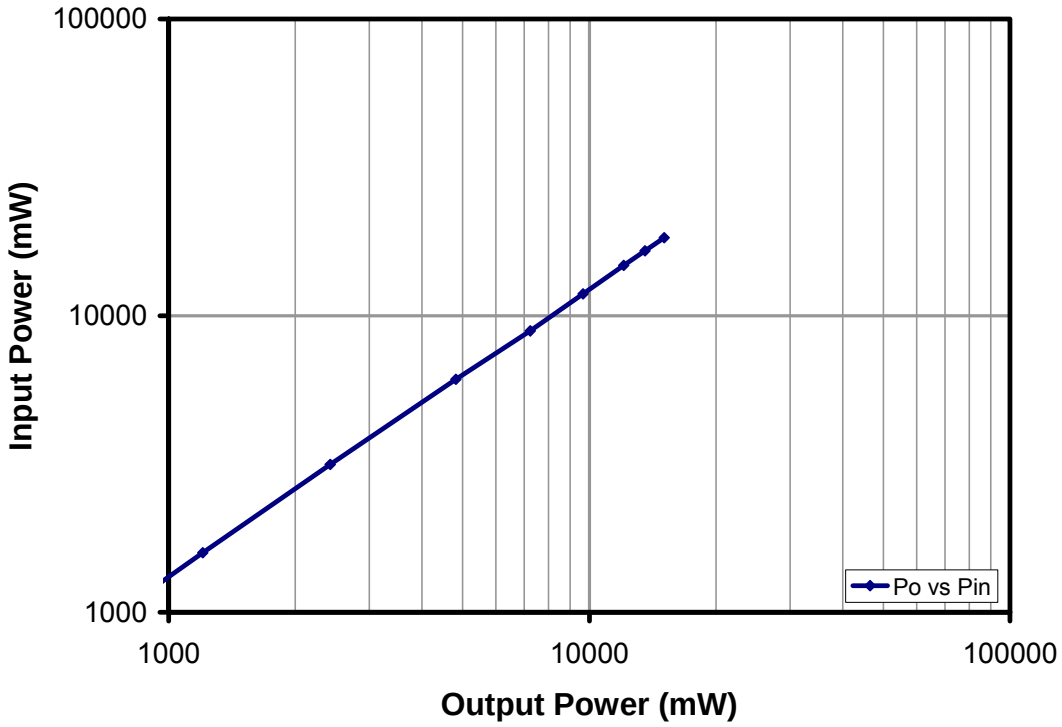

Figure 8b – Output Power vs Input Power at 230 VAC, Room Temperature, 60 Hz.
(1 W Input to 15 W Input.)

9.5 Available Standby Output Power

The chart below shows the available output power versus line voltage at input power consumption levels of 1, 2 and 3 watts (respectively). Again, this performance illustrates the value of ON/OFF control, as it automatically maintains a high efficiency, even during very light loading. This simplifies complying with standby requirements that specify that a fair amount of power be available to the load at low input power consumption levels. The *TinySwitch-III* ON/OFF control scheme maximizes the amount of output power available to the load in standby operation when the allowable input power is fixed at a low value. This simplifies the design of products such as printers, set-top boxes, DVD players, etc. that must meet stringent standby power consumption requirements.

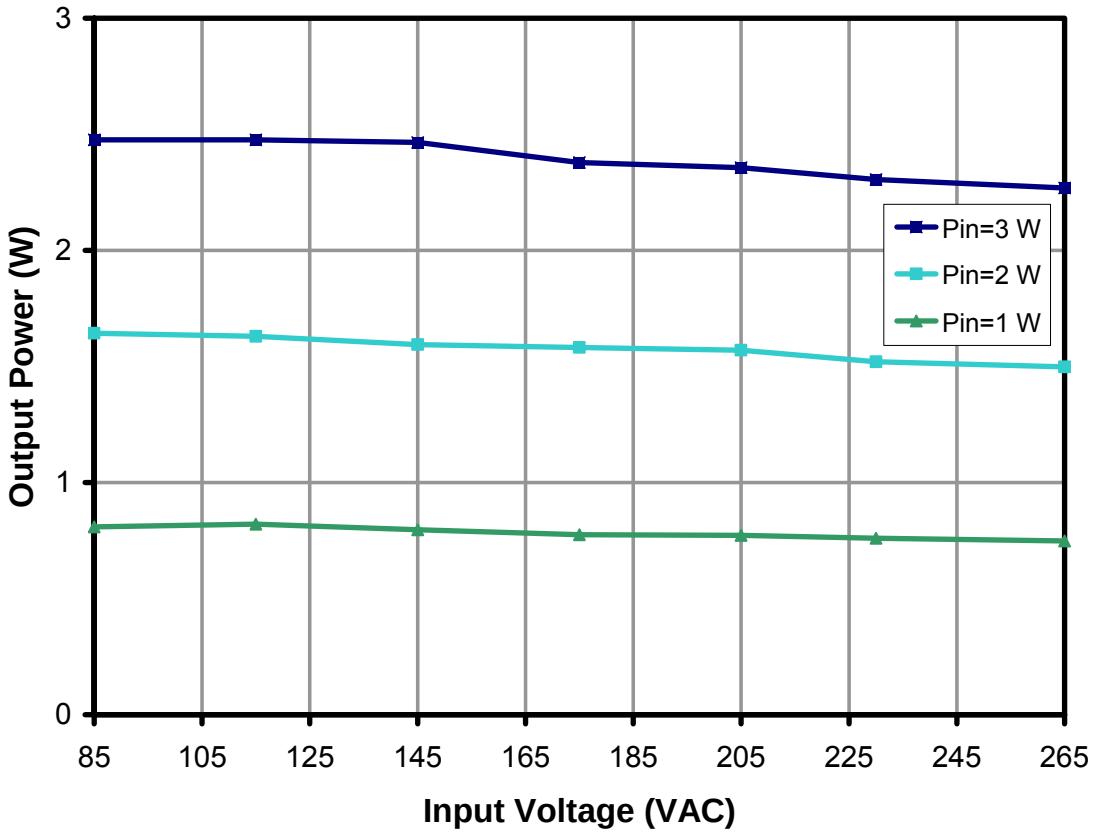

Figure 9 – Available Output Power for 1, 2 and 3 Watts of Input Power.

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9.6 Regulation

9.6.1 Load and Line

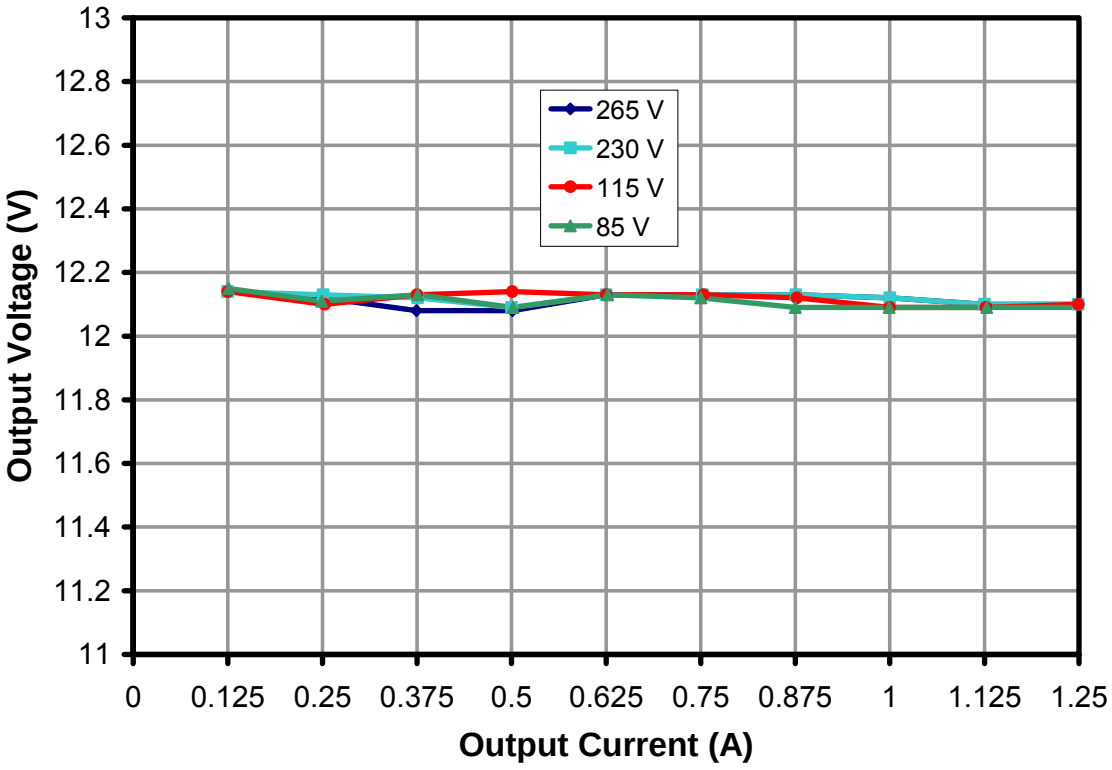

Figure 10 – Load and Line Regulation, Room Temperature.

10 Thermal Performance

Temperature measurements of key components were taken using t-type thermocouples. The thermocouples were soldered directly to a Source pin of the TNY278PN device and to the cathode of the output rectifier. The thermocouples were glued to the external core and winding surfaces of transformer T1.

The unit was sealed inside a large box to eliminate any air currents. The box was placed inside a thermal chamber. The ambient temperature within the large box was raised to 50 °C. The unit was then operated at full load and the temperature measurements were taken after they stabilized for 1 hour at 50 °C.

Temperature (°C)		
Item	**85 VAC**	**265 VAC**
Ambient inside the box	50*	50*
TNY278PNP (U1)	95	92
Transformer winding(T1)	83	88
Transformer core (T1)	74	81
Output Rectifier (D7)	99	101

*To simulate operation inside sealed enclosure at 40 °C external ambient.

These results show that all key components have an acceptable rise in temperature.

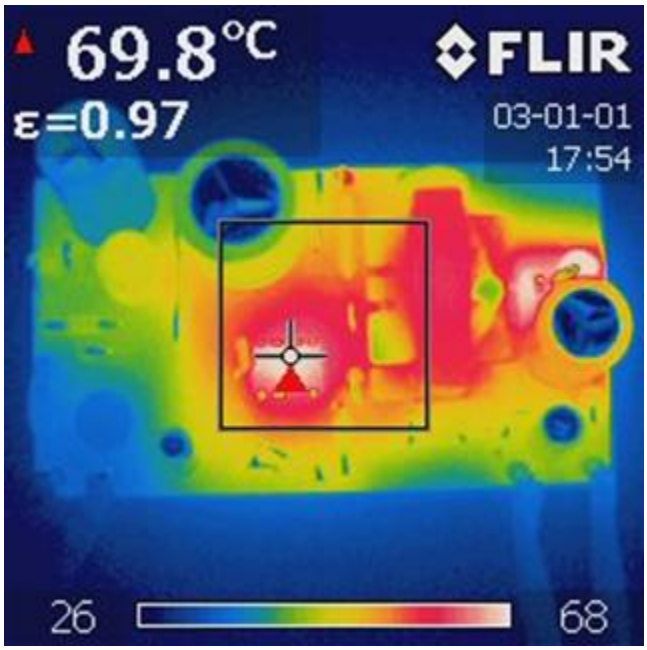

Figure 11 – Infrared Thermograph of Open Frame Operation, at Room Temperature. Cursor indicatesplastic temperature of U1

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11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

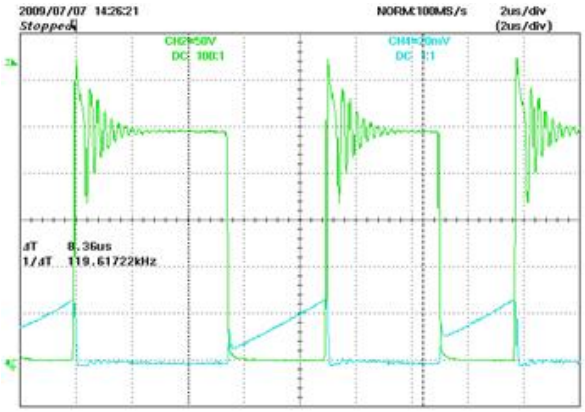

Figure 12 – 115 VAC, Full Load.
Upper: I_{DRAIN}, 0.4 A / div.
Lower: V_{DRAIN}, 50 V / div, 2 μs / div.

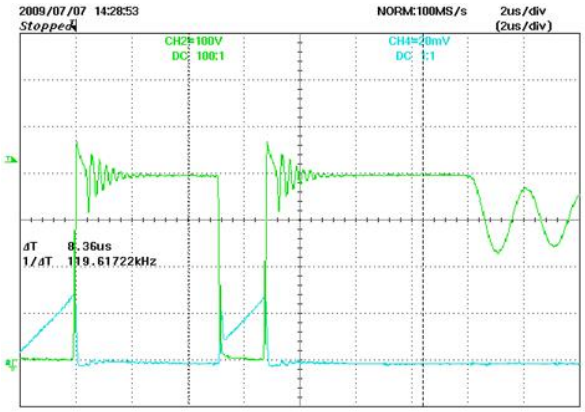

Figure 13 – 230 VAC, Full Load.
Upper: I_{DRAIN}, 0.4 A / div.
Lower: V_{DRAIN}, 100 V / div. 2 μs / div

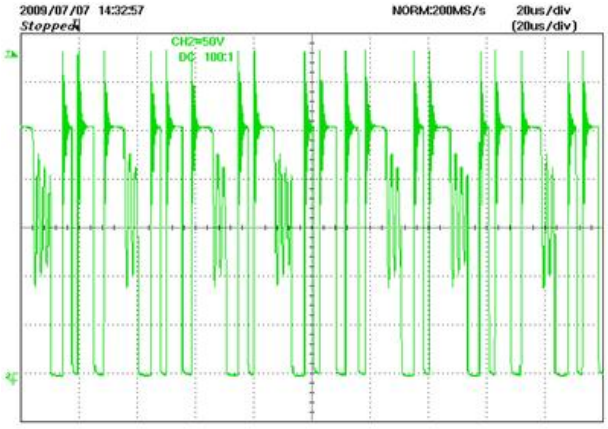

Figure 14 – 115 VAC, Full Load.
V_{DRAIN}, 50 V, 20 μs / div.

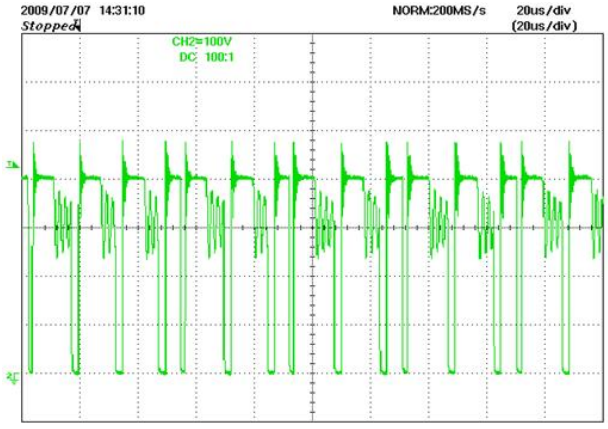

Figure 15 – 230 VAC, Full Load.
V_{DRAIN}, 100 V, 20 μs / div.

11.2 Output Voltage Start-Up Profile

Start-up into full resistive load and no-load were both verified. A 12 Ω resistor was used for the load, to maintain 1 A under steady-state conditions.

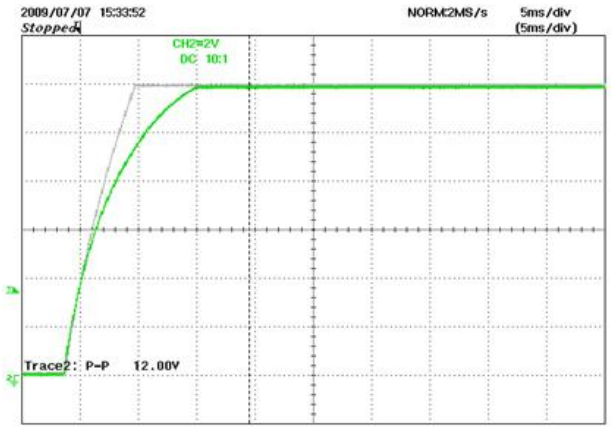

Figure 16 – Start-Up Profile, 115 VAC.
Fast Trace is No-load Rise Time
Slower Trace is Maximum Load
2 V, 5 ms / div.

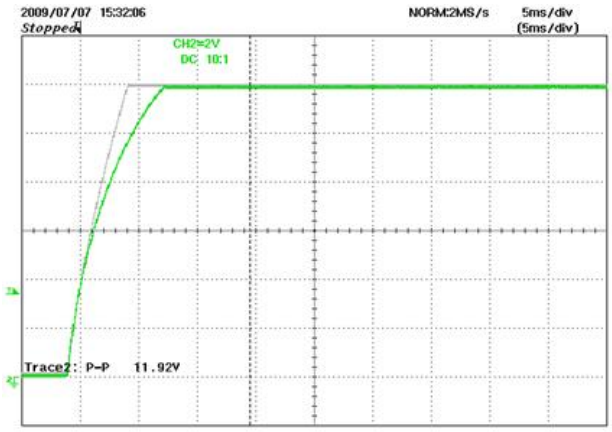

Figure 17 – Start-Up Profile, 230 VAC.
Fast Trace is No-load Rise Time
Slower Trace is Maximum Load
2 V, 5 ms / div.

11.3 Drain Voltage and Current Start-Up Profile

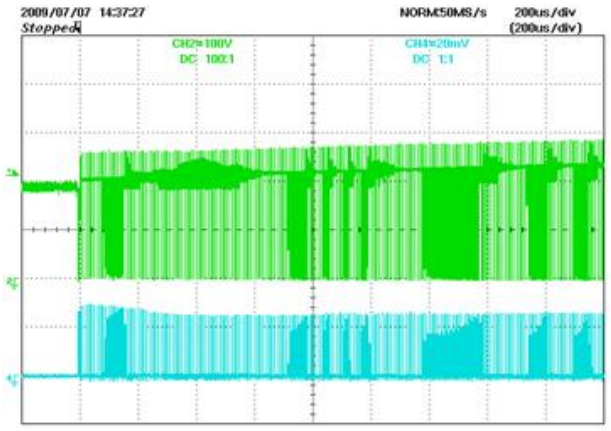

Figure 18 – 85VAC Input and Maximum Load.
Upper: V_{DRAIN}, 100 V & 200 μs / div.
Lower: I_{DRAIN}, 0.4 A / div.

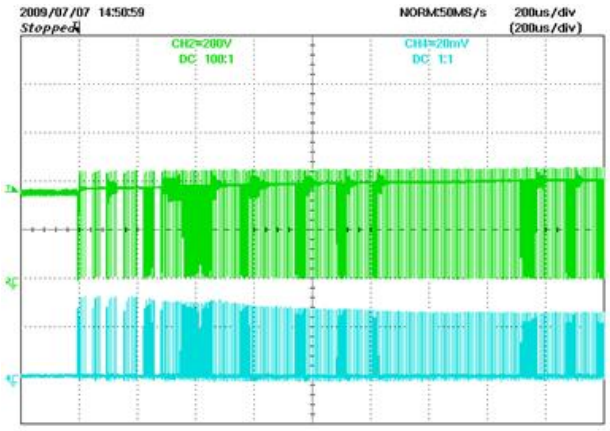

Figure 19 – 265 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 200 V & 200 μs / div.
Lower: I_{DRAIN}, 0.4 A / div.

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11.4 Load Transient Response (75% to 100% Load Step)

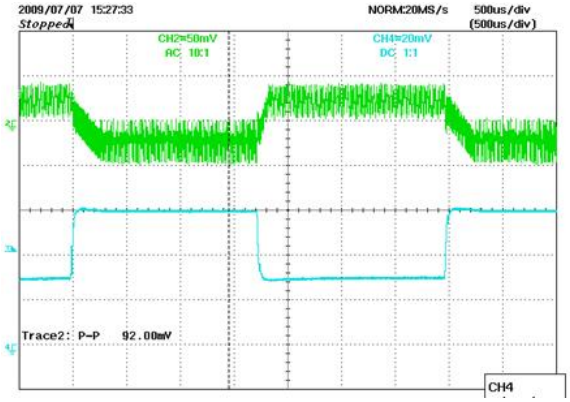

Figure 20 – Transient Response, 115 VAC, 50-100-50% Load Step. Upper: V_{OUT} 50 mV / div. Lower: I_{OUT} 0.4 A, 0.5 ms / div.

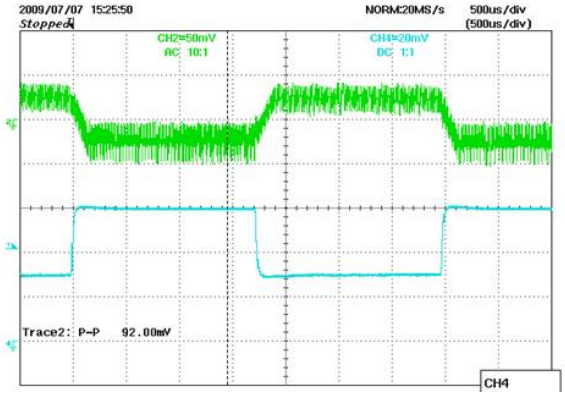

Figure 21 – Transient Response, 230 VAC, 50-100-50% Load Step. Upper: V_{OUT} 50 mV / div. Lower: I_{OUT} 0.4 A, 0.5 ms / div.

11.5 Output Ripple Measurements

11.5.1 Ripple Measurement Technique

A modified oscilloscope test probe was used to take output ripple measurements, in order to reduce the pickup of spurious signals. Using the probe adapter pictured in Figure 22, the output ripple was measured with a 1 μF electrolytic, and a 0.1 μF ceramic capacitor connected as shown.

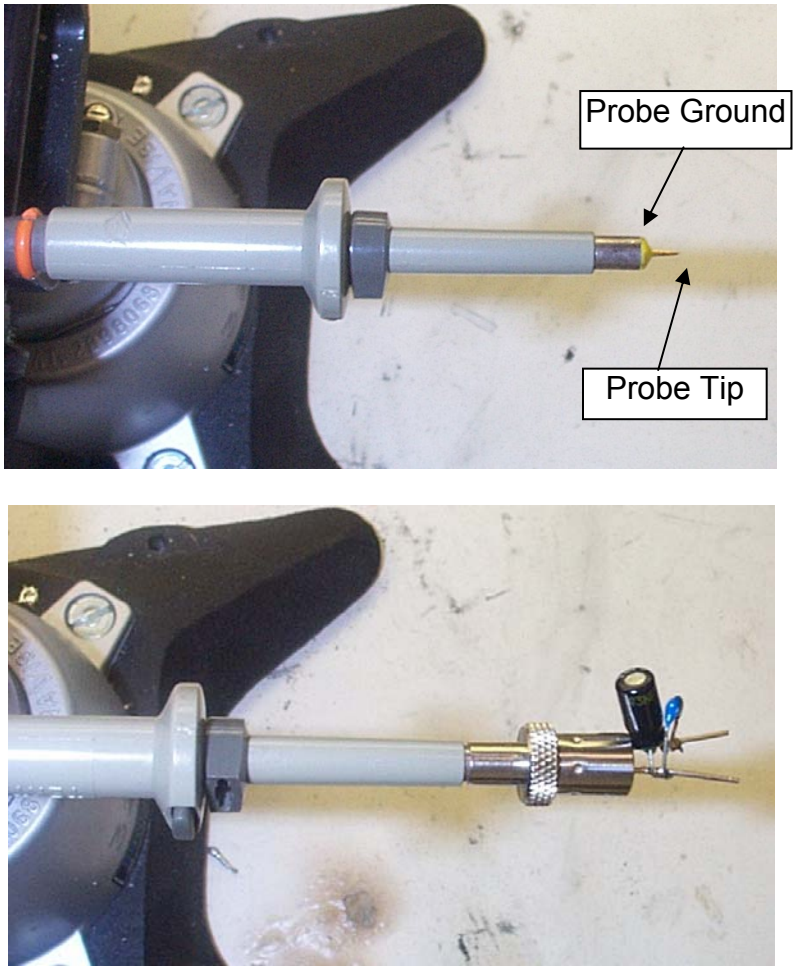

Figure 22 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter.
(Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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11.5.2 Measurement Results

The maximum voltage ripple at the output terminals of the power supply was measured as 58 mV.

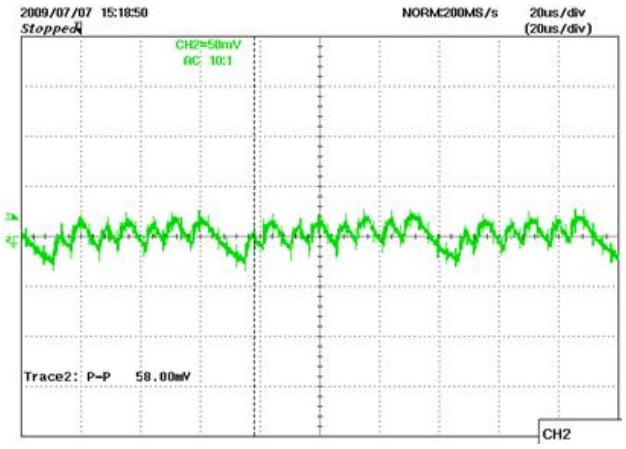


Figure 23 – Ripple, 85 VAC, Full Load.
20 μs, 50 mV / div.

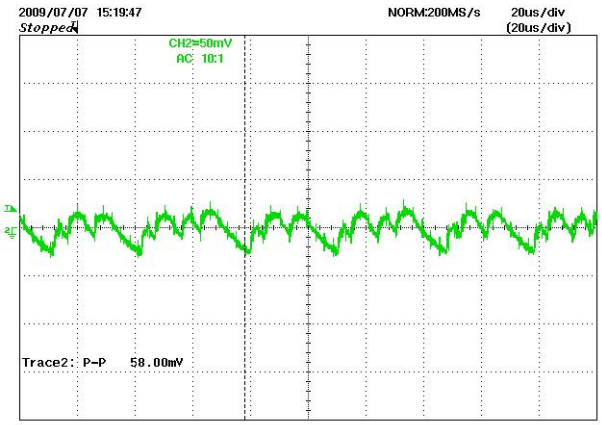


Figure 24 – Ripple, 115 VAC, Full Load.
20 μs, 50 mV / div.

12 Conducted EMI

Conducted emissions tests were performed at 115 VAC and 230 VAC at full load (12 V, 1.25 A). Measurements were taken with both Artificial Hand connection to output return and output return floating. In both cases a resistor load was used connected at the end of an output cable.

Composite EN55022B / CISPR22B conducted limits are shown. In all cases there was excellent (>10 dB) margin.

12.1 115 VAC, Full Load

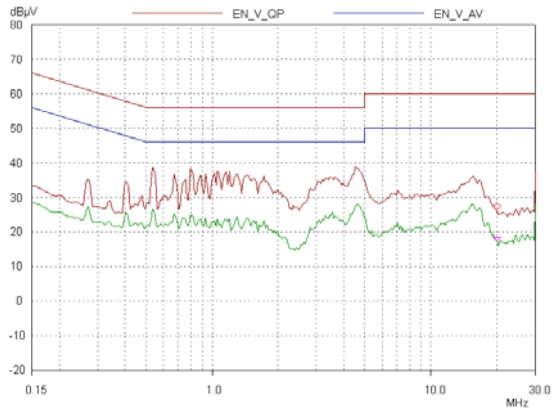
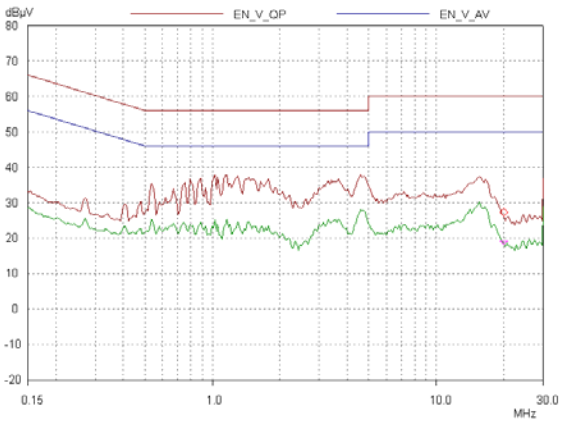
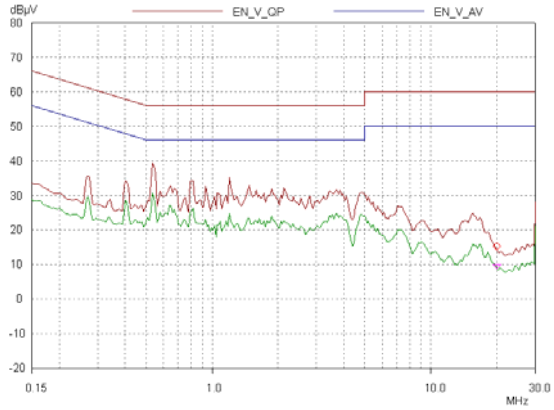
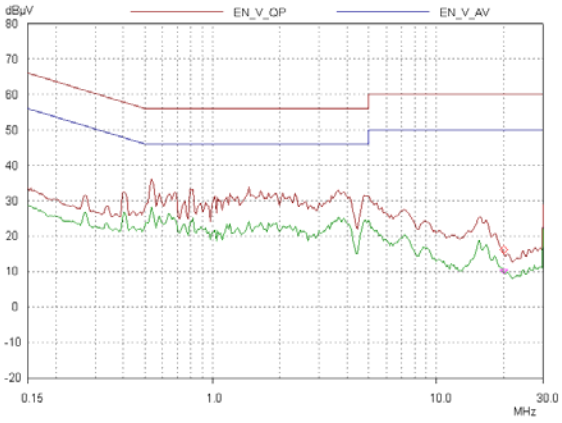
Line	Neutral
 Artificial Hand Connected to Output Return	 Artificial Hand Connected to Output Return
 Output Floating	 Output Floating

Figure 25– Conducted EMI at 115 VAC.

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12.2 230 VAC, Full Load

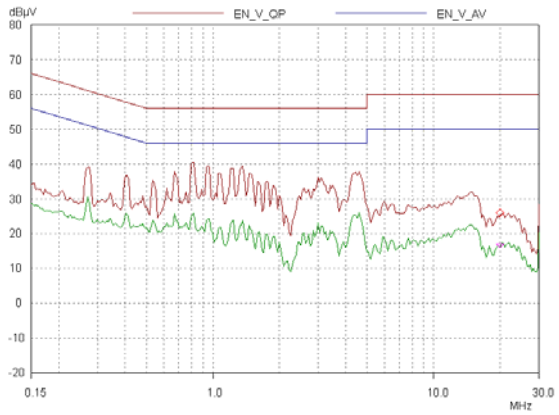
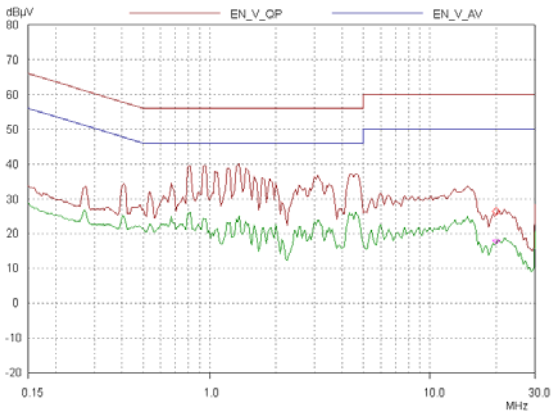
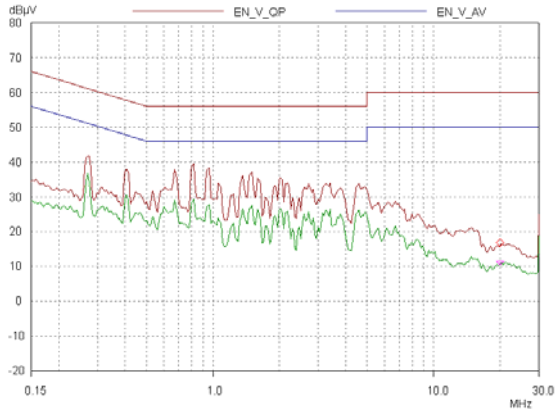
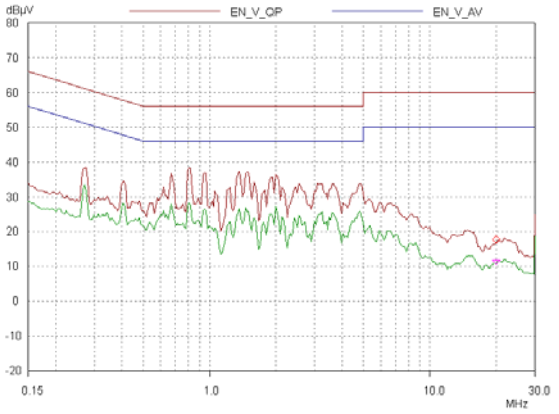
Line	Neutral
 Artificial Hand Connected to Output Return	 Artificial Hand Connected to Output Return
 Output Floating	 Output Floating

Figure 26 – Conducted EMI at 230 VAC.

13 Revision History

Date	Author	Revision	Description & Changes	Reviewed
23-Jul-09	PL	1.0	Initial Release	Apps
19-Nov-09	KM	1.1	Updated Figure 8a, 8b	Mktg

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