



**PRELIMINARY**

**CY62128**

# 128K x 8 Static RAM

## Features

- 4.5V – 5.5V operation
- CMOS for optimum speed/power
- Low active power (70 ns, LL version)
  - 330 mW (max.) (60 mA)
- Low standby power (70 ns, LL version)
  - 110 μW (max.) (20 μA)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  options

## Functional Description

The CY62128 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}_1$ ), an active HIGH chip enable ( $CE_2$ ), an active LOW output enable ( $\overline{OE}$ ), and three-state drivers. This device has an automatic power-down

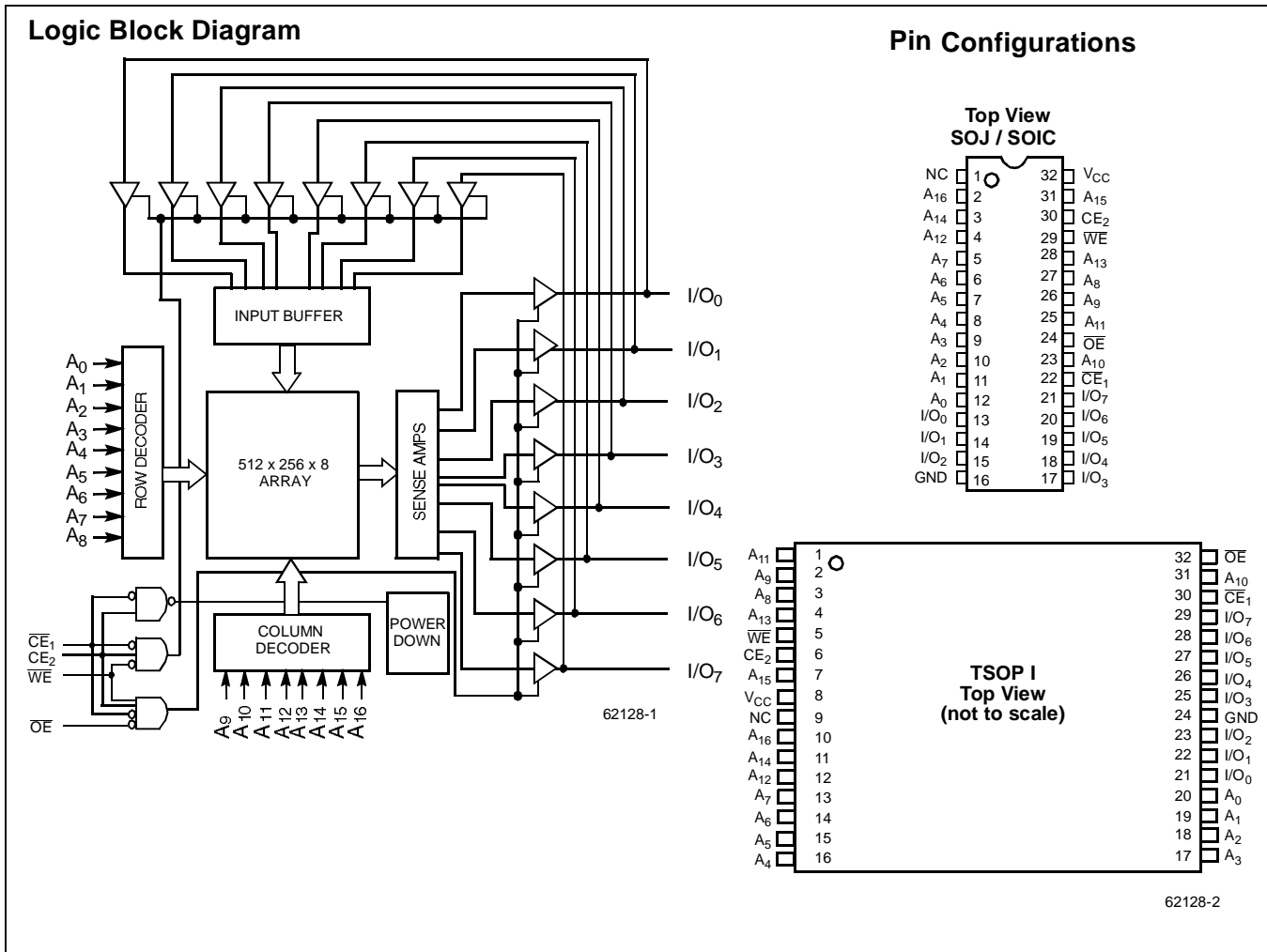
feature that reduces power consumption by more than 75% when deselected.

Writing to the device is accomplished by taking chip enable one ( $\overline{CE}_1$ ) and write enable ( $\overline{WE}$ ) inputs LOW and chip enable two ( $CE_2$ ) input HIGH. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking chip enable one ( $\overline{CE}_1$ ) and output enable ( $\overline{OE}$ ) LOW while forcing write enable ( $\overline{WE}$ ) and chip enable two ( $CE_2$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

The CY62128 is available in a standard 400-mil-wide SOJ, 525-mil wide (450-mil-wide body width) SOIC and 32-pin TSOP type I.



**Selection Guide**

		CY62128-55	CY62128-70
Maximum Access Time (ns)		55	70
Maximum Operating Current	Commercial	115 mA	110 mA
	L	70 mA	60 mA
	LL	70 mA	60 mA
Maximum CMOS Standby Current	Commercial	10 mA	10 mA
	L	100 $\mu$ A	100 $\mu$ A
	LL	20 $\mu$ A	20 $\mu$ A

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> +0.5V

DC Input Voltage<sup>[1]</sup>..... -0.5V to V<sub>CC</sub> +0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	V <sub>CC</sub>
Commercial	0°C to +70°C	5V $\pm$ 10%

**Electrical Characteristics** Over the Operating Range<sup>[3]</sup>

Parameter	Description	Test Conditions	62128-55		62128-70		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = - 1.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 2.1mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> +0.3	2.2	V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input Load Current	GND $\leq$ V <sub>I</sub> $\leq$ V <sub>CC</sub>	-1	+1	-1	+1	$\mu$ A
I <sub>OZ</sub>	Output Leakage Current	GND $\leq$ V <sub>I</sub> $\leq$ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	$\mu$ A
I <sub>OS</sub>	Output Short Circuit Current <sup>[4]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com'l	115		110	mA
			L	70		60	mA
			LL	70		60	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ or CE <sub>2</sub> $\leq$ V <sub>IL</sub> , V <sub>IN</sub> $\geq$ V <sub>IH</sub> or V <sub>IN</sub> $\leq$ V <sub>IL</sub> , f = f <sub>MAX</sub>	Com'l	25		25	mA
			L	10		10	mA
			LL	2		2	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3V$ , or CE <sub>2</sub> $\leq$ 0.3V, V <sub>IN</sub> $\geq$ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> $\leq$ 0.3V, f=0	Com'l	10		10	mA
			L	100		100	$\mu$ A
			LL	20		20	$\mu$ A

Shaded areas contain advance information

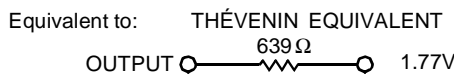
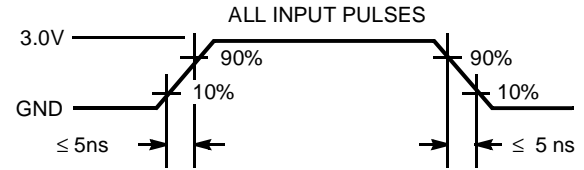
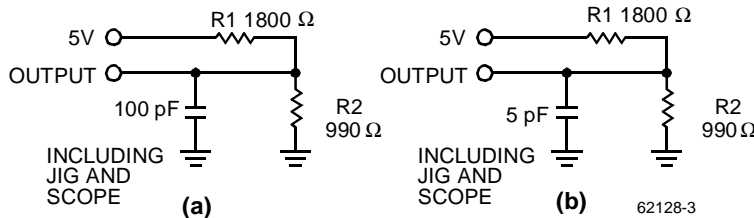
**Notes:**

- V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	9	pF
C <sub>OUT</sub>	Output Capacitance		9	pF

**AC Test Loads and Waveforms**



62128-3

62128-4

**Switching Characteristics<sup>[3,6]</sup> Over the Operating Range**

Parameter	Description	62128-55		62128-70		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	5		5		ns
t <sub>ACE</sub>	$\overline{\text{CE}}_1$ LOW to Data Valid, CE <sub>2</sub> HIGH to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to Data Valid		20		35	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to Low Z	0		0		ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to High Z <sup>[7, 8]</sup>		20		25	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}_1$ LOW to Low Z, CE <sub>2</sub> HIGH to Low Z <sup>[8]</sup>	5		5		ns
t <sub>HZCE</sub>	$\overline{\text{CE}}_1$ HIGH to High Z, CE <sub>2</sub> LOW to High Z <sup>[7, 8]</sup>		20		25	ns
t <sub>PU</sub>	$\overline{\text{CE}}_1$ LOW to Power-Up, CE <sub>2</sub> HIGH to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{\text{CE}}_1$ HIGH to Power-Down, CE <sub>2</sub> LOW to Power-Down		55		70	ns
<b>WRITE CYCLE<sup>[9]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{\text{CE}}_1$ LOW to Write End, CE <sub>2</sub> HIGH to Write End	45		60		ns
t <sub>AW</sub>	Address Set-Up to Write End	45		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	45		50		ns
t <sub>SD</sub>	Data Set-Up to Write End	45		55		ns

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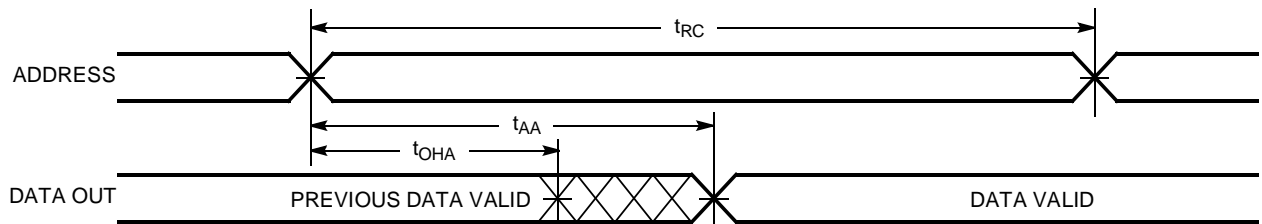
**Notes:**

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition time of 5ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 100pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}_1$  LOW, CE<sub>2</sub> HIGH, and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}_1$  and  $\overline{\text{WE}}$  must be LOW and CE<sub>2</sub> HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

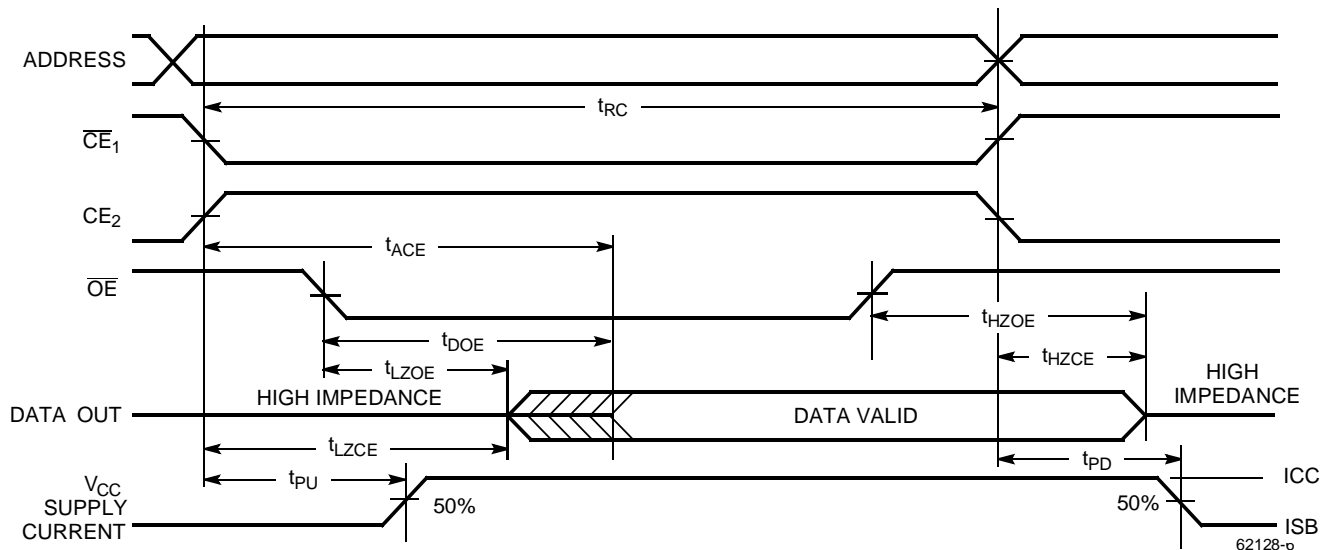
**Switching Characteristics**<sup>[3,6]</sup> Over the Operating Range (continued)

Parameter	Description	62128-55		62128-70		Unit
		Min.	Max.	Min.	Max.	
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[8]</sup>	5		5		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[7,8]</sup>		20		25	ns

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**Switching Waveforms**
**Read Cycle No.1**<sup>[10,11]</sup>


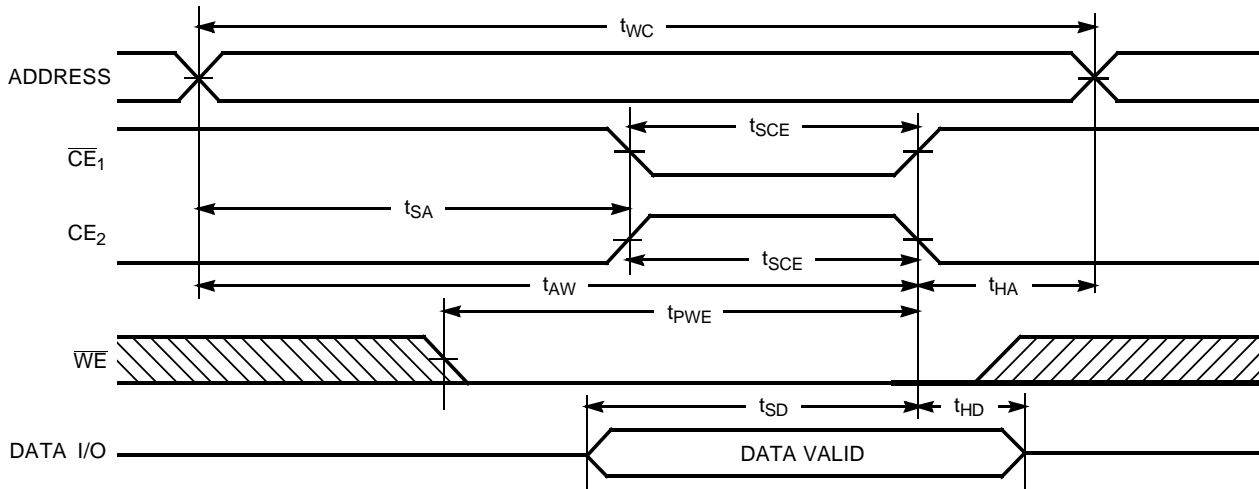
62128-5

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)**<sup>[11,12]</sup>


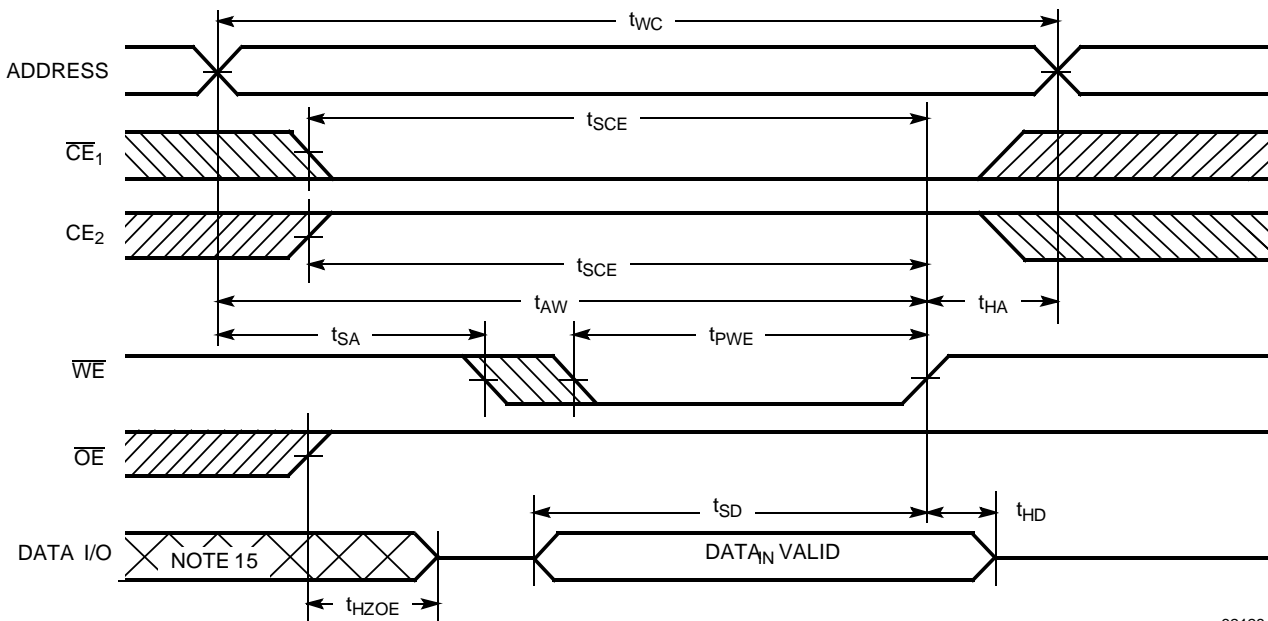
62128-o

**Notes:**

10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{CE}_1$  or  $CE_2$  Controlled)<sup>[13,14]</sup>**


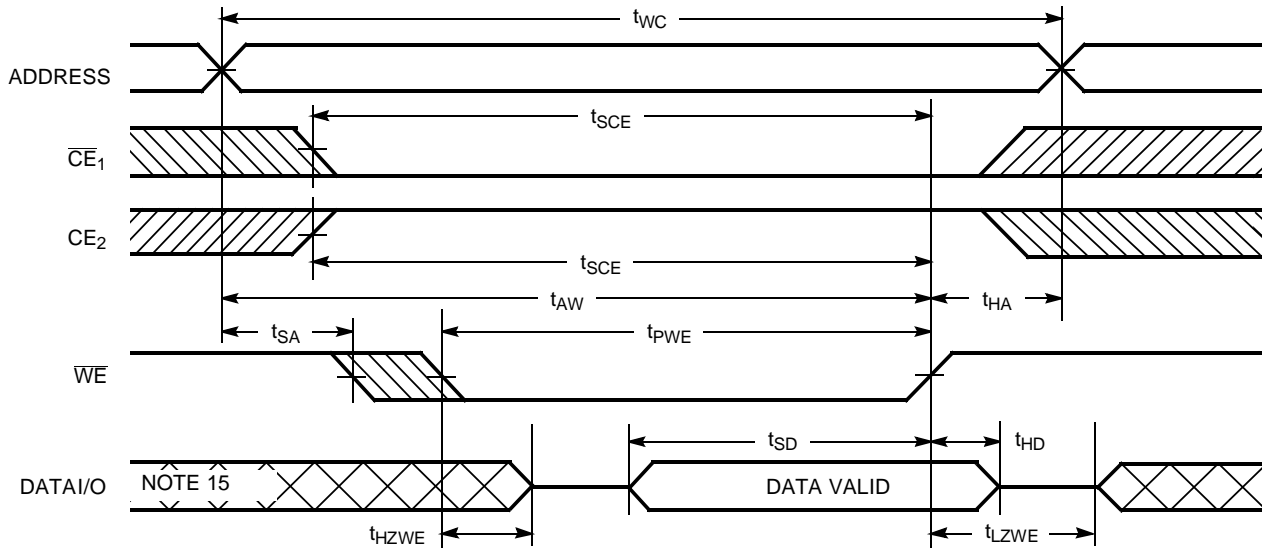
62128-7

**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[13,14]</sup>**


62128-8

**Notes:**

13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
14. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
15. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No.3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[13,14]</sup>**


62128-9

**Truth Table**

CE <sub>1</sub>	CE <sub>2</sub>	OE	WE	I/O <sub>0</sub> - I/O <sub>7</sub>	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I <sub>SB</sub> )
X	L	X	X	High Z	Power-Down	Standby (I <sub>SB</sub> )
L	H	L	H	Data Out	Read	Active (I <sub>CC</sub> )
L	H	X	L	Data In	Write	Active (I <sub>CC</sub> )
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

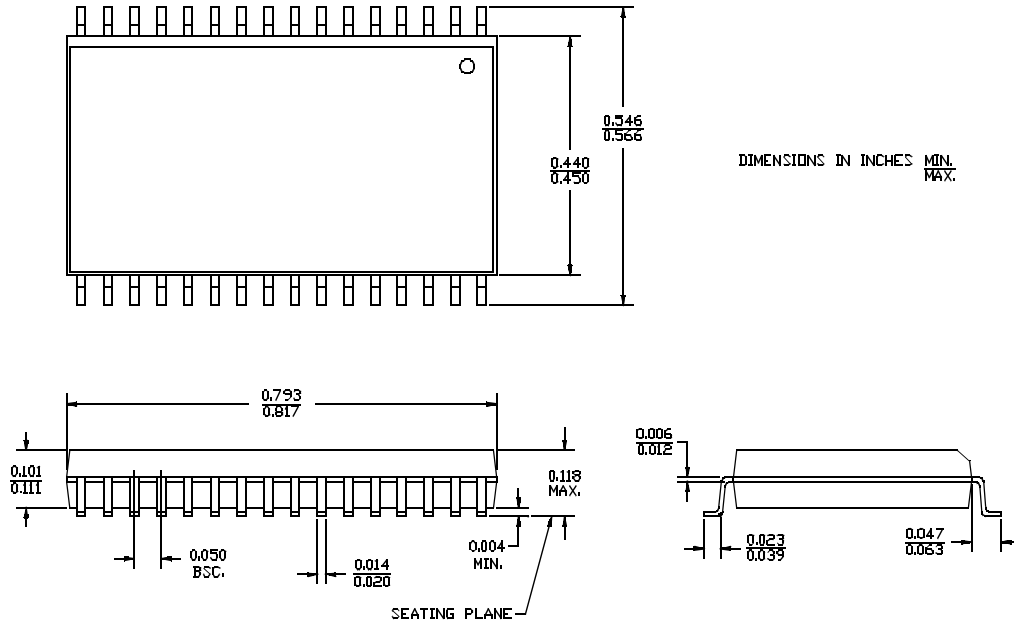
**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62128-55VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
	CY62128-55SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62128-55ZC	Z32	32-Lead TSOP Type I	
70	CY62128-70VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
	CY62128-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62128-70ZC	Z32	32-Lead TSOP Type I	
	CY62128L-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62128L-70ZC	Z32	32-Lead TSOP Type I	
	CY62128LL-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62128LL-70ZC	Z32	32-Lead TSOP Type I	

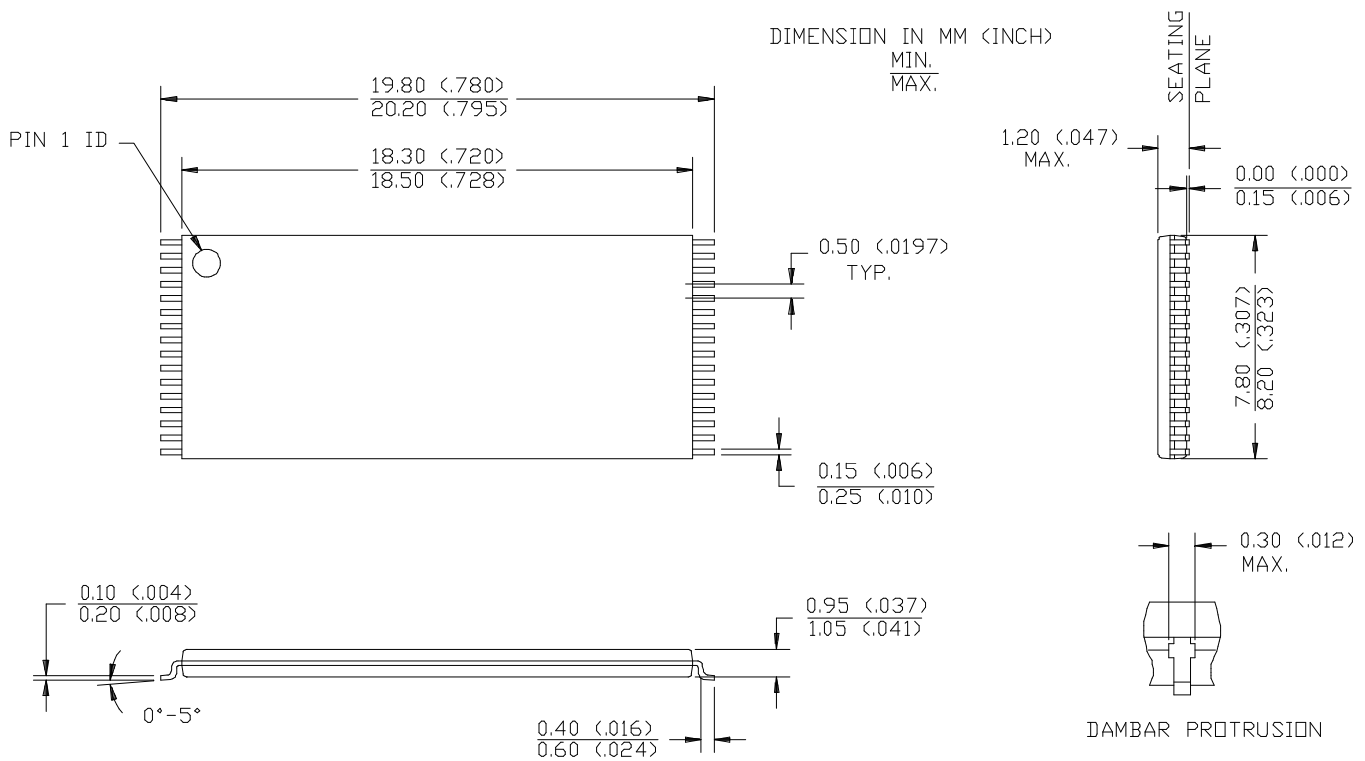
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**Package Diagrams**

**32-Lead (450 Mil) Molded SOIC S34**



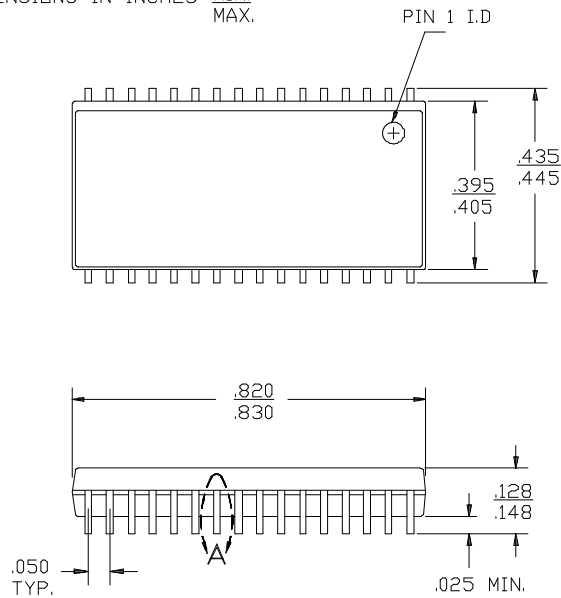
**32-Lead Thin Small Outline Package Z32**



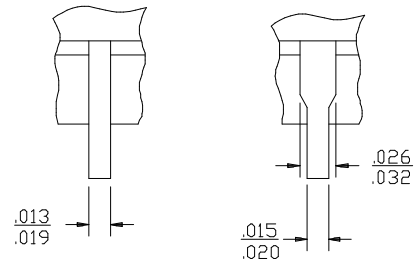
Package Diagrams (continued)

**32-Lead (400-Mil) Molded SOJ V33**

DIMENSIONS IN INCHES MIN. MAX.



DETAIL A  
EXTERNAL LEAD DESIGN



OPTION 1

OPTION 2

