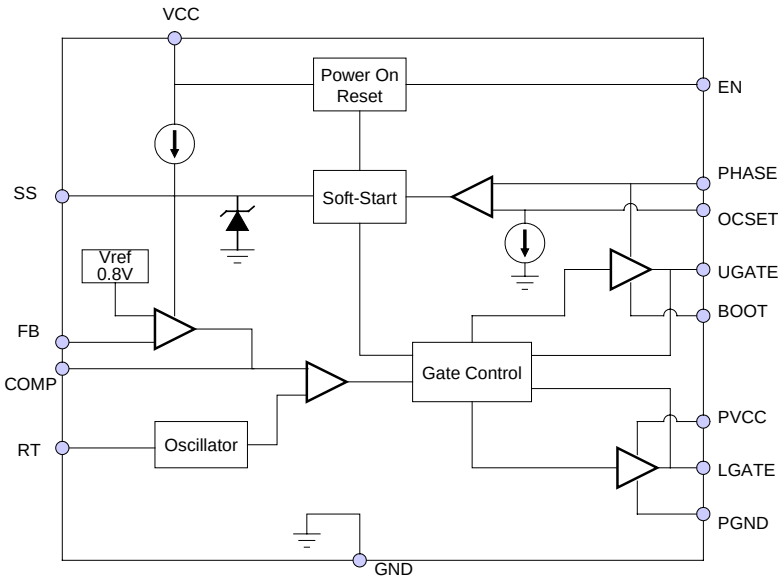
晶瀚科技
Chip Advanced Tech

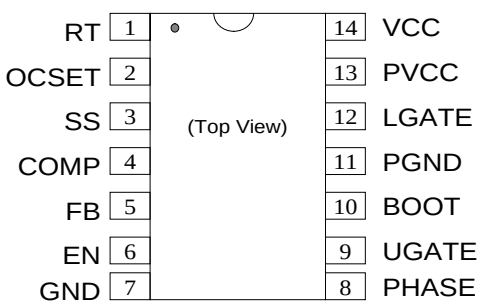
CAT7522
Synchronous and Rectified Buck PWM Controller

ABSTRACT:
The CAT7522 is designed to drive 2 N-channel MOSFETs with synchronous and rectified buck output. It integrates output adjustment, monitoring and over-current protection, all together to function a simple and complete control over DC-to-DC power management.

FEATURES:
- **12V Power Supply (VCC)**
- **+5V or +12V Input Voltage Range (VIN)**
- **Output Regulation 0.8V, lowest output voltage ±1% tolerance**
- **Wide Oscillation Range**
  Free run around 220KHz
  50K to 1MHz for adjustment
- **Fast transient response**
  Full Duty ratio, 0 – 100%
- **Over Current Fault monitoring**
  Use Upper MOSFET to enhance efficiency and cost benefit
- **14-Lead SOIC Package**

BLOCK DIAGRAM


APPLICATIONS:
- **Graphic Cards**
- **DDR memory power supply**
- **Data communication**
- **5V to 3.xV DC-to-DC**

PIN CONFIGURATION:


ORDERING INFORMATION:

Part Number	Package	Operating Temp(℃)
CAT7522	14L SOIC (Normal)	0-70
CAT7522G	14L SOIC (Pb free)	0-70

SPECIFICATIONS

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
V_{CC} Supply Current						
Nominal Supply	I_{CC}	EN=Vcc;UGATE & LGATE open		5		mA
Shutdown Supply		EN=0 V		50	100	μA
Power On Reset						
Rising Vcc Threshold		V_{OCSET}=4.5V			10.4	V
Falling Vcc Threshold		V_{OCSET}=4.5V	8.8			V
Enable-Input Threshold		V_{OCSET}=4.5V	0.8		2.0	V
Rising V_{OCSET} Threshold				1.27		V
Oscillator						
Free running frequency		RT=open ;Vcc=12 V	170	220	260	kHz
Ramp Amplitude	ΔV_{OSC}	RT=open		1.9		Vp-p
Reference Voltage Tolerance	V_{REF}		-1		+1	%
Reference Voltage				0.8		V
ERROR Amplifier						
DC Gain				90		dB
Gain-Bandwidth Product	GBW			15		MHz
Slew Rate	SR	COMP=10pF		6		V/μs
Gate Driver						
Upper Gate Source	I_{UGATE}	V_{BOOT}-V_{PHASE}=12V;V_{UGATE}=6V (Note 1)		450		mA
Upper Gate Sink	R_{UGATE}	I_{LGATE}=0.3A (Note 1)		5.5	10	Ω
Lower Gate Source	I_{LGATE}	Vcc=12V;V_{LGATE}=6V (Note 1)		690		mA
Lower Gate Sink	R_{LGATE}	I_{LGATE}=0.3A (Note 1)		3.5	6.5	Ω
Protection						
OCSET Current Source	I_{OCSET}	V_{OCSET}=4.5V	170	200	230	μA
Soft Start Current	I_{SS}			10		μA

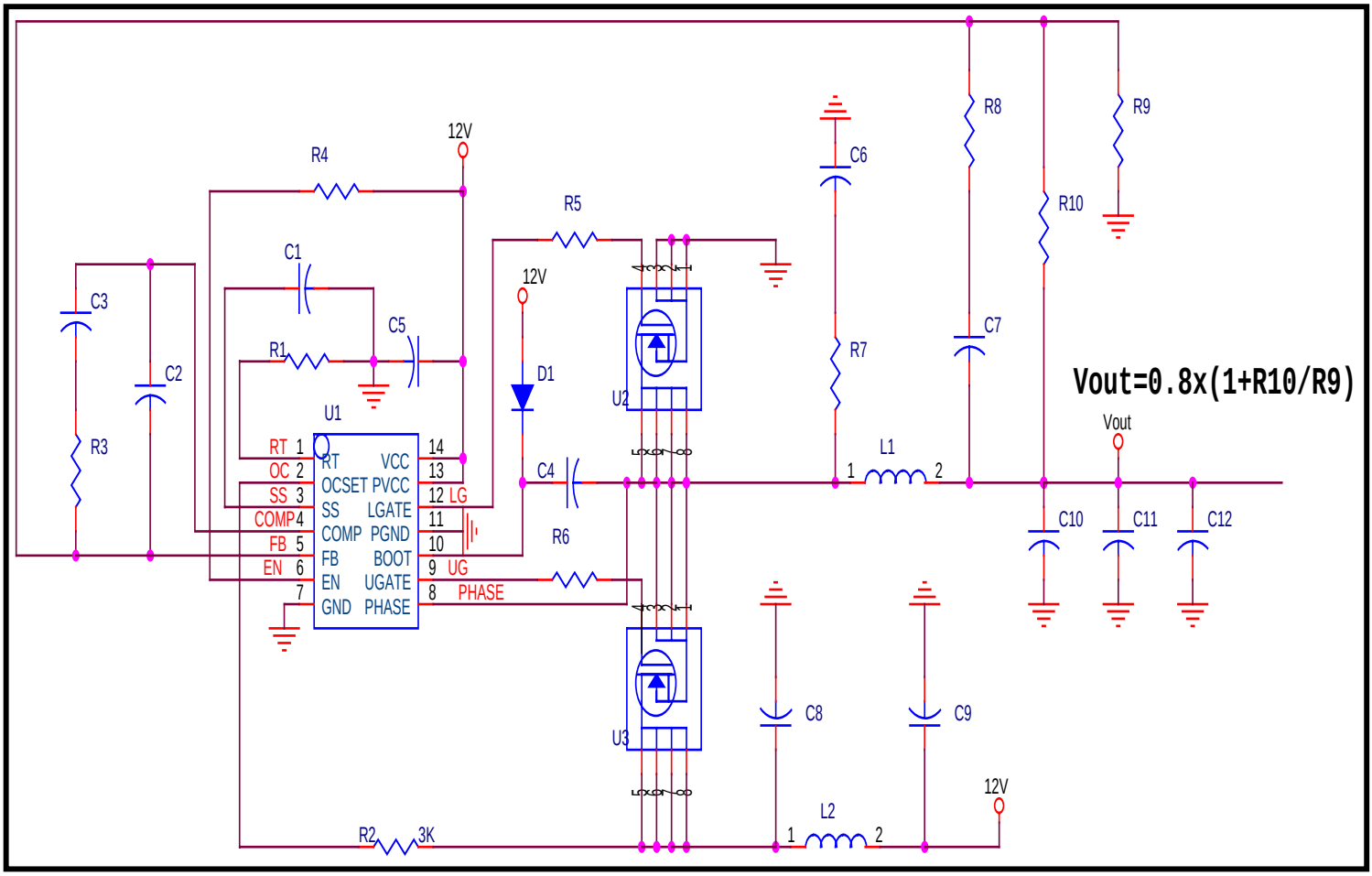
Note:
1. Guaranteed by design; not production tested.

ABSOLUTE RATING

Parameter	Max. Rating
Vcc, Supply Voltage	15V
Boot Voltage(V_{BOOT}-V_{PHASE})	15V
Input & Output Voltage	Vcc + 0.3V GND - 0.3V
Operating Temperature	0℃ to 70℃
Storage Temperature	-65℃ to 150℃
Max. Junction Temperature	150℃
ESD Classification	Class 2

CAT7522

TYPICAL APPLICATION



[Note]:

1. C1~C5 & C6~C10 are flexible in using considering cost and system performance, the above 5 devices and 6 devices are designed for internal characteristics testing use.
2. The recommended applications shall be customer design-in orientation to fit each customers demand. Based on the nature of customers demand-oriented, please contact CAT or agent for design support service.

PIN DESCRIPTION

RT
This pin allows oscillator switching frequency to be adjusted by the resistor value (R_t), from this pin to GND. The nominal 220 kHz switching frequency is increased according to the following equation:

$$Fs\ (kHz) \sim= 10^6 / R_t + 220\ kHz$$

The following table lists some resistors for R_t in common use and their approximately corresponding switching frequency:

Fs(K Hz)	220	300	400	500	600	700	800	900	1000
Rt (K ohm)	NC	22	6.8	4.1	2.9	2.2	1.7	1.5	1.28

OCSET
A resister, R_{OCSET}, from this pin to the drain of upper MOSFET (On resistance $r_{DS(ON)}$), and internal current source I_{OCS} to determine the converter over-current (OC) trip point by the following equation,

$$I_{PEAK} = I_{OCS} * R_{OCSET}/r_{DS(ON)}$$

Over-current (OC) trip cycles the soft-start function.

SS
Connect a capacitor from this pin to GND, and the capacitor along with and internal 10 μ A current source sets the soft start interval of the converter.

COMP and FB
COMP is the error amplifier output. FB is the interval input of error amplifier. These 2 pins are used to compensate the voltage-control feedback loop of the converter.

EN
EN means open-collector enable pin, pulling under 1V to disable the converter. In shut-down mode, the soft-start pin is discharged and the UGATE and LGATE pins are held low.

UGATE
Connect UGATE to the upper MOSFET gate. This pin provides the gate drive for upper MOSFET. It is also monitored by the adaptive shoot through protection function to determine when upper MOSFET has turned off.

LGATE
Connect UGATE to the lower MOSFET gate. This pin provides the gate drive for lower MOSFET. It is also monitored by the adaptive shoot through protection function to determine when lower MOSFET has turned off.

PHASE
This pin is used to monitor the voltage drop across the MOSFET for over-current protection. This pin also provides the return path for the upper gate drive.

BOOT
This pin provides bias voltage to the upper MOSFET driver. A bootstrap circuit may used to generate BOOT voltage suitable to drive a standard N-channel MOSFET.

VCC
Provide 12V bias supply for the chip.

GND
Signal ground of the chip

PVCC
Supply voltage for lower gate drive

PGND
Power ground pin, connected to lower MOSFET source to this pin.

FUNCTION DESCRIPTION

OUTPUT REGULATION

The output voltage level setting is

VOUT = 0.8V * (1 + R10 / R9)

Please reference the application diagram.

SOFT-START

In CAT7522, an internal 10uA current source charges an external capacitor (Css) on the SS pin to 4V. Soft-start clamps the error amplifier output (COMP pin) to the SS pin voltage. Figure 1 shows the soft-start interval. The formula to calculate the interval is:

$t1 = Css / Iss * Vosc$ (min)

$t_{soft\_start} = t2 - t1 = Css / Iss * Vout / Vin * \triangle Vosc$

where: Css : Soft start capacitor.
Iss : 10uA, soft start current.
Vosc(min) = 1.35V, bottom of oscillator.
△ Vosc = 1.9V, peak to peak oscillator amplitude.

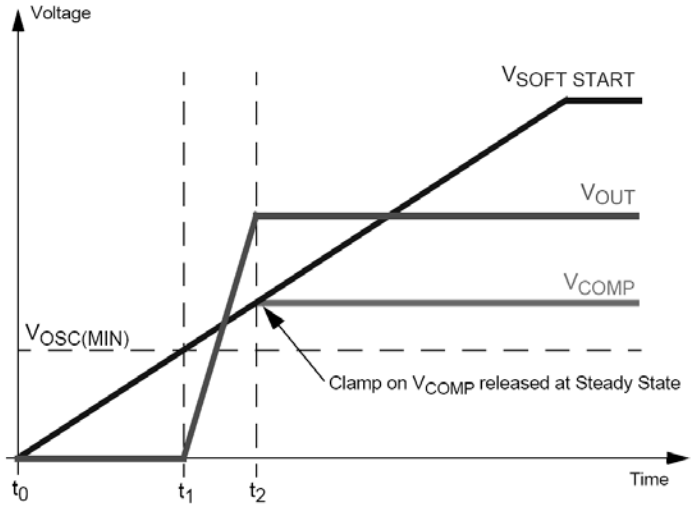


Figure 1

OVERCURRENT PROTECTION

The overcurrent function protects the converter from a shorted output by using the upper MOSs on-resistance, $r_{DS(ON)}$ to monitor the current.

The overcurrent function cycles the soft-start function in a hiccup mode to provide fault protection. A resistor (R_{OCSET}) programs the overcurrent trip level. An internal 200uA (typical) current sink develops a voltage across R_{OCSET} that is reference to Vin. When the voltage across the upper MOSFET (also referenced to VIN) exceeds the voltage across R_{OCSET}, the overcurrent function initiates a soft-start sequence.

The peak inductor current (I_{peak}) is determined by the following equation:

$I_{peak} = 200uA * R_{ocset} / r_{DS(on)}$

A small ceramic capacitor should be placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input voltage.

FEEDBACK COMPENSATION

The compensation required for VOUT1 and VOUT2 is similar to many other switching regulators. The figure 2 shows type-3 compensation, but the simpler type 2 is also possible, under the right conditions. A simple rule of thumb of type-3 compensation is that when buck capacitors are used on the outputs, the effective ESR is about smaller than 3 mohm. Notes that the component labels match the equations given in this section, but may not match other diagrams in this datasheet.

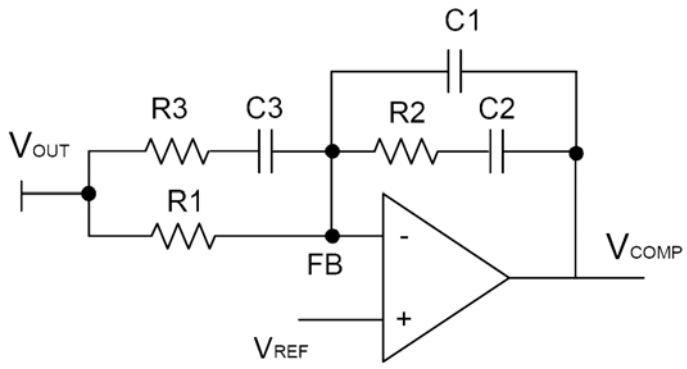


Figure 2

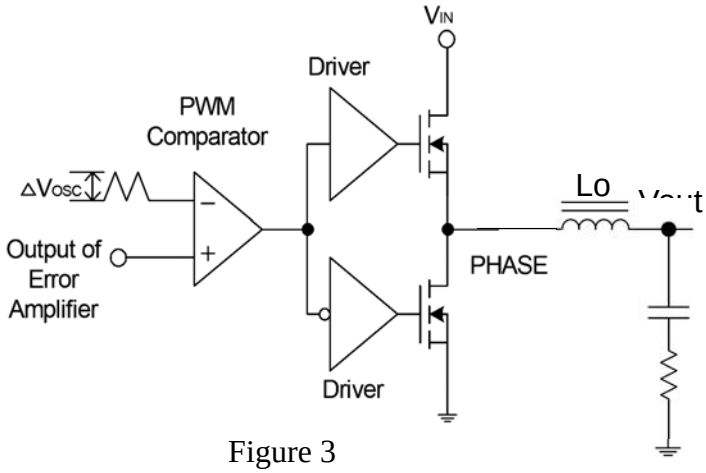


Figure 3

In Figure 2 and 3, the output voltage (Vout) is regulated to the Reference voltage level. The error amplifier output (VCOMP) is compared with the oscillator (OSC) triangular wave to provide a

pulse-width modulated (PWM) wave with an amplitude of VIN at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

The closed loop transfer function of the converter includes two part, the error amplifier compensation and the modulator transfer functions. The modulator transfer function is dominated by a DC gain and the output filter, with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (VIN) divided by the peak-to-peak oscillator voltage $\triangle V_{OSC}$.

$$F_{LC} = \frac{1}{2\pi \bullet \sqrt{L_O \bullet C_O}} \qquad F_{ESR} = \frac{1}{2\pi \bullet (ESR \bullet C_O)}$$

The poles and zeros location of the type-3 compensation of error amplifier list below.

$$F_{Z1} = \frac{1}{2\pi \bullet R2 \bullet C2} \qquad F_{P1} = \frac{1}{2\pi \bullet R2 \bullet \left(\frac{C1 \bullet C2}{C1 + C2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \bullet (R1 + R3) \bullet C3} \qquad F_{P2} = \frac{1}{2\pi \bullet R3 \bullet C3}$$

The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (fco) and adequate phase margin. The following guidelines will help users to design the compensation network.

(1). Select the desired zero crossover frequency F_{CO}. F_{CO} is usually 1/4 ~ 1/10 switch frequency (F_S).
(2). Choose a value for R1.
(3). Pick gain R2/R1 for desired F_{CO}. To simplify, the R2 can be calculated by

$V_{in} / \triangle V_{OSC} * F_{LC}/F_{CO} * R2/R1 = 1$

(4). Place F_{Z1} about 0.75 * F_{LC} to calculate the C2.
(5). Place F_{P1} at F_{ESR} to calculate the C1.
(6). Place F_{Z2} about F_{LC}.
(7). Place F_{P2} about 0.5 * F_s.

Combined (6), (7) the R3 and C3 will be calculated.

(8). Estimate the stability, Modify F_{CO} and R2/R1 gain then repeat if necessary.

The Figure 4 shows an asymptotic plot of the converter's gain vs. frequency.

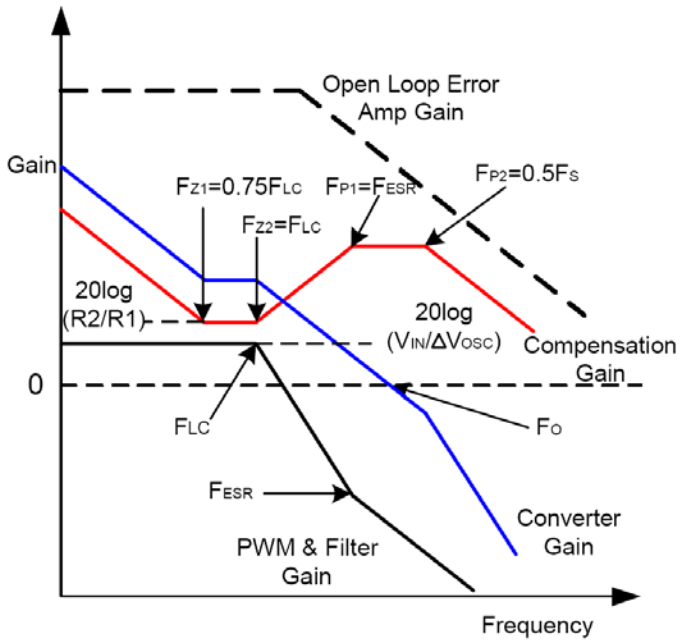


Figure 4

OUTPUT INDUCTOR SELECTION

The output inductor is selected to meet the output voltage ripple requirements and affects the load transient response. Higher inductance reduces the inductor's ripple current and induces lower output ripple voltage. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fs \times L} \bullet \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Although increase the inductance reduce the ripple current and voltage, but the large inductance reduces the regulator's response time to load transient. Increasing the switching frequency (Fs) for a given inductor also reduces the ripple current and voltage but it will increase the switching loss of the power MOS.

To select the inductor value, a guideline is to choose the ripple current ($\triangle$I) to be approximately 10%~50% of the maximum output current. Once the inductor value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. It is also important to have the inductance tolerance specified to keep the accuracy of the system controlled. Using 20% for the inductance (at room temperature) are reasonable tolerances that most manufacturers can meet. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

OUTPUT CAPACITORS SELECTION

An output capacitor is required to filter the output and supply the load transient current. Higher Capacitor value and lower ESR reduce the output ripple and the load transient drop. These requirements are met with a mix of capacitors and careful layout.

In typical switching regulator design, the ESR of the output capacitor bank dominates the transient response. The number of output capacitors can be determined by using the following equations:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

$\triangle V_{ESR}$ = change in output voltage due to ESR (assigned by the designer).
$\triangle I_{OUT}$ = load transient.
ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).
ESR_{MAX} = maximum allowable ESR.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Consult the capacitors manufacturer to make sure the decoupling requirements.

POWR MOS SELECTION

CAT7522 requires 2 N-channel power MOSs for each PWM output. These should be selected base on $R_{ds(on)}$, gate supply voltage, gate charge (capacitance) and thermal management requirements. In general, the upper power MOS should be chosen to minimize the gate charge, since switching loses dominate. Since the lower power MOS is on most of the time, low $R_{ds(on)}$ should be the main consideration.

It can be advantageous to use multiple power MOSs to reduce power consumption. By placing a number of MOSs in parallel, the effective $R_{ds(on)}$ is reduced, thus reducing the ohmic power loss. However, placing MOSs in parallel increases the gate capacitance so that switching losses increase. As long as adding another parallel MOS reduces the ohmic power loss more than the switching losses increase, there is some advantage to doing so.
The following equations can be used to calculate power dissipation in the power MOSs.

$$P_{UPPER} = I_O^2 \times r_{DS(ON)} \times D + \frac{1}{2} Io \times V_{IN} \times t_{SW} \times Fs$$

$$P_{LOWER} = I_O^2 \times r_{DS(ON)} \times (1 - D)$$

Where,
D is the duty cycle = Vout / Vin.
t_{SW} is the switching interval.
Fs is the switching frequency.

CONTACT:

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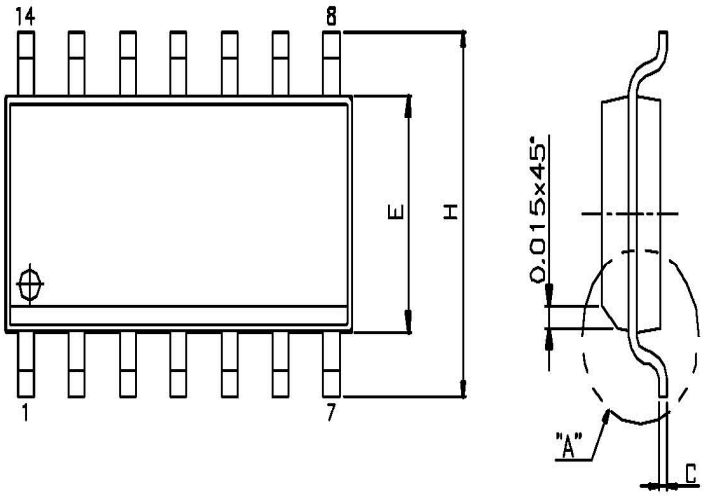
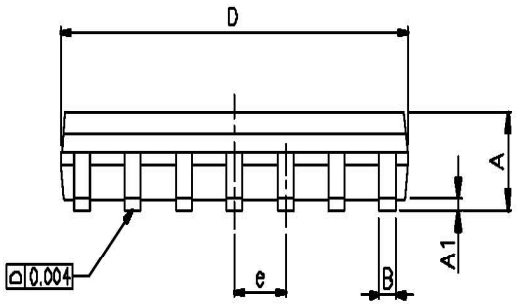
CAT7522

MECHINICAL DIMENSION



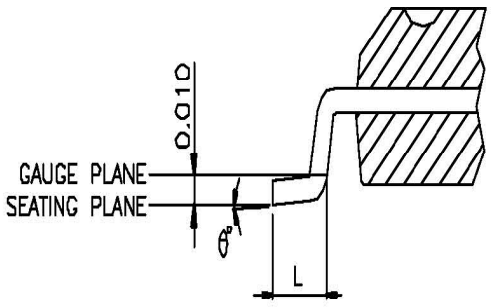
SYMBOLS	MIN.	NOM.	MAX.
A	0.058	0.064	0.068
A1	0.004	–	0.010
B	0.013	0.016	0.020
C	0.0075	0.008	0.0098
D	0.336	0.341	0.344
E	0.150	0.154	0.157
e	–	0.050	–
H	0.228	0.236	0.244
L	0.015	0.025	0.050
θ°	0°	–	8°

UNIT : INCH



NOTES:

1. JEDEC OUTLINE : MS-012 AB
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.



DETAIL : A