NEXSEM

NX2511

2-4 PHASE SELECTABLE VRD10.X CONTROLLER

PRELIMINARY DATA SHEET

Pb Free Product

DESCRIPTION

The NX2511 is a multiphase PWM controller with the ability to operate in 2,3 or 4 phase control operation. This device with external FET drivers such as NX3202 , NX3203 or NX3212 is designed to provide a high performance high current multiphase converter that meets the VRD10.0 specification.The NX2511 uses differential remote sensing using either current sense resistor or inductor DCR sensing to achieve accurate current matching between the three channels. Differential sensing eliminates the error caused by PCB board trace resistance that is otherwise present when using a single ended voltage sensing. In addition, the NX2511 offers complete VRD10 signal interface using 6 bit DAC with on the fly DAC change, Differential Output Voltage Sensing, accurate programmable droop allowing to reduce number of output capacitors, accurate enable circuit provides programmable start up point for Bus voltage, PGOOD output, programmable switching frequency and hiccup current limiting circuitry.

FEATURES

- VRM9/VRM10 compatible 6 bit VID
- 2 to 4 Phase selectable interleaved PWM stages.
- Differential current sensing allows accurate current share using Inductor ESR or current sense resistor
- Programmable output voltage droop & offset control
- Programmable UVLO for both BUS voltage and Driver Supply Voltage
- Differential Remote Voltage Sensing
- Over Voltage Protection (OVP)
- Hiccup Current current Limit (OCP)
- Power Good signal for Power Sequencing
- Internal Soft start operation
- Programmable switching frequency from 100kHz to 600kHz per phase
- Pb-free and RoHS compliant

APPLICATIONS

- Desktop mother board VRD10.X
- Low voltage high current applications

TYPICAL APPLICATION

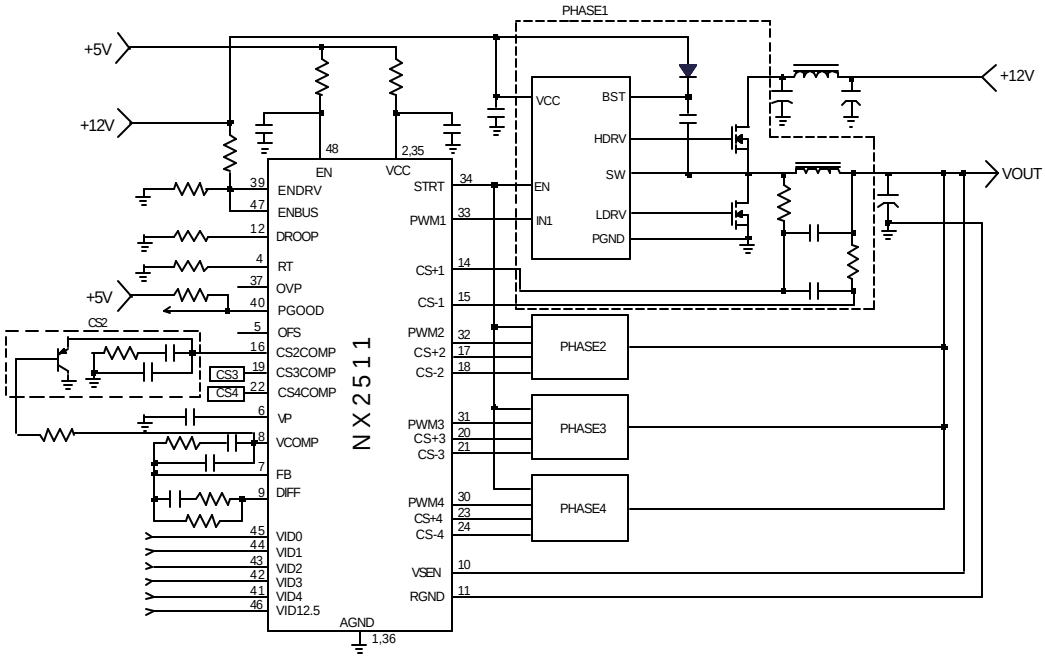


Figure1 - Typical application of 2511

ORDERING INFORMATION

Device	Temperature	Package	Pb-Free
NX2511CMTR	0 to 70°C	MLPQ-48 L	Yes

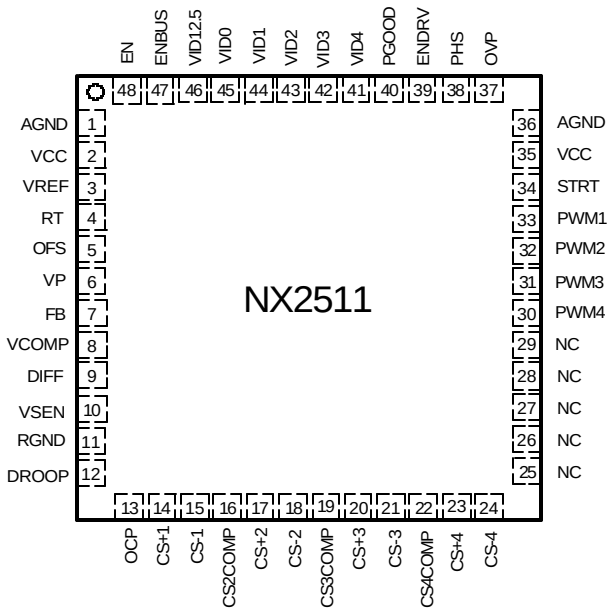
ABSOLUTE MAXIMUM RATINGS

Vcc to PGND & BST to SW voltage ..... -0.3V to 6.5V
All other pins ..... -0.3V to 6.5V
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature Range ..... -40°C to 125°C

CAUTION: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

48-LEAD PLASTIC MLPQ



$\theta_{JA} \approx 29^{o}C/W$

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc = 5V, EN=HIGH, and T_A= 0 to 70°C. Typical values refer to T_A = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
VID Voltage(VID4, VID3, VID2, VID1,VID0, VID12.5)						
DAC initial accuracy				0.5		%
DAC Voltage line regulation		Vcc=4.75 to 5.25V		0.1		%
VID Pull up Current			35	50	65	uA
VID Input Low Level					0.4	V
VID Input HI Level			0.8			V
Supply Voltage(Vcc)						
V_{CC} Voltage Range	V_{CC}		4.5	5	5.5	V
V_{CC} Supply Current	I_{CC}		-	5		mA

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Under Voltage, Vcc , Enable(EN) & ENBUS						
V_{CC}-Threshold	V_{CC}_UVLO	V_{CC} Rising		4		V
V_{CC}-Hysteresis	V_{CC}_Hyst			0.2		V
EN Threshold		EN Rising		0.6		V
EN Hysteresis				0.1		V
ENBUS Threshold		ENBUS Rising		1.6		V
ENBUS Hysteresis				0.16		V
Oscillator (Rt)						
Frequency	FS	Clock Freq.		600		KHz
Ramp-Amplitude Voltage	V_{RAMP}			1		V
Ramp Peak				2.5		V
Ramp Valley				1.5		V
Max Duty Cycle		F=600Khz		93		%
Min duty Cycle					0	%
OVP latched Drive Current				2		mA
OVP delay		Freq per phase=200kHz		160		uSec
Current Sense Transconductance Amplifiers						
Open Loop Gain			50	65		dB
Transconductance				1600		umoh
Input Offset Voltage	Vio			0		mV
Voltage Mode Error Amplifier						
Open Loop Gain			50			dB
Output Current Source or Sink				1		mA
Output HI Voltage			Vcc-1.5			V
Output LOW Voltage					0.5	V
Remote Sense Differential Amplifier (Vsen, Rgnd, Diff)						
Gain			0.995	1	1.005	V/V
Common Mode Range			-0.3		Vcc	V
Common Mode Rejection			50			dB
Output Current Source or Sink			5			mA
Output HI Voltage			Vcc-1.5			V
Output LOW Voltage					0.5	V
SS (Internal)						
Soft Start time	Tss	Fclock=600Khz 200Khz/Phase		6.4		mS
Delay before SS ramp up				320		uSec

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Power Good(Pgood) Threshold		V_{SEN} Falling		74		$\%V_{ID}$
Hysteresis				5		$\%V_{ID}$
PGood Voltage Low		I_{PGood}=-5mA		0.5		V
Current Sense Amplifier(CS+, CS-) Input Offset Voltage				0		mV
Voltage Gain			29.7	30	30.3	V/V
Pin Adjust Offset Voltage (OFS) Voltage at OFS Pin		Rofs connected to GND		1.25		V
		Rofs connected to Vcc(measured with respect to Vcc)		1.25		
OCP Adjust Blank time before activating OCP		8 Clock cycles of 200 kHz per phase		40		uS
Vref Reference Voltage				1.6		V

PIN DESCRIPTIONS

Pin #	Symbol	Pin Description
2,35	VCC	IC's supply voltage. This pin biases the internal logic circuits. An internal undervoltage lockout keeps IC off till VCC reach 4V.
34	STRT	This pin is used to enable external drivers like NX3202. It goes high when all Enable signal as well as internal UVLO is true.
48	EN	This pin is used to enable the IC when is pulled high. The pin has a threshold voltage of 0.6 volts.
33, 32, 31, 30	PWM1,PWM2, PWM3,PWM4	These pins provide the PWM signal to the external drivers for phase 1, phase 2, phase 3, and phase 4 respectively.
38	PHS_SEL	The pin selects the number of phases the converter will operatate. Connect to GND for 4 phase, leave open for 3 phase or connect to 5V for 2 phase operation.
40	PGOOD	This pin is an open drain output. If used, it should be pulled to 5v with a resistor greater than or equal to 10k, otherwise it my be left open. When soft start ends, the PGOOD pin switches high. Any fault or under voltage on the enable pins will cause the signal to be pulled low.
6	VP	Input to the positive pin of the error amplifier. A resistor is connected from the output of the DAC to this pin. Place a small capacitor from this pin to GND to filter any noise as well as to provide a smooth transition during on the fly transistion.
7	FB	This pin is the error amplifier inverting input. It is connected via a resistor to the output of the differential sense amplifier.
4	RT	This pin programs the internal oscillator frequency using a resistor from this pin to ground. The frequency of each phase is 1/N of this frequency. When N is selected number of phases.
37	OVP	This pin indicates an over voltage fault has occurred. This pin switches high when the Diff pin is greater than 200mV above the Vp pin. It can drive a SCR to turn off the converter.
14, 17 20, 23	CS+1,CS+2, CS+3,CS+4	Positive input of the differential current sense amplifiers. It is connected directly to the RC junction of the respective phase's output inductor.
15, 18 21, 24	CS-1,CS-2, CS-3,CS-4	Negative input of the differential current sense amplifiers. It is connected directly to the negative side of the respective phase's output inductor.
16, 19, 22	CS2COMP, CS3COMP, CS4COMP	The output of the transconductance op amp for current sharing circuit. An external RC is connected from these pins to GND to stabilize the current loop.
8	Vcomp	This is the output pin of the error amplifier. The compensation network is attached between this pin, the Fb pin and the Diff pins.
5	OFS	A resistor from this pin to ground or Vcc provides a positive or negative offset respectively. This is accomplished using two different internal current sources.

Pin #	Symbol	Pin Description
10, 11,9	VSEN, RGND,DIFF	These pins are the input and output to a differential amplifier and are used to remotely sense the output voltage. Vsen is the positive input, Rgnd is the negative input, and Diff is the output voltage to the differential amplifier.
13	OCP	A resistor divider connected from this pin to Vref programs the current limit threshold. The outputs of the internal current sense differential amplifiers are summed together to represent the output current. This voltage is then compared to this threshold and resets the soft start after 64 clock cycles.
3	VREF	A 1.6V buffered reference is brought out.
47	ENBUS	This pin is used to program the under voltage lockout of the bus supply. A resistor divider from the bus voltage to this pin programs the under voltage lockout. When the voltage of this pin is greater than 1.6V, the bus voltage is assumed operation.This pin has a 10% hysterisis.
39	ENDRV	This pin is used to program the under voltage lockout of the gate driver supply. A resistor divider from the gate driver voltage to this pin programs the under voltage lockout. When the voltage of this pin is greater than 1.6V, the gate driver voltage is assumed operation.This pin has a 10% hysterisis.
46 45, 44, 43, 42, 41	VID12.5, VID0, VID1, VID2, VID3, VID4	These are the inputs to the internal DAC that provides the reference voltage for the regulated output. They can be connected directly to the open drain signal output or pulled up externally up to Vcc. These pins have 40uA internal pull up current source that goes to zero as the voltage rises above the logic threshold.
11	DROOP	A resistor from this pin to ground programs an internal current source that is fed into the FB pin. This current source is proportional to the output current of the regulator. The product of this current times the external resistor RFB provides a droop voltage.