5V/12V Synchronous-Rectified Buck Controller with Enable Input

General Description

The uP6109 is a compact synchronous-rectified buck controller specifically designed to operate from 5V or 12 supply voltage and to deliver high quality output voltage as low as 0.8V. This (P)SOP-8 device operates at fixed 300 kHz frequency and provides an optimal level of integration to reduce size and cost of the power supply.

This controller integrates internal MOSFET drivers that support 12V+12V bootstrapped voltage for high efficiency power conversion. The bootstrap diode is built-in to simplify the circuit design and minimize external part count.

Other features include internal softstart, undervoltage protection, overcurrent protection and shutdown function. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part is available in (P)SOP-8 packages.

Ordering Information

Order Number	Package Type	Remark
uP6109ASA8	SOP-8	
uP6109ASU8	PSOP-8	

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 and RoHS requirements. They are 100% matte tin (Sn) plating and suitable for use in SnPb or Pb-free soldering processes.

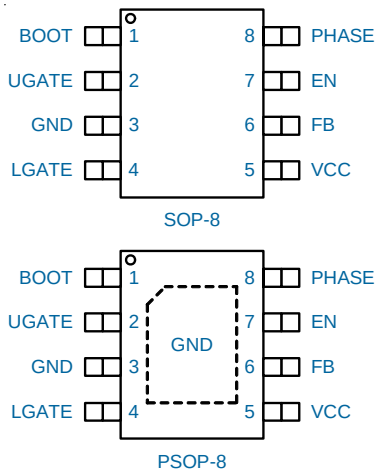
Features

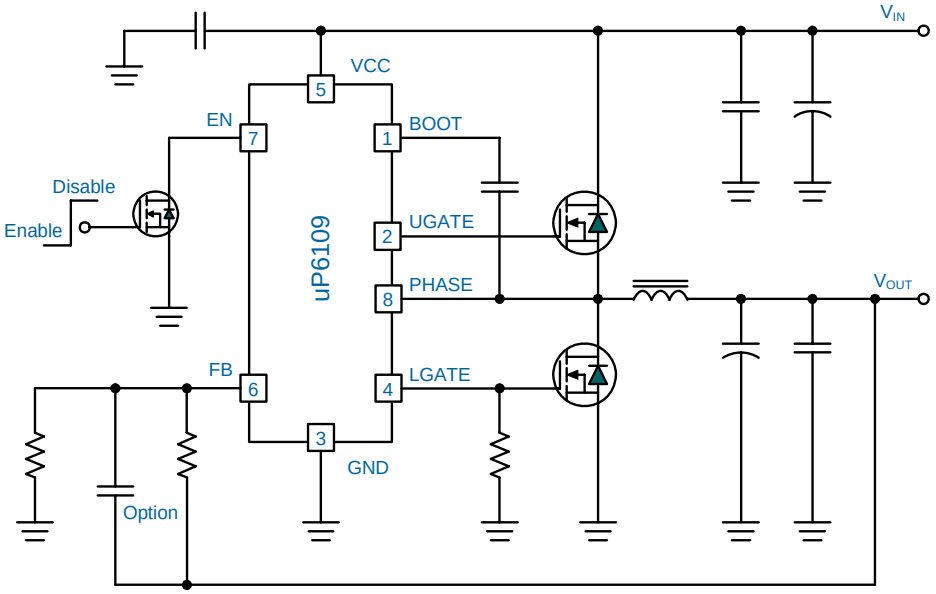
- Operate from 5V or 12V Supply Voltage
  - 3.3V to 12V V_{IN} Input Range
  - 0.8 V_{REF} with 1.5% Accuracy
  - Output Range from V_{REF} to 80% of V_{IN}
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
  - Fast Transient Response
- High-Bandwidth Error Amplifier
  - 0% to 80% Duty Cycle
- Lossless, Programmable Overcurrent Protection
  - Uses Lower MOSFET $R_{DS(ON)}$
- 300 kHz Fixed Frequency Oscillator
- Internal Soft Start
- Integrated Bootstrap Diode

Applications

- Power Supplies for Microprocessors or Subsystem Power Supplies
- Cable Modems, Set Top Boxes, and xDSL Modems
- Industrial Power Supplies; General Purpose Supplies
- 5V or 12V Input DC-DC Regulators
- Low Voltage Distributed Power Supplies

Pin Configuration & Typical Application Circuit

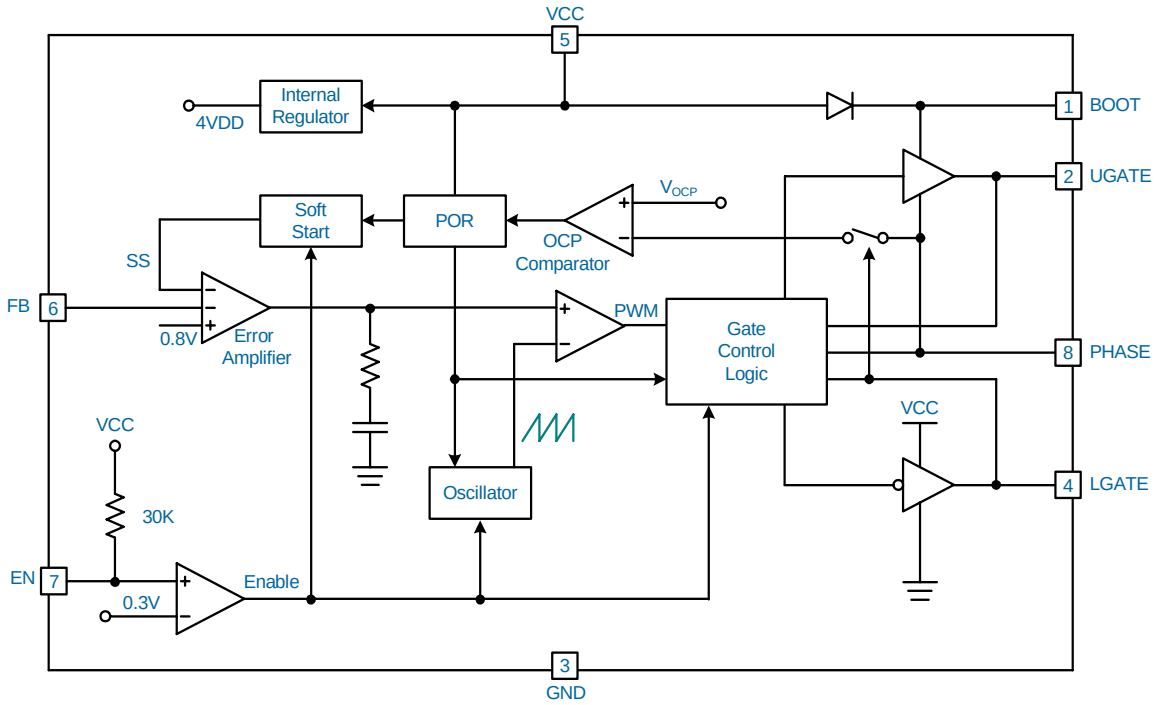




Functional Pin Description

No.	Pin Name	Pin Function
1	BOOT	**Bootstrap Supply** for the floating upper gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the PHASE pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Typical values for C_{BOOT} range from 0.1uF to 0.47uF. Ensure that C_{BOOT} is placed near the IC.
2	UGATE	**Upper Gate Driver Output.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
3	GND	**Signal and Power Ground for the IC.** All voltages levels are measured with respect to this pin. Tie this pin to the ground island/plane through the lowest impedance connection available.
4	LGATE	**Lower Gate Driver Output.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turn off.
5	VCC	**Supply Voltage.** This pin provides the bias supply for the uP6109 and the lower gate driver. The supply voltage is internally regulated to 4VDD for internal control circuit. Connect a well-decoupled 4.5V to 13.2V supply voltage to this pin. Ensure that a decoupling capacitor is placed near the IC.
6	FB	**Feedback Voltage.** This pin is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage. Use this pin in combination with the COMP/EN pin to compensate the voltage control feedback loop of the converter.
7	EN	**Chip Enable.** Pulling this pin lower than 0.3V disables the controller and causes the oscillator to stop, the UGATE and LGATE outputs to be held low.
8	PHASE	**PHASE Switch Node.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE driver, and to monitor the voltage drop across the lower MOSFET for over current protection. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.

Functional Block Diagram



Functional Description

The uP6109 is a compact synchronous-rectified buck controller specifically designed to operate from 5V or 12 supply voltage and to deliver high quality output voltage as low as 0.8V. This (P)SOP-8 device operates at fixed 300 kHz frequency and provides an optimal level of integration to reduce size and cost of the power supply.

Supply Voltage

The VCC pin receives a well-decoupled 4.5V to 13.2V supply voltage to power the uP6109 control circuit, the lower gate driver and the bootstrap circuit for the higher gate driver. A minimum 0.1uF ceramic capacitor is recommended to bypass the supply voltage. Place the bypassing capacitor physically near the IC.

An internal linear regulator regulates supply voltage into a 4.0V voltage 4VDD for internal control logic circuit. No external bypass capacitor is required for filtering the 4.0VDD voltage.

The uP6109 integrates MOSFET gate drives that are powered from the VCC pin and support 12V+12V driving capability. A bootstrap diode is embedded to facilitates PCB design and reduce the total BOM cost. No external Schottky diode is required. Converters that consist of uP6109 feature high efficiency without special consideration on the selection of MOSFETs.

Note: The embedded bootstrap diode is not a Schottky diode having a 0.7V forward voltage. External Schottky diode is highly recommended if the VCC voltage is expected to be lower than 5.0V. Otherwise the bootstrap diode may be too low for the device to work normally.

Power On Reset and Chip Enable

A power on reset (POR) circuitry continuously monitors the supply voltage at VCC pin. Once the rising POR threshold is exceeded, the uP6109 sets itself to active state and is ready to accept chip enable command. The rising POR threshold is typically 4.2V at VCC rising.

The EN pin is internally pulled high to VCC by a 30kΩ resistor as shown in Figure 1. A signal level NPN or NMOSFET transistor is adequate to pull this lower than 0.3V to shut down the device. When EN pin is released, it is pulled high and clamped to about 1.0V by internal zener diode.

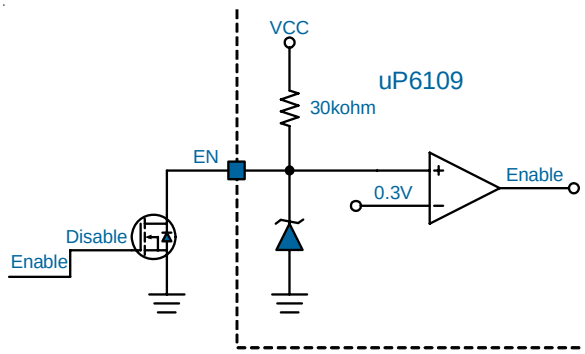


Figure 1. Enable Implementation of uP6109.

SoftStart

A built-in Soft Start is used to prevent surge current from power supply input during turn on (referring to the Functional Block Diagram). The error amplifier is a three-input device. Reference voltage V_{REF} or the internal soft start voltage SS whichever is smaller dominates the behavior of the non-inverting input of the error amplifier. SS internally ramps up to 4VDD in 50ms after the softstart cycle is initiated. The ramp is created digitally, so there will be 100 small discrete steps. Accordingly, the output voltage will follow the SS signal and ramp up smoothly to its target level.

The SS signal keeps ramping up after it exceeds the internal reference V_{REF}. However, the reference voltage V_{REF} takes over the behavior of error amplifier after SS > V_{REF}. When the SS signal climb to its ceiling voltage (5V), the uP6109 claims the end of softstart cycle and enable the under voltage protection of the output voltage.

For internal reference voltage, the effective ramp-up time of the output voltage is about 3.6ms.

For the uP6109 (300kHz operation frequency), the soft start is about 2.4ms.

Figure 2 shows a typical start up interval where the EN pin has been released from a grounded (system shutdown) state.

Functional Description

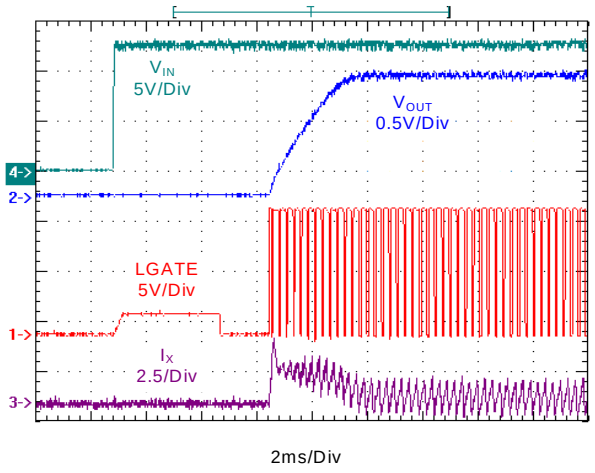


Figure 2. Softstart Behavior.

Power Input Detection

The uP6109 detects PHASE voltage for the present of power input when the UGATE turns on the first time. If the PHASE voltage does not exceed 3.0V when the UGATE turns on, the uP6109 asserts that power input in not ready and stops the softstart cycle. However, the internal SS continues ramping up to 4VDD. Another softstart is initiated after SS ramps up to 4VDD. The hiccup period is about 12ms. Figure 3 shows the start up interval where V_{IN} does not present initially.

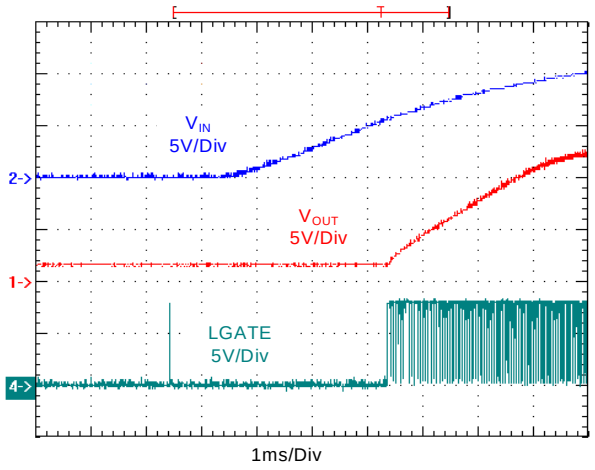


Figure 3. Softstart where VIN does not Present Initially.

Overcurrent Protection (OCP)

The uP6109 detects voltage drop across the lower MOSFET (V_{PHASE}) for overcurrent protection when it is turn on. If V_{PHASE} is lower than the user-programmable voltage V_{OCP}, the uP6109 asserts OCP and shuts down the converter. The OCP level can be calculated according the on-resistance of the lower MOSFET used.

$$I_{OCP} = -\frac{V_{OCP}}{R_{DS(ON)}} \quad (A)$$

Connecting a resistance from LGATE to GND selects the appropriate V_{OCP} as shown in Table 1. Also shown in Table 1 is OCP level if a lower MOSFET with 10mΩ $R_{DS(ON)}$ is used.

Table 1. OCP Level Selection

R_{OCP} (Ω)	open	42k	26k	10k
V_{OCP} (mV)	-375	-300	-225	-150
I_{OCP} (A)	37.5	30	22.5	15

When programming the OCP level, take into consideration the conditions that affect $R_{DS(ON)}$ of the lower MOSFET, including operation junction temperature, gate driving voltage and distribution. Consider the $R_{DS(ON)}$ at maximum operation temperature and lowest gate driving voltage.

Another factor should taken into consideration is the ripple of the inductor current. The current near the valley of the ripple current is used for OCP, resulting the averaged OCP level a little higher than the calculated value.

Undervoltage Protection (UVP)

The FB voltage is monitored for undervoltage protection. The UVP threshold level is typical 0.6V for both stand-alone and tracking mode. The uP6109 shuts down upon the detection of UVP and can be reset only by POR or toggling EN pin.

Absolute Maximum Rating

Supply Input Voltage, VCC (Note 1) ---------- -0.3V to +15V
PHASE to GND
DC ---------- -5V to 15V
< 200ns ---------- -5V to 30V
BOOT to PHASE ---------- 15V
BOOT to GND
DC ---------- -0.3V to PHASE +15V
< 200ns ---------- -0.3V to 42V
Input, Output or I/O Voltage ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
SOP-8 θ_{JA} ---------- 160°C/W
PSOP-8 θ_{JA} ---------- 50°C/W
PSOP-8 θ_{JC} ---------- 15°C/W
Power Dissipation, P_D @ T_A = 25°C
SOP-8 ---------- 0.625W
PSOP-8 ---------- 2.0W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC} ---------- +4.5V to 13.2V

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Voltage	V_{CC}		4.5	--	13.2	V
Supply Current	I_{CC}	UGATE, LGATE Open; V_{CC} = 12V, Switching	--	4	--	mA
Quiescent Supply Current	I_{CC_Q}	V_{FB} = 0.9V, No Switching	--	3	--	mA
Power Input Voltage	V_{IN}		3.0	--	13.2	V
Power On Reset						
POR Threshold	V_{CCRTH}	V_{CC} rising	4.0	4.2	4.4	V
POR Hysteresis	V_{CCHYS}		--	0.2	--	V
Oscillator						
Free Running Frequency	f_{OSC}	V_{CC} = 12V	255	300	345	kHz
Ramp Amplitude	ΔV_{OSC}	V_{CC} = 12V	--	1.5	--	V_{P-P}

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	55	70	--	dB
Gain-Bandwidth Product	GBW	Guaranteed by Design	--	10	--	MHz
Slew Rate	SR	Guaranteed by Design	3	6	--	V/us
Transconductance		Guaranteed by Design	--	--	0.7	mS
PWM Controller Gate Drivers						
Upper Gate Sourcing Current	I_{UG_SRC}	V_{BOOT} - V_{PHASE} = 12V, V_{BOOT} - V_{UGATE} = 6V	--	-1	--	A
Upper Gate $R_{DS(ON)}$ Sinking	R_{UG_SNK}	V_{UGATE} - V_{PHASE} = 0.1V	--	2	4	Ω
Lower Gate Sourcing Current	I_{LG_SRC}	V_{CC} - V_{LGATE} = 6V	--	-1	--	A
Lower Gate $R_{DS(ON)}$ Sinking	R_{LG_SNK}	V_{LGATE} = 0.1V	--	2	4	Ω
PHASE Falling to LGATE Rising Delay		V_{CC} = 12V; V_{PHASE} < 1.2V to V_{LGATE} > 1.2V	--	30	--	ns
LGATE Falling to UGATE Rising Delay		V_{CC} = 12V; V_{LGATE} < 1.2V to (V_{UGATE} - V_{PHASE}) > 1.2V	--	30	--	ns
Reference Voltage						
Nominal Feedback Voltage	V_{FB}	Stand Alone Mode	0.788	0.8	0.812	V
Enable Threshold						
Enable Threshold	V_{ENRTH}	V_{EN} rising.	0.6	--	--	V
Disable Threshold	V_{ENFTH}	V_{EN} falling.	--	--	0.3	V
Protection						
Under Voltage Protection	V_{FB_UVP}		0.55	0.6	0.65	V
Over Current Threshold	V_{PHASE}	R_{LGATE} Open	--	-375	--	mV
Soft-Start Interval	T_{SS}		2.4	3.6	4.8	ms

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

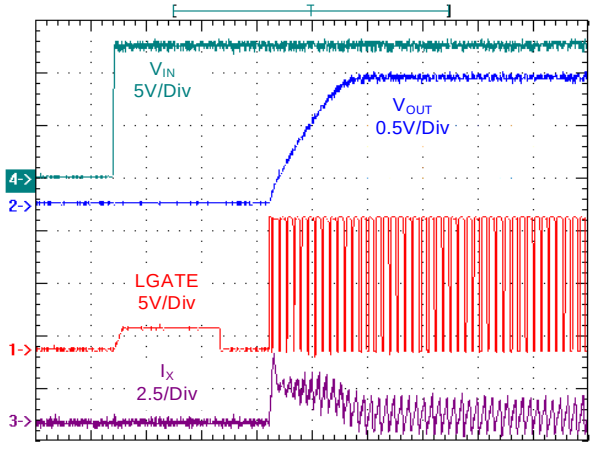
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

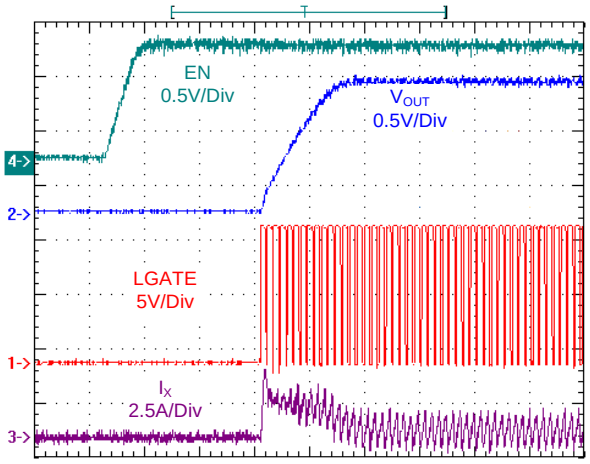
Typical Operation Characteristics

Power On Waveforms



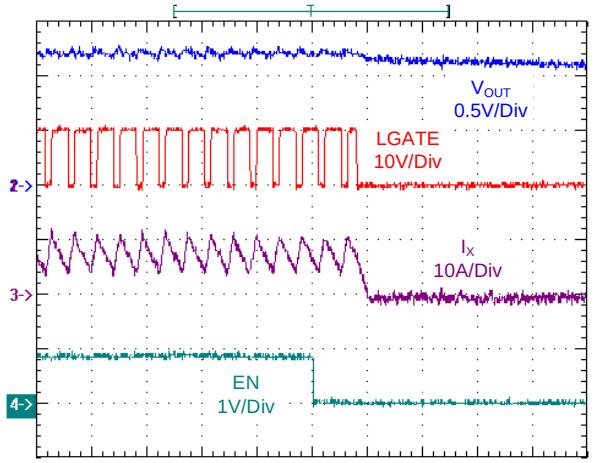
2ms/Div
V_{IN} =12V, V_{OUT} = 1.2V, C_{OUT} = 1500uF, No Load

Turn On Waveforms



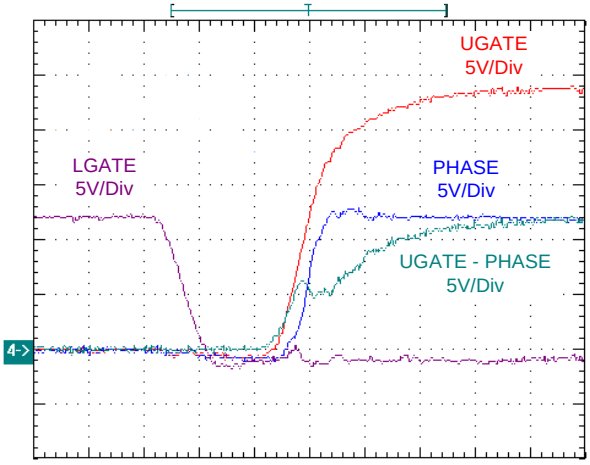
2ms/Div
V_{IN} =12V, V_{OUT} = 1.2V, C_{OUT} = 1500uF, No Load

Turn Off Waveforms



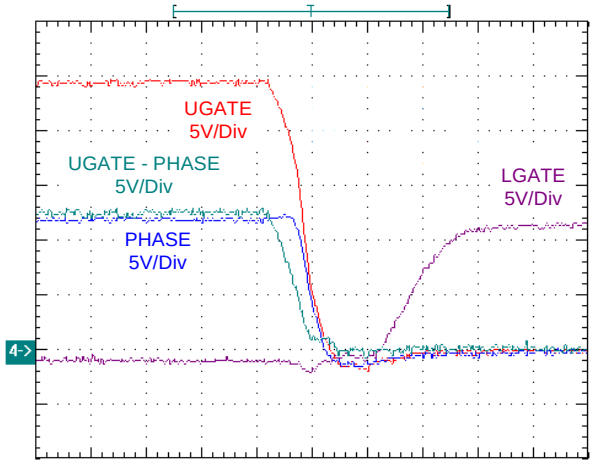
10us/Div
V_{IN} = 12V, V_{OUT} = 1.2V, C_{OUT} = 1500uF, I_{OUT} = 6A

Switching Waveforms: UGATE Turn On



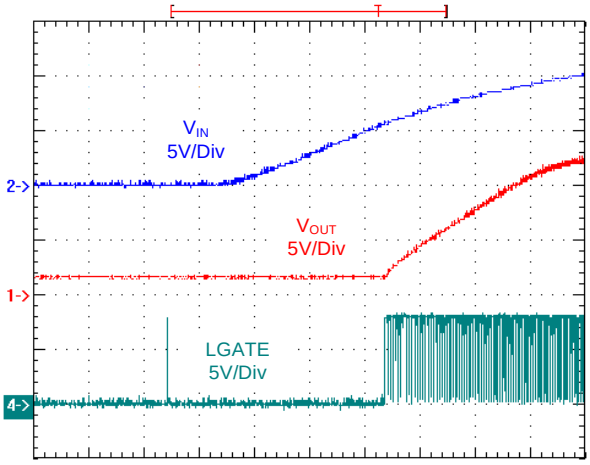
25ns/Div
V_{IN} = 12V, I_{OUT} = 10A

Switching Waveforms: UGATE Trun Off



25ns/Div
V_{IN} = 12V, I_{OUT} = 10A

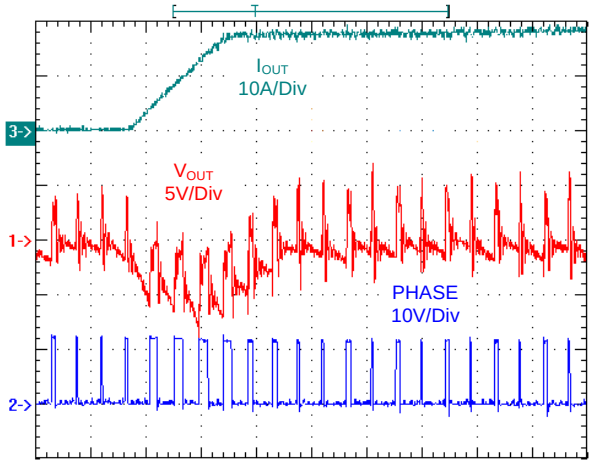
Power Sequencing Operation



1ms/Div
V_{CC} =12V Ready, V_{OUT} = 1.2V, C_{OUT} = 1500uF, No Load

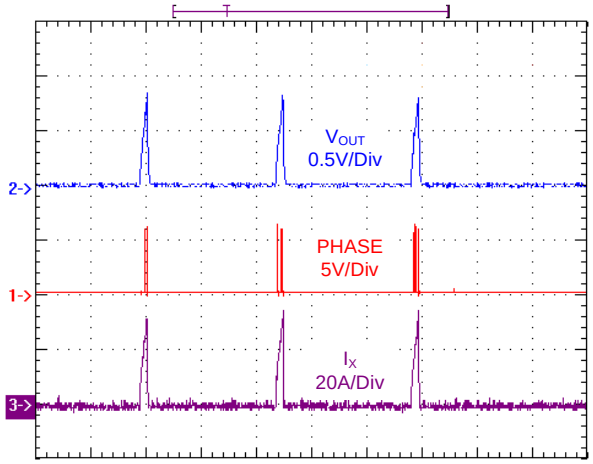
Typical Operation Characteristics

Load Transient Response



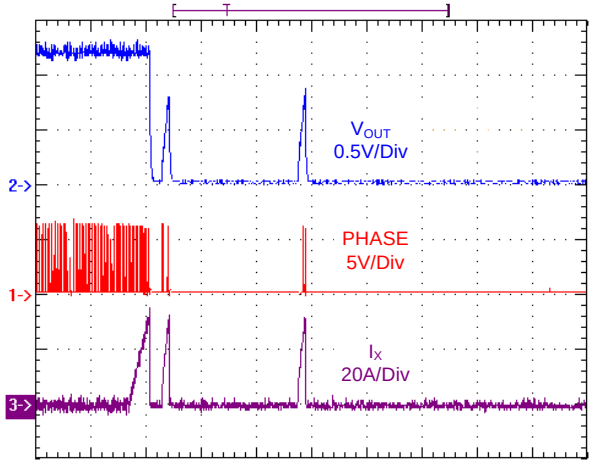
10us/Div
V_{IN} =12V, V_{OUT} = 1.2V, C_{OUT} = 1500uF

Over Current Protection



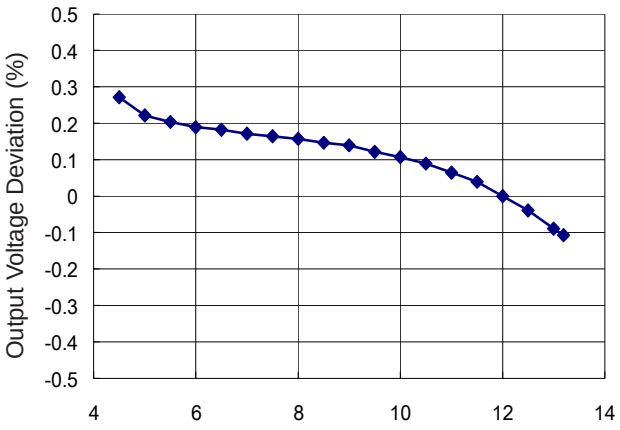
5ms/Div, V_{IN} = 12V, V_{OUT} = 1.2V, C_{OUT} = 1500uF,
Turn On to Short Circuit

Over Current Protection

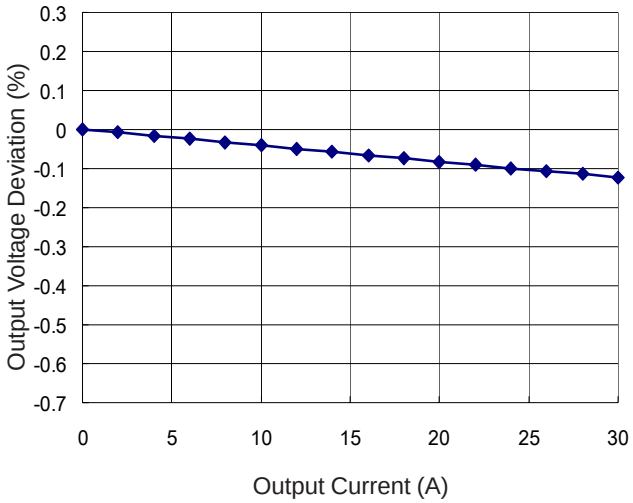


5ms/Div, V_{IN} = 12V, V_{OUT} = 1.2V, C_{OUT} = 1500uF,
Output Short to Ground

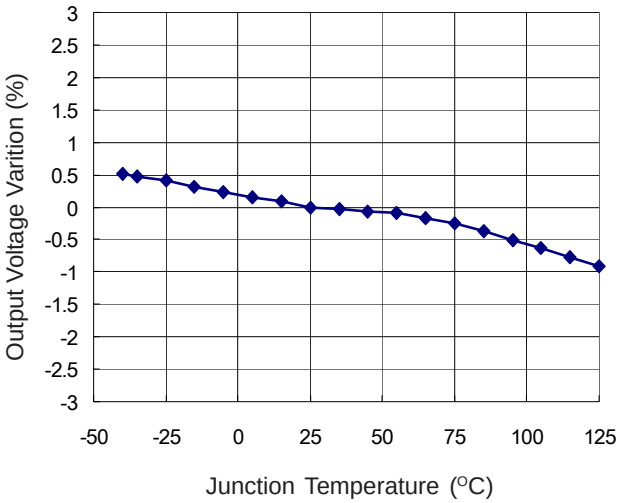
Line Regulation



Load Regulation

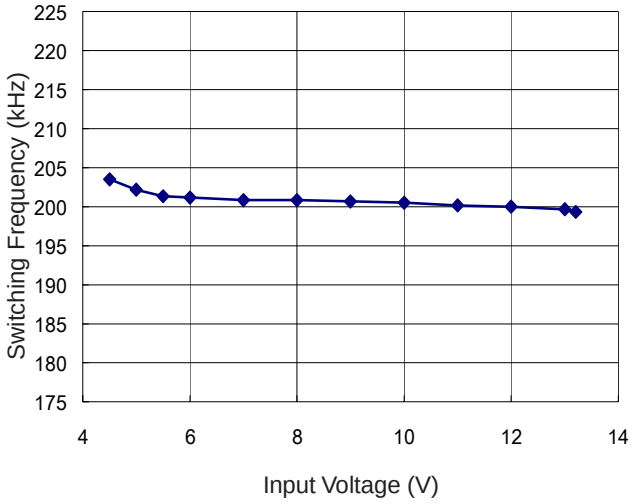


Output Voltage vs. Junction Temperature

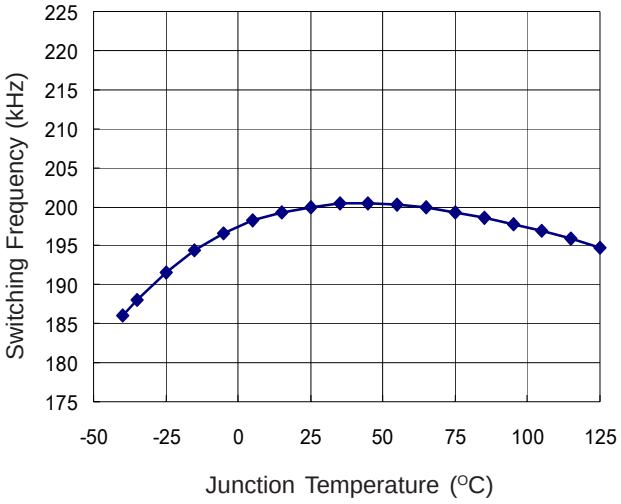


Typical Operation Characteristics

Switching Frequency vs. Input Voltage



Switching Frequency vs. Junction Temperature



Application Information

Power MOSFET Selection

External component selection is primarily determined by the maximum load current and begins with the selection of power MOSFET switches. The uP6109 requires two external N-channel power MOSFETs for upper (controlled) and lower (synchronous) switches. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, maximum current $I_{DS(MAX)}$, gate supply requirements, and thermal management requirements.

The gate drive voltage is powered by VCC pin that receives 4.5V~13.2V supply voltage. When operating with a 12V power supply for VCC (or down to a minimum supply voltage of 8V), a wide variety of NMOSFETs can be used. Logic-level threshold MOSFET should be used if the input voltage is expected to drop below 8V. Since the lower MOSFET is used as the current sensing element, particular attention must be paid to its on-resistance. Look for $R_{DS(ON)}$ ratings at lowest gate driving voltage.

Special cautions should be exercised on the lower switch exhibiting very low threshold voltage $V_{GS(TH)}$. The shoot-through protection present aboard the uP6109 may be circumvented by these MOSFETs if they have large parasitic impedances and/or capacitances that would inhibit the gate of the MOSFET from being discharged below its threshold level before the complementary MOSFET is turned on. Also avoid MOSFETs with excessive switching times; the circuitry is expecting transitions to occur in under 50 nsec or so.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty cycle. Since the uP6109 is operating in continuous conduction mode, the duty cycles for the MOSFETs is:

$$D_{UP} = \frac{V_{OUT}}{V_{IN}} \; ; \; D_{LO} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The resulting power dissipation in the MOSFETs at maximum output current are:

$$P_{UP} = I_{OUT}^2 \times R_{DS(ON)} \times D_{UP} + 0.5 \times I_{OUT} \times V_{IN} \times T_{SW} \times f_{OSC}$$

$$P_{LO} = I_{OUT}^2 \times R_{DS(ON)} \times D_{LO}$$

where T_{SW} is the combined switch ON and OFF time.

Both MOSFETs have I^2R losses and the top MOSFET includes an additional term for switching losses, which are largest at high input voltages. The bottom MOSFET losses are greatest when the bottom duty cycle is near 100%, during a short-circuit or at high input voltage. These equations assume linear voltage current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFET's body diode. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

The gate-charge losses are dissipated by the uP6109 and don't heat the MOSFETs. However, large gate charge increases the switching interval, T_{SW} that increases the MOSFET switching losses. The gate-charge losses are calculated as:

$$P_G = V_{CC} \times (V_{CC} \times (C_{ISS\_UP} + C_{ISS\_LO}) + V_{IN} \times C_{RSS}) \times f_{OSC}$$

where C_{ISS_UP} is the input capacitance of the upper MOSFET, C_{ISS_LO} is the input capacitance of the lower MOSFET, and C_{RSS_UP} is the reverse transfer capacitance of the upper MOSFET. Make sure that the gate-charge loss will not cause over temperature at uP6109, especially with large gate capacitance and high supply voltage.

Output Inductor Selection

Output inductor selection usually is based the considerations of inductance, rated current, size requirement, and DC resistance (DC)

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} \times V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$.

There is another tradeoff between output ripple current/ voltage and response time to a transient load. Increasing the value of inductance reduces the output ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

Application Information

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40°C temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements.

Input Capacitor Selection

The synchronous-rectified buck converter draws pulsed current with sharp edges from the input capacitor resulting in ripples and spikes at the input supply voltage. Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of upper MOSET and the source of lower MOSFET to avoid the stray inductance along the connection trace.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck converter is calculated as:

$$I_{IN(RMS)} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{IN(RMS)} = I_{OUT(RMS)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

For a through-hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can also be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}\right)$$

Since ΔIL increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout. Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on

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specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes.

However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading.

Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Bootstrap Capacitor Selection

An external bootstrap capacitor C_{BOOT} connected to the BOOT pin supplies the gate drive voltage for the upper MOSFET. This capacitor is charged through the internal diode when the PHASE node is low. When the upper MOSFET turns on, the PHASE node rises to V_{IN} and the BOOT pin rises to approximately V_{IN} + V_{CC}. The boot capacitor needs to store about 100 times the gate charge required by the upper MOSFET. In most applications 0.1uF to 0.47uF, X5R or X7R dielectric capacitor is adequate.

PCB Layout Considerations

High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Fast current switching from one device to another in a synchronous-rectified buck converter causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise that result in overvoltage stress on devices. Careful component placement layout and printed circuit design minimizes the voltage spikes induced in the converter.

Follow the layout guidelines for optimal performance of uP6109

1 The upper and lower MOSFETs turn on/off and conduct pulsed current alternatively with high slew rate transition. Any inductance in the switched current path generates a large voltage spike during the switching. The interconnecting wires indicated by red heavy lines conduct pulsed current with sharp transient and should be part of a ground or power plane in a printed circuit board to minimize the voltage spike. Make all the connection the top layer with wide, copper filled areas.

2 Place the power components as physically close as possible.

2.1 Place the input capacitors, especially the high-frequency ceramic decoupling capacitors, directly to the drain of upper MOSFET ad the source of the lower MOSFET. To reduce the ESR replace the single input capacitor with two parallel units

2.2 Place the output capacitor between the converter and load.

3 Place the uP6109 near the upper and lower MOSFETs with pins 1 to 4 facing the power components. Keep the components connected to pins 4 to 8 close to the uP6109 and away from the inductor and other noise sources (noise sensitive components).

4 Use a dedicated grounding plane and use vias to ground all critical components to this layer. The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs. Use an immediate via to connect the components to ground plane including GND of uP6109 Use several bigger vias for power components.

5 Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes to maintain good voltage filtering and to keep power losses low. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.

6 The PHASE node is subject to very high dV/dt voltages. Stray capacitance between this island and the surrounding circuitry tend to induce current spike and capacitive noise coupling. Keep the sensitive circuit away from the PHASE node and keep the PCB area small to limit the capacitive coupling. However, the PCB area should be kept moderate since it also acts as main heat convection path of the lower MOSFET.

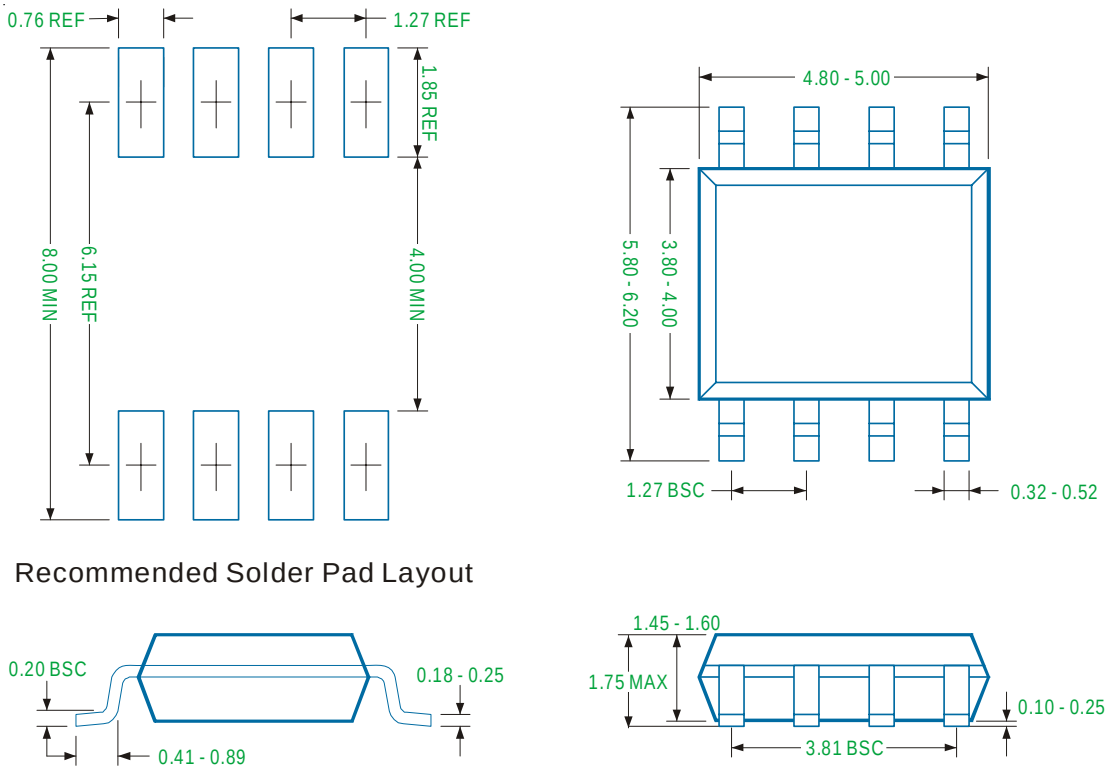
7 uP6109 sources/sinks impulse current with 2A peak to turn on/off the upper and lower MOSFETs. The connecting trance between the controller and gate/source of the MOSFET should be wide and short to minimize the parasitic inductance along the traces.

8 Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component.

9 Provide local VCC decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins.

Package Information

SOP - 8 Packagke

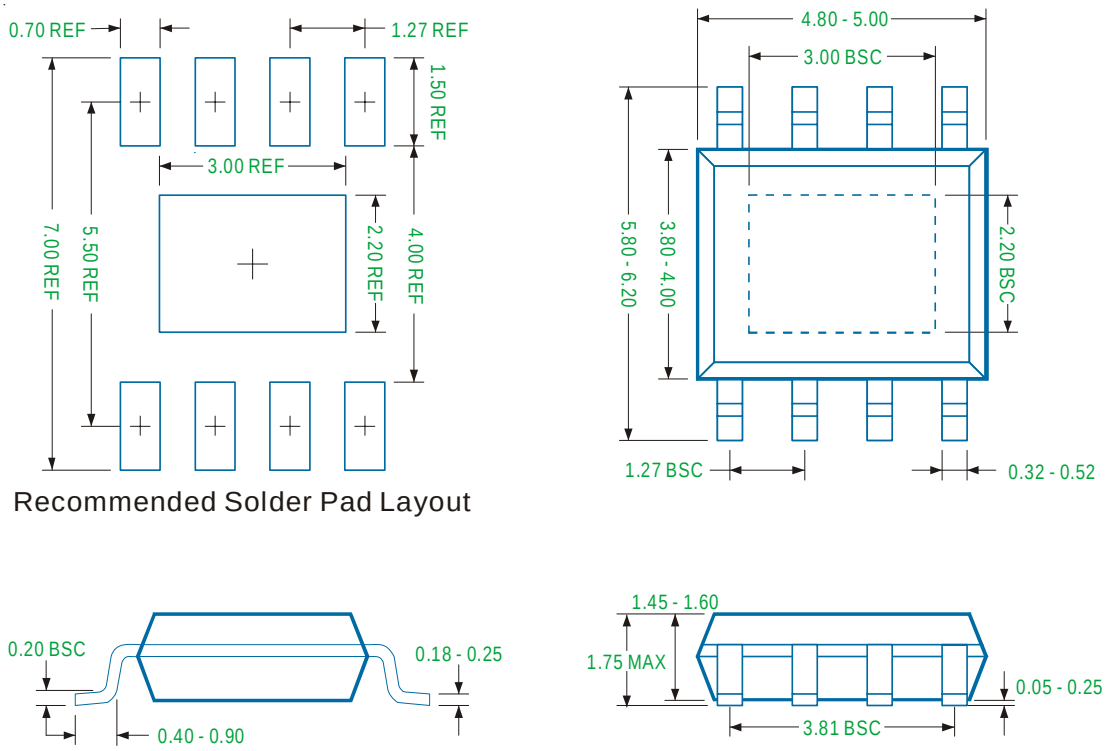


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions no not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.

Package Information

PSOP - 8 Packagke



Recommended Solder Pad Layout

Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions no not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.