design**ideas**

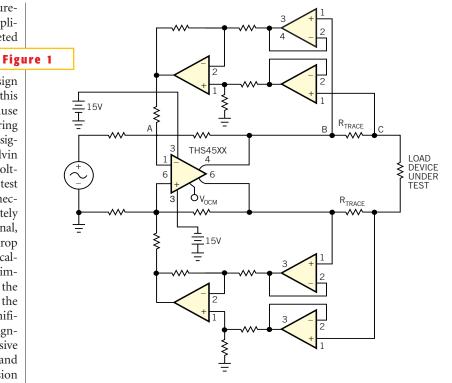
Edited by Bill Travis

Correct voltage drop and phase shift in transmission lines

Ron Shakery, Texas Instruments, Dallas, TX

ANY PRECISION test-and-measurement and high-speed analog applications require an exact targeted voltage to be delivered to the device under test or intended load to accurately analyze the device. Design and test engineers are well-aware that this goal is sometimes unattainable, because the impedance across the traces delivering the signal to the load alters the original signal. Traditionally, engineers use a Kelvin connection to measure the accurate voltage that the load or the device under test sees at its terminals. The Kelvin-connection method enables you to accurately measure the voltage at the load terminal, but it may not correct for the voltage drop or the phase shift that occurs dynamically across the signal lines with various impedances. In high-frequency signals, the RLC (transmission-line effects) of the traces come into play and cause a significant signal phase shift. As a result, designers always look for the least expensive methods to correct the voltage drop and the phase shift across the transmission lines. The circuit in Figure 1 is a fully differential line driver comprising a fully differential amplifier and two high-frequency, high-impedance feedback paths.

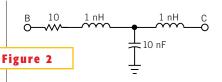
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This fully differential circuit compensates for voltage drop and phase shift in transmission lines.

The resistance associated with each trace causes a voltage drop through the path. Thus, the signal amplitude delivered to the load is lower than the signal amplitude at the output of the fully differential line driver. This voltage drop is proportional to the resistance value of the trace, R_{TRACE} , and the current flow through the corresponding trace. For example, if the output current of the line driver is 100 mA and the trace resistance is 10 Ω , a 1V drop develops across R_{TRACE} . As a result, if the output am-

plitude is 10V p-p, the load sees a 9V p-p signal. The feedback paths, which work as subtracters, accurately measure this voltage drop. The feedback paths measure the voltage drop across R_{TRACE} . This voltage then adds to the input of the line driver at the summing Node A. Because the circuit is symmetrical, the same function occurs at the opposite corresponding points. As a result, regardless of the value of the total voltage drop across R_{TRACE} , the sub-



This circuit represents a simulated transmission line inserted between points A and B of the circuit in Figure 1.

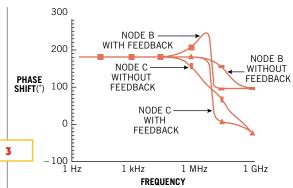


tracter measures it and adds it back into the input signal of the line driver. Consequently, the output of the line driver increases by the measure of the voltage drop across R_{TRACE} , and the load sees the exact voltage it was initially intended to see. Because the circuit is a closed-loop system and has negative feedback, the circuit remains in a stable condition.

The buffers in the feedback paths form a high-input-impedance node to prevent any load alteration. For example, without buffers, the series and parallel resistors of the subtracter would cause the value of the load to vary. These buffers, in conjunction with the subtracter, form an instrumentation amplifier. You can adjust this configuration for different gains to create variations of this circuit for different applications. The instrumentation amplifier creates a high-input-impedance path that works similarly to the sense lines of a Kelvin connection. The main difference is that the sense line in this circuit measures the actual voltage drop across R_{TRACE} over various frequencies and adds it back to the original signal. You should pay attention to the ratio of the line driver's gain configuration and the subtracter's gain configuration to ensure stability of the circuit. Additionally, you should verify that the bandwidths of the feedback-path devices are greater than the bandwidth of the line driver to prevent any added errors to the system via feedback paths' bandwidth limitations. You may choose to design the feedback paths with much greater bandwidth than the line driver (two times greater, for example). Doing so enables this circuit to correct the phase shift across the transmission line if the traces manifest RCL characteristics. Figure 3

For example, assume that you insert a transmission-line model between nodes B and C in the circuit of **Figure 1**, as in **Figure 2**. The bandwidth of the fully differential amplifier is 300 MHz at unity

gain, and the input signal is 2V p-p. The bandwidth of the feedback paths is 600 MHz to prevent any added phase shift to the signal from the feedback circuit. Configuring the test circuit as such lets you see the phase shift that the transmission line alone introduces. The transmission line causes a significant phase shift in the signal delivered to the load. Figure 3 shows the phase-shift curves at Node B before the transmission line and at Node C after the transmission line, right above the load. These curves show the effect of the feedback path in correcting the phase shift at the end of the transmission line where the load is located. This circuit configuration essentially corrects the phase shift of the signal that the RCL of the transmission line causes. The fully differential line driver enables you to deliver twice the voltage swing across the load as opposed



The phase-shift curves at Node B before the transmission line and at Node C after the transmission line show the effect of the feedback path in correcting the phase shift at the end of the transmission line.

to using a single-ended line driver with the same power supplies and similar specifications. However, the nature of fully differential configurations requires that you pay close attention to maintaining the balance of passive and active components to preserve the signal integrity delivered to the load. Therefore, you should set equal resistor values on the top and the bottom feedback paths. This design can correct for voltage drop and phase shifts across the transmission lines in low- and high-frequency cases. Design simplicity and the fact that the design uses few components make it cost-effective for many applications dealing with voltage-correction and phase-shift issues.

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Why limit your power supply's input range?

Michael Day, Texas Instruments, Dallas, TX

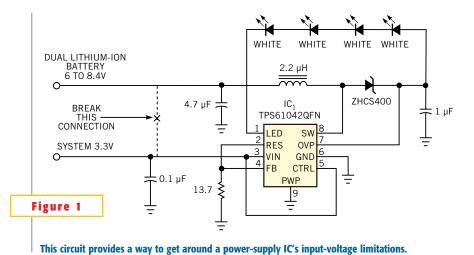
AKING ONLY A CURSORY LOOK at the input-voltage ratings of your powersupply IC can limit the usable inputvoltage range. With careful examination of an IC's operating specifications and circuit topology, you may be able to work around that input-voltage limitation. For instance, The data sheet for TI's (www.ti.com) TPS61042 shows that it has all the functions necessary for providing a constant-current drive to a white-LED circuit; however, the inputvoltage of the IC does not meet the inputvoltage requirements of this Design Idea. The dual lithium-ion input voltage varies from 6 to 8.4V, but the TPS61042 inputvoltage range is 1.8 to 6V. Closer examination of the circuit shows that the power stage need not connect to the same voltage rail as the control IC. **Figure 1** shows that by separating the input voltage to the TPS61042 from the power stage, you can power the LED driver from an input voltage greater than 6V.

The IC can receive power from any available system voltage of 1.8 to 6V by

connecting this voltage to the VIN pin. The input to the power stage can now connect directly to the battery. In general, the power stage can connect to any voltage that is lower than the required output voltage. With a boost topology, the input voltage to the power stage must be less than the output voltage, or the inductor and diode pass the input voltage directly to the output. The maximum allowable voltage on the SW pin, 28V, also limits the maximum input voltage to the power stage.

This technique also improves system ef-





ficiency. Efficiency data for this circuit shows that higher input voltages provide higher efficiency. If you have to run the LED driver from a voltage that is lower than 6V, the power to drive the LED is "double-converted." It first converts from the raw lithium-ion input into an intermediate system voltage and then converts from the intermediate-system voltage into the LED-drive current. By carefully examining the operating specs for the IC, you can get around around its input-voltage limitation, save cost and board space, and increase system efficiency.

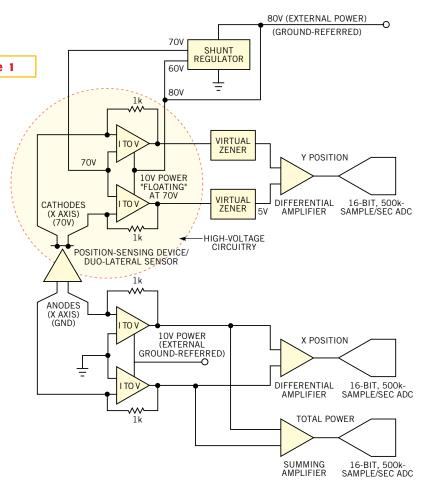
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Virtual-zener circuit simplifies high-voltage interface

Philip Lane, Transparent Networks Inc, Bellevue, WA

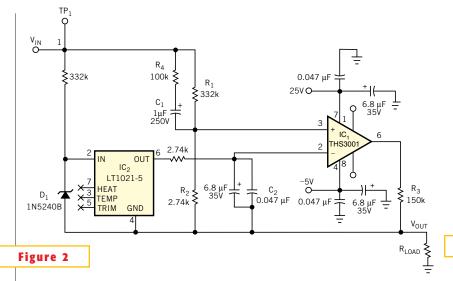
HIS DESIGN FOR a photonic switch needs more than approximately 70V at the cathode of a duo-lateral optical position-sensing device. **Figure 1** This voltage gets speedy response at longer wavelengths, such as 980 nm. The circuit uses fast transimpedance amps, "floated" at 70V. Two "virtual-zener" circuits step down the high-voltage signals for subsequent processing in a ground-referred differential-amplifier stage (Figure 1). The circuit drops exactly 65.58V dc with the component values shown, notwithstanding errors arising from op-amp offset voltages and resistor tolerances (Figure 2). The function of the virtual-zener circuit is to provide a regulated, floating dc voltage drop between input and output. The size of the drop depends on the ratio of R_1 to R_2 and the magnitude of the reference voltage. The input of the circuit, nominally at 70V dc, draws a constant 3.65 mA. The THS3001 sources or sinks this current plus any additional current as necessary, adjusting the output voltage until the voltages at its two inputs are equal. This equality occurs when $V_{z} = (V_{IN} - V_{OUT}) =$ $V_{RFF}(1+R_1/R_2).$

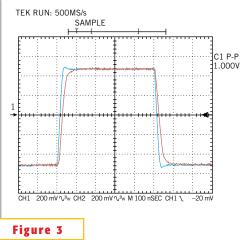
The op amp's power-supply rails and output range, along with the voltage drop across R_3 , limit the output-voltage compliance. C_1 bypasses R_1 . This bypass swamps the bandwidth-reducing effect of



"Virtual-zener" circuits simplify the high-voltage interface in this position-sensing system.







This virtual-zener circuit provides a regulated, "floating" voltage between the input and output.

capacitance at the noninverting input, and it greatly reduces the noise at the output. Without C_1 , the op amp's inherent noise would gain up by a factor of $(1+R_1/R_2)$. R_4 protects IC₁'s noninverting input by limiting the transient current supplied by C_1 during power-up and power-down. R_3 and the output, R_{IOAP} , have a similar protective effect on the inverting input, limiting any transient current in C_2 . R_3 is necessary to ensure feedback stability of the op amp. The inclusion of this resistor is standard operating procedure for a current-feedback op amp, such as the THS3001. If you use a voltage-feedback type, you could possi-

The transient response of the circuit in Figure 2 is exceedingly fast.

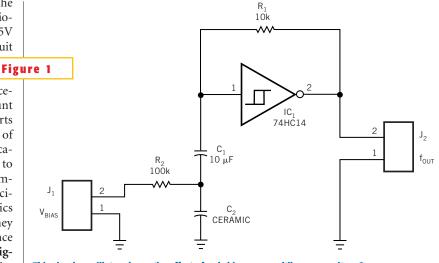
bly eliminate R_3 . Bandwidth is extremely high. **Figure 3** shows the pulse response at 100 nsec per division. (Blue is the input, and red is the output.)

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Multilayer capacitor doubles as varactor

Susanne Nell, Breitenfurt, Austria

HE MAIN PURPOSE for building the circuit in Figure 1 is to study the idiosyncrasies of X5R, Z5U, and Y5V multilayer ceramic capacitors. The circuit is also an inexpensive VCO (voltage-controlled oscillator) with only five components. Many types of ceramic capacitors for surface-mount placement are on the market. The parts become continually smaller because of space problems on the board, and the capacitance values continually increase to compete with more expensive tantalumelectrolytic units. Unfortunately, capacitors with X5R, Z5U, or Y5V dielectrics have some undesirable properties. They exhibit voltage-dependent capacitance values. The idea behind the circuit in Figure 1 is to check the influence of a dc bias

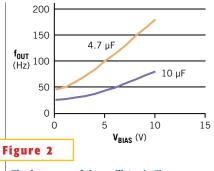


This simple oscillator shows the effect of a dc bias on a multilayer capacitor, C2.



voltage on the frequency of a simple oscillator. The net result is a low-frequency VCO with a relatively large voltagegain figure, which depends largely on the type of capacitor you use.

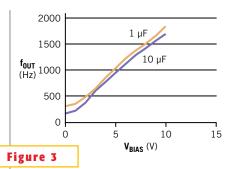
The circuit is a simple oscillator using a Schmitt-trigger inverter. The frequency is a function of R_1 , C_1 , and C_2 . C_2 is the



The frequency of the oscillator in Figure 1 exhibits almost a 4-to-1 shift for a 4.7- μ F Z5U multilayer capacitor.

ceramic capacitor with voltage-dependent capacitance. Using the value of C_1 , you can shift the frequency independently of C_2 . This design uses a stable-foiltype capacitor for C_1 to avoid bias-voltage-dependent effects in the measured results. If necessary, you can compensate the temperature coefficient of the capacitor with a combination of NTC,

PTC, and metal-film resistors for R₁. For measurements, this design uses a simple metal-film resistor. The capacitance change with temperature is normally less than 10% from 10 to 35°C for Z5U and Y5V and much lower for X5R. **Figure 2** shows the measured voltageversus-frequency graphs with different values and types for C₂. For **Figure 2**, $C_1=10 \ \mu$ F; the orange curve represents a 4.7- μ F, 10V, Z5U multilayer capacitor, and the purple curve represents a 10- μ F, 10V, Z5U multilayer capacitor. **Figure 3** shows similar plots for values of C₁ (or-



The value of C₁ has little effect on the frequency curves for the circuit in Figure 1.

ange: 1 μ F; purple: 10 μ F). The moral of the story is: Be wary when using high-capacitance ceramic capacitors with high or variable dc bias; the varying capacitance can greatly influence circuit performance.

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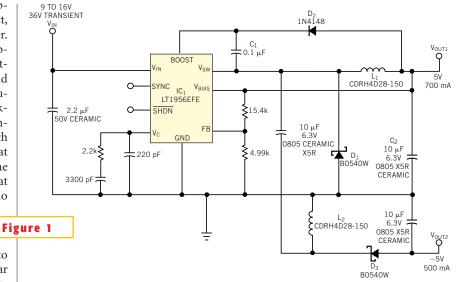
Buck regulator and two inductors make dual-polarity converter

Keith Szolusha, Linear Technology Corp, Milpitas, CA

COMMON PROBLEM for power-supply designers is to create a compact, dual-polarity step-down converter. If space and cost are not concerns, the obvious solution is a pair of dc/dc converters, one for each output. But space and cost are almost always issues for communications, data-acquisition, and diskdrive applications. **Figure 1** shows a single current-control- regulator approach that supplies 5V at 700 mA and -5V at 500 mA from a 12V system source. The circuit features efficiency similar to that of a two-regulator solution and has no

component measuring more than 3 mm high. The low profile and low board real estate that this de-

sign requires are almost impossible to match using a flyback design or a similar dual-output SEPIC design using a transformer instead of two inductors. Note, however, one important limitation of this circuit that makes it inappropriate for some applications: For the circuit to maintain regulation, the positive load



This dual-polarity dc/dc converter uses a single-switch buck regulator.

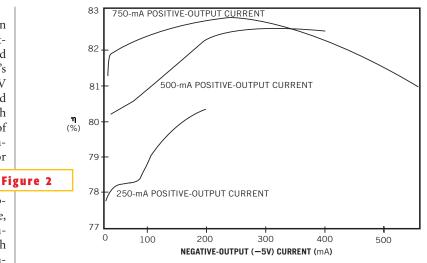
must always outweigh the negative load. **Figure 2** shows some efficiency curves at various positive-output currents.

The dual-polarity output circuit is

similar to that of a typical single-output positive buck regulator. The circuit adds a secondary negative output by attaching a coupling capacitor (C_1) , a second in-



ductor (L_2) , a catch diode (D_3) , and an output capacitor (C_2) . The negative output voltage maintains regulation based on the voltage of the coupling capacitor's remaining constant and equal to the 5V output voltage. Current ramps up and down in the secondary inductor, L₂, with the same peak-to-peak ripple as that of the primary inductor, L1. The low-impedance path of the coupling capacitor provides the current to L, during the on-time of the switch and induces the same voltage across L₂ as appears across L₁. The Schottky catch diode, D₃, provides a current path for the inductor during the off-time of the switch and a current path from the coupling capacitor when discharging into the positive output. Current must flow from the coupling capacitor into L₁ during the offtime of the switch for the capacitor to discharge all the charge gained during the on-time of the switch. This current flow-



These curves represent efficiency figures for various positive and negative output currents.

ing into the positive inductor during the off-time takes the place of some of the current that would normally be sourced from the positive catch diode, D₁, reduc-

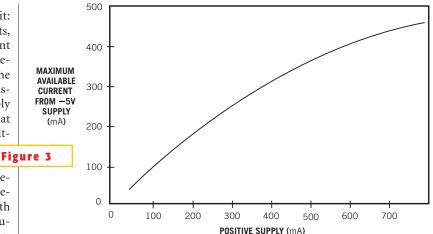
ing the losses in D_1 but increasing the losses in D_3 .

The need for the coupling capacitor to charge and discharge equally creates



an important limitation of the circuit: To maintain regulation on both outputs, the negative-supply output current must always be less than the positivesupply output current (**Figure 3**). If the negative-supply output current increases enough to equal the positive-supply output current, regardless of how great the positive current is, the output volt-

age begins to collapse. Also, if the negative-supply output current is too low (below 5 to 25 mA, depending on input voltage), the negativesupply voltage can balloon. With extremely light negative loads, the coupling-capacitor discharge current during switch off-time and the inductor current (L_2) during switch on-time come only from the negative output capacitor, C_2 (as opposed to both the negative output capacitor and the negative dc load). Thus, the output capacitor charges well past its intended voltage



This curve gives the maximum available negative-output current as a function of positive-supply current.

because no negative dc load is available to discharge the capacitor. If you use this circuit in an application in which the negative output will see light loads, use a 25-mA preload to maintain regulation.

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