Edited by Bill Travis

Simple phototimer controls load

Abel Raynus, Armatron International, Melrose, MA

N INDUSTRIAL and home applications, the need **Figure 1** sometimes exists for a device that, after activation by some physical effect, such as light, temperature, or sound, switches a load on for a predetermined time. The load, such as a lamp, motor, solenoid, or heater, usually derives its power from the ac line. The phototimer in Figure 1, based on an inexpensive MC68HC705KJ1 microcontroller, is a simple and inexpensive way to satisfy this need. A load switches on when it becomes dark and stays on for an interval that an operator sets with the Hours pushbutton

switch. A seven-segment LED display shows the interval. The time value is a function of the design objectives, the microcontroller software, and the displayinterface complexity. The design in **Figure 1** is simple, because it needs only one pushbutton switch and a single-digit display.

The heart of the design is the microcontroller software (**Listing 1**). The routine serves manual and automatic operating modes. The initialization process sets the manual, or continual, mode. This

Simple phototimer controls load	
Delay line upgrades vintage scope	94
Circuit reduces negative-voltage stresses on control IC	98
Track multisite temperatures on your PC	
Publish your Design Idea in <i>EDN.</i> What's Up section at www.ednmag	See the g.com.



When it becomes dark, this circuit turns the load on for a predetermined interval.

sign**ideas**

0000 2 Sligt SPAGEWIDTH 160 0000 з 0731 resistor osc and input pulldown 4 org MOR; 5 fcb %00100000; 0791 20 6 0792 LHD 7 equ pA0 equ pAl 0782 8 g t 0772 . equ pA2 10 equ pA3 0792 å 0772 11 equ pA4 0772 12 c equ pAS 0772 13 ъ equ pA6 0792 14 equ pA7 a Photo equ pB2 07F2 15 0772 16 Load equ pB3 ** VARIABLES ********************************* 17 0000 18 org RAM 0000 19 Treg rmb 1 ;Time register 0001 20 Tent rmb 1 (Time counter 0002 21 cntlh rmb 1 ; counter for 1 hour 0003 22 rmb 1 ;counter for 30 sec cnt30s 0004 23 cnt1s rmb 1 (counter for 1 sec 24 7-segment CODE TABLE address ******* 0005 25 adr7s RCMend+1-\$0b ; for 11 constants equ 26 INITIALISATION *************** 0300 21 org ROM 0300 [02] A6FF 28 init 1da #SEE rest prtA as output 0302 [04] 8704 29 sta ddrA [05] 3700 30 prtă ; 3,ddr5 ;set pB3 as output 0304 clr 31 0306 [05] 1605 bset 0308 [05] 32 belr Load, prtB ; set Load 1701 off ;clear A010 [05] 3FC0 33 clr Treg 030C [05] 3FC1 34 clr Tont a11 35 0308 [05] 3FC2 clr cnt1h registers 0310 [05] 3FC3 36 clr cnt30s used [05] 0312 37C4 37 olr cnt1s (continued on pg 94) 0314 [02] 38 cli

LISTING 1–ROUTINE FOR PHOTOTIMER-LOAD CONTROLLER

www.ednmag.com

designideas

setting means, that after a 30-sec delay, the load switches on and stays on until you press the Reset pushbutton. The 30sec delay allows you to change your mind and choose an automatic mode. During the manual mode, the display exhibits "C" for continual. The dot on the display lights every time the load is on, a useful feature when the timer and the load are far away from each other. By pressing the Hours pushbutton, you change the manual mode to an automatic one. In the automatic mode, the display exhibits a time delay in hours. When you press and hold the pushbutton, the digits increment automatically from 1 to 9 every second. This feature comes about by using counter modulo 9 in the external interruptservice routine (lines 85 to 92 in Listing 1). You can download the software associated with this circuit from the Web version of this Design Idea at www. ednmag.com.

After the time-delay setting elapses, the microcontroller waits for night-in other words, for a high level on the Photo input-to switch on the load. During that wait, the dot in the display blinks in 1-sec intervals. When it becomes dark, the LM393 voltage comparator's output switches high and triggers the program to continue. The load switches on, and the dot in the display stops blinking and stays on. The display digit shows the elapsed working time. When this time expires, the load and the dot in the display switch off, and the display exhibits "E." You can stop the process at any time by pressing the Reset pushbutton. Otherwise, the microcontroller automatically repeats the entire sequence every night. The circuit in Figure 1 is extremely flexible. The circuit can switch on the load using any physical effect just by changing the sensor on the comparator input. You can also modify the software for different time delays. As an example, you might want to display two-digit hours and twodigit minutes. In this case, you should use decoder/drivers, such as the CD4511 or MM74HC138, to configure an interface with the display.

Is this the best Design Idea in this issue? Select at www.ednmag.com.

LISTING 1-ROUTINE FOR PHOTOTIMER-LOAD CONTROLLER (CONTINUED)

							•
0315	[03]	BECO	39	main	ldx	Treg	Treg> X
0317	1061	CD0363	40		jar	display	Time> display
0318	[06]	CD03A8	41		isr	dly30s	:delay 30 sec
0310	1041	3000	42	mode	tet	Treg	TTeg = 07
0218	1031	2740	41		her	manual	
0278	[03]	2140			hele	A NO. OWNER	100 .00
0321	1021	1100	44		beir	LED, pres	A PERD OIL
0323	[05]	1701	45		belr	Load, prt	tB iLoad off
0325	[05]	050130	46	Auto	brelr	photo, pr	rtB, blink; is it a day?
0328	1051	1100	47		belr	LHD, prtJ	LED off
032A	1061	CD03A8	48		far	d1v30s	(delay for 10 sec
0120	1051	050139	4.9		brelr	photo n	the blink is a day?
0320	[os]	100120			brek	Lood must	to toad on
0330	1051	LOVA	50		heet	annes, pres	
0332	1021	1000	51		bset	LED, pres	A JLED ON
0334	[03]	B6C0	52		lda	Treg	Treg> Tent
0336	[04]	B7C1	53		sta	Tent	
0338	[06]	CD03B4	54	work	jar	dlyih	; delay for 1 hour
0338	[05]	3AC1	55		dec	Tont	/decrement Tont
0330	1031	2707	56		beg	TimeEnd	time is expired
0338	1031	mmers.	6.7		lde	Pank	"Tank ask V
0000	10.01	00000	50		Lak	dim.	prene> A
0341	[OP]	CD0363	58		Jar	arspray	tues true> grebral
0346	[03]	20F2	59		bra	MOLK	100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100
0346	[05]	1701	60	timeEn	d belr	Load, prt	tB ;Load off
0348	[02]	ABOA	61		ldx	#\$a	7"E"> display
034A	1061	CD0363	62		Ser	display	
0340	1051	0401FD	63	night	brast	photo.pr	tB.night;wait for a dawn
0350	1061	000384	64	and here		diath	idelay for 1 hour
0350	Lon1	0.003.04			300	shoke as	The and the state of the state
0353	1051	040187	63		DIBOL	photo, pi	replusheriant for a daap
0356	[03]	2080	66		bra	main	
			67	******			
0358	[06]	CD039C	68	blink	jer	dlyls	;delay 1 sec
0358	[03]	3600	69		lda	prtA	
0350	[02]	A801	70		ear	#%000000	001
015F	[GAT	8700	23			DELA	
0.000	LAN!	20.00	20		here	Buches	
0361	[03]	2002	72		DTA	AUCO	
		1011230000	73				
0363	[05]	D607C5	74	display	y 1da	adr75,x ;	code, x> Acc
0366	[04]	B700	75		sta	prtA .	Acc> prtA
0368	[05]	070102	76		brelr	Load, prti	8, disEnd ; is Load off?
0268	Lost	1000	77		heat	LED orta	LED on
0308	1491	1000		A1	Lane.	num be nu	waturn from dianlar
036D	1001	17	7.0	disand	TER		recurn from display
			79				
036E	[05]	1000	80	manual	bset	LED, prt/	A /LED on
0370	[05]	1601	81		bset	Load, prt	tB ;Load on
0372	[03]	2089	82		bra	node	
	10.01	000000				41	debourding delow 100 ms
0374	Inel	CD0393	83	EXCIDE	Jer	grace 1	debounding delay 100 mm
0377	[03]	2912	84		DIN	m3 1	if imgel, and of interrupt
0379	[03]	BECO	85	an O	ldx	Treg /	Treg>X
0378	[02]	A309	86		cpx	#9 ;	Treg > 97
0370	[03]	2405	87		bhs	ml	
0378	1051	3000	88		inc	Treg	Treg + 1
0303	1031	10000	8.0	-2	1 de	Tree	Tran
0201	1001	0000			dan	diaplant .	Twon dienlaw
0383	roe1	CD0363	20		345	grabray :	tred> grabink
0389	[00]	GD039G	91		3er	divis (delay 1 sec
0389	[03]	2EEE	92		bil	m0 /	is IRQ-pin still low ?
0388	[05]	120A	93	m3	bset	IRQR, ISCS	R ;IRQ reset
038D	[09]	80	94		rti		return from ExtInt
0388	[05]	3FC0	95	ml	clr	Treg	0> Treg
0190	[03]	2087	96		bra	#2	
	1001				14- 410		
0393	[02]	A680	97	divois	1da #12	BT 11	LOG ms delay
0394	[03]	5.9	98	1p1	CILK		
0395	[03]	53	99	1p2	decx		
0396	[03]	26FD	100		bne 1p2		
0398	[03]	48	101		deca		
0399	[031	2679	102		bne lot		
0205	Inci	81	107		with apra		
49310	1001		202				
			104		1.4.		
0390	[02]	ACUA	105	grÅ18	104 #10	10'1%	wrosisec dersh
0398	[04]	8704	106		sta cht	18	
0320	[06]	CD0392	107	dls	jsr dly	01s	
03A3	[05]	3AC4	108		dec cnt	18	
0385	[03]	2689	109		bne dla		
0387	[06]	81	110		rts		
- cost			111	******			
0250	Len1	3618	33.3	d1-20-	14- 430		30mm dalam
0.246	ford1	2012		arA308		2301	tone certal
AACO	1041	8703	113	1000	sta cht	308	
03AC	[06]	GD039G	114	d39s	jar dly	18	
03AF	[05]	3AC3	115		dec ont	30s	
03B1	[03]	26F9	116		bne d30	10	
0383	1061	81	117		rts	598) î	
10000			110				
0.204	LOCT	3674	11.0	41-11	14- 44-	AT	120-1 hour
0384	102]	A018	119	aryth	1da #12	AL 1308 X]	Livel nour
0386	[04]	B7C2	120	100 C	sta ont	18	
0388	[06]	CD03A8	121	dlh	jar dly	30s	
0388	[05]	3AC2	122		dec cnt	lh	
0380	1031	26F9	123		bne dih		
0387	IDET	81	124		rte		
0205	thel	7.4	100				
-			140				
0705		REAL PROPERTY.	126		org	adr7s	
10.000		9C60DAF2	127		fcb	\$90,\$60,\$	5da, \$12, \$66
07C5							
07C5		66					
07C5		66 B63EE0FE	128		fcb	\$56,\$38.5	eD, \$fe, \$e6, \$9e
07C5 07CA		66 B63EE0FE E69E	128		fcb	\$66,\$38,\$	\$eD,\$fe,\$e6,\$9e
07C5 07CA		66 B63EE0FE E69E	128		fcb	\$66,\$30,\$	00,\$fe,\$e6,\$9e
07C5 07CA		66 B63820FR E69E	128 129		feb	\$66,\$3e,\$	teD.Sfe.Se6.S9e
07C5 07CA 07FA		66 B63EE0FE E69E	128 129 130		fcb org	\$56,\$3e,\$	5eD,\$fe,\$e6,\$9e
07C5 07CA 07FA 07FA		66 B63EE0FE E69E 0374	128 129 130 131		fcb org fdb	\$b6,\$3e,\$ vectors+2 ExtInt	}eD,\$£⊕,\$e6,\$9⊕ 1
07C5 07CA 07FA 07FA 07FB		66 B63EE0FE E69E 0374	128 129 130 131 132		fcb org fdb org	\$56,\$3e,\$ VECTORS+2 ExtInt VECTORS+6	;aD,\$£⊕,\$a6,\$9⊕



Delay line upgrades vintage scope

Robert Houtman, Blaine, WA

INTAGE TRIGGEREDsweep oscilloscopes find use in many applications. However, they have no internal delay line, so they can't display the pulse that triggers the sweep. Moreover, early laboratory scopes con-

tain delay lines hav-

display such pulses during a uniform portion of the sweep. With such oscilloscopes, the true pulse shape remains a mystery. You can circumvent these limitations if you add an external delay line and equalizer. The scope can then display the exact triggerpoint trace. The instrument then becomes easier to use, and the measurements become more trustworthy. For every additional microsecond of equalized cable, the scope can display a microsecond of pretrigger information. Figure 1 shows the components you need to implement these improvements on a Philips PM3230 10-MHz oscilloscope. The components are a wideband amplifier to restore the signal to its original level and provide a trigger; a 750-nsec delay cable; and a passive, two-stage equalizer.

CATV cables, such as RG6U, RG59U, and others, are commonly available at garage sales and second-hand stores. You connect the 75 Ω cables with solid or

Figure 2 foam dielectrics using standard CATV connectors to make | ing the cable (b), differ. the 750-nsec delay line. A low-im-

pedance driver displays the bipolar step response of the delay line, as the eye pattern in Figure 2a shows. The delay line transmits approximately 65% of the signal at audio frequencies, because of resistive losses. The losses increase at higher radio frequencies, because of the skin effect in the conductor. The theoretical form for the step response that the skineffect loss causes is a complementary er-



ing insufficient delay to | This circuit modifies vintage oscilloscopes having no internal delay line.







ror function, $\operatorname{cerf}(kl/\sqrt{t} \ (\text{Reference 1}).$ The time, t, refers to the start of the step after traversing the cable of 160m length. Computer evaluation of this function shows the constant to be $k=2.6\times$ $10^{-7}(sec)^{0.5}/m$ for best agreement with the step response in Figure 2a. You cannot adequately correct this functional form by using the usual single-bridged-T filter. You therefore apply time-domain methods to obtain the two-stage, pole-zerocancellation equalizer in Figure 1 (Reference 2). This double-bridged-T filter corrects the cable's phase and amplitude distortion over a 10-MHz band.

Each of these two filters is basically a resistive attenuator, but fast

steps can bypass the attenuation during a time constant, τ . For short times, the equalizer's input port sees a load of only the 75 Ω cable via the capacitor, which presents a short circuit at high frequencies. The inductor presents an open circuit at high frequencies, so the resistors have no effect for short times. Eventually, as t surpasses τ in the step response, the capacitor and inductor yield to the resistive attenuator while presenting the 75Ω load to the equalizer's input. With only the first, $\tau = 180$ -nsec filter, the step response becomes a more finely rounded waveform. With the second, τ =25-nsec filter, the step response is a sharp step, limited only by the oscilloscope's bandwidth. Each filter resides in a reclaimed CATV signalsplitter box. You can connect these 75 Ω constant-resistance filters at various locations along the delay line without incurring reflections. You can therefore use this arrangement to fine-tune the passive components to eliminate residual reflections, using time-domain reflectometry.

The AD8055-based amplifier has greater-than-100-MHz bandwidth, fully adequate for the 10-MHz oscil-

loscope. Its input impedance is 1 M Ω in parallel with 30 pF to match the oscilloscope's input and its low-capacitance probes. Figure 2b shows the final eye pattern, using the amplifier, the two-stage equalizer, and the 750-nsec delay cable. This pattern is essentially identical to the eye pattern that ensues using the oscilloscope without the circuit in Figure 1, except for the 750-nsec temporal shift. You



can see the benefit of the circuit in **Figure 3**. Trace A shows the original impulse response of the oscilloscope without the circuit. Trace A is merely an uninteresting, featureless trace. For Trace B, the input impulse passes through the amplifier to the external-trigger input and then through the equalizer and delay cable to the oscilloscope's input. Because its delay is longer than the intrinsic delay of the oscilloscope in starting its sweep, a clean pulse of approximately 20 nsec appears on the display. You can now use the complete unit as a 10-MHz laboratory oscilloscope.

You can define an input impulse as an even function composed purely of cosine waves of zero phase. However, the cable's impulse response is simply the derivative of the waveform in **Figure 2a** and acquires a long, slow tail. This impulse re-



Figure 3Traces A and B show the impulse
response, respectively, without and with
nnthe delay network.

sponse is thus no longer an even function, so its composite cosine waves have evidently acquired various phase shifts accruing to the cable. **Figure 3** illustrates that the circuit in **Figure 1** corrects these phase shifts and amplitude variations. Trace B shows a short, symmetrical pulse with no tail, an even function as similar as possible to the input impulse using this oscilloscope.

References

1. Nahman, NS, "The measurement of baseband pulse risetimes of less than 10^{-9} second," *Proceedings* of the IEEE, Volume 55, No. 6, June 1967, pg 855.

vith 2. Houtman, Hubert, "1-GHz sampling oscilloscope front-end is easily modified," *Electronic Design*, Sept 18, 2000, pg 175.

Is this the best Design Idea in this issue? Select at www.ednmag.com.

Circuit reduces negative-voltage stresses on control IC

Michael Day, Texas Instruments Inc, Dallas, TX

N A SYNCHRONOUS, buck switching power supply, the two FETS and the output inductor meet at the phase node (Figure 1). The phase node often connects directly to the control IC. The voltage on this node swings from the input voltage to some voltage lower than ground. If the voltage goes too far below ground, the ESD structures or other circuitry within the control IC can become forward-biased, causing currents to flow through the chip's substrate. These unwanted currents can cause erratic behavior and damage to the IC under certain circumstances. Although it is impossible to keep the phase node from going below ground, it is necessary to keep the voltage at the control IC from going so far negative that it adversely affects or damages the IC.

Trace A in **Figure 2a** shows the phasenode voltage waveform with $V_{IN}=12V$, and $V_{OUT}=3.5V$ at 8A. When the top FET is on, the output current flows through that FET and the inductor to the output. During this time, the phase-node voltage is equal to V_{IN} . The bottom FET must re-



main off until after the top FET fully turns off. When the top FET turns off, the current then flows from ground, through the bottom FET, and through the output inductor. Dead time is the time lag between turning off the top FET and turning on the bottom FET. During the dead time, the current flows through the body diode of the bottom FET, and the phasenode voltage is approximately -1V, depending on the current levels and the FET parameters. When the bottom FET turns on, the current flows through the FET structure rather than through the body diode. During this time, the voltage is a function of the output current and the resistance of the FET.

During the dead time, the negative voltage coupled with parasitic ringing can apply a negative voltage that exceeds the maximum voltage ratings of the control IC. Trace B in Figure 2b shows the phase node when the top FET turns off. The output current flows through the body diode of the bottom FET, and the voltage drop across the FET is -0.76V. With the ringing in the circuit, the phasenode voltage can exceed -1V, a voltage applied directly to the control IC. When the bottom FET turns on, the voltage drops to approximately -0.1V (8A× 0.013Ω). Adding a Schottky diode in parallel with the bottom FET helps, but a Schottky diode is large and expensive and has little effect on the voltage. Trace C in Figure 2b shows the voltage that occurs with the addition of a large D-Pak MBRD835L Schottky diode. The diode reduces the voltage to -0.6V. With ringing, the control IC sees -0.7V.



Expanding the dead-time waveforms (a) leads to three scenarios (b): the unadorned buck regulator (Trace B), adding a Schottky diode (Trace C), and the simple solution in Figure 3 (Trace D).



The circuit in **Figure 3** is small and inexpensive and significantly reduces the phase-node voltage at the control IC. The gate-drive resistor moves from the gate to the source of the top FET. Following the current from the IC as it charges and discharges the gate capacitance of the top FET shows that moving the resistor has no effect on the circuit operation. An SOT-23 or an SOD-123 Schottky diode with a current rating of 0.5A connects to the control IC. As you can see in Trace D of **Figure 2b**, when the voltage across the FET's body diode goes to -1V, the Schottky diode clamps the voltage on the IC to approximately -0.3V. The full output current flows through the FET, and the gate-drive resistor limits the current through the Schottky diode. This solution is small and inexpensive and prevents erratic operation or damage to the power-supply control IC.

Is this the best Design Idea in this issue? Select at www.ednmag.com.

Track multisite temperatures on your PC

Clayton Grantham, National Semiconductor, Tucson, AZ

HE LOW-COST CIRCUIT in Figure 1 allows you to track four remote temperatures with thermistor sensors through the parallel port on your PC. This four-zone thermometer instrument has a temperature range of -40 to $+90^{\circ}$ C and a resolution of better than $\pm 1^{\circ}$ C. You can calibrate its accuracy to within 1°C over a 0 to 50°C span and within 3° C over a -40 to $+90^{\circ}$ C span. Thermistors are low-cost, passive, rugged components, making them a good choice for temperature sensing. The signal-conditioning hardware in Figure 1 performs a simple voltage division to partially linearize the thermistors. Temperature data in the form of thermistor voltages goes into Excel macros, and software performs a fifth-order-equation fit using calibration coefficients to convert the data into Celsius temperatures. This Design Idea focuses on the electronics in Zone 1; the other zones behave similarly. You can implement one, two, three, or all four zones without software modification.

All components have low power (quiescent current) consumption to minimize LPT1 sourcing requirements. Four LPT1 outputs at D0 (Zone 1), D2 (Zone 2), D4 (Zone 3), and D6 (Zone 4) power this application. The hardware typically requires less than 162 μ A of current per zone. Parallel-port drivers within your PC generally source at least 400 μ A. Supervisory circuit IC₁ monitors the voltage from the LPT1 port. The reset output signal of IC₁ goes back to the parallel port at S7 for software error-checking at initialization. The software ascertains that the hardware is present and that the minimum voltage from D0 of the LPT1 port is greater than approximately 4.65V. Most PCs have a 5V parallel-port interface, but a few have only 3.3V available. For 3.3V PCs, you need to scale the voltage options of the components you use.

 IC_2 is a voltage reference for both the RT_1 - R_7 voltage divider and the ADC, IC_3 . Inasmuch as IC_2 is common to the divider and the ADC, you obtain accurate ratiometric analog-to-digital conversion, and gain, offset, and thermistor-interchangeability errors are at a minimum. The low temperature coefficient of IC_2



(grades are available with lower than 10 ppm/°C) ensures that the circuit exhibits high accuracy in the environments that a portable PC encounters. You should also select R₄ and R₇ with thermal performance in mind. A 0.1% tolerance, 25ppm/°C metal-film resistor is a good choice. If you intend to use the circuit in a temperature-controlled lab, then you can use less expensive components. RT, operates in a zero-power resistance mode, in which self-heating errors are negligible. RT, and R₂ form a voltage divider that only slightly linearizes the exponential equation of the NTC thermistor's negative-resistance-versus-temperature relationship: $R_T = R_{T_0} exp[(T_0 - T)/$ $(T \times T_0)$]. The software performs further curve fitting.

 IC_3 and IC_4 (the ADC block) perform the voltage-measurement function. IC_4 , a rail-to-rail op amp, buffers the R_6 - C_3 lowpass filter. The serial output of IC_3 (D0) connects to the parallel port at S3. The converted (8 bits) voltage representing the temperature data, sampled from the divider voltage, goes to the parallel port. C0 of the parallel port controls the timing of IC_3 's clock input. C1 of the parallel port controls IC_3 's CS input; a negative-going front starts the conversion. Resistors R_1 , R_2 , and R_3 help provide the logic interface between IC_3 and the parallel port. Pulling the thermistor connections either above the PC's 5V supply level or below ground could result in damage to the circuit, the PC, or both. R_4 and R_6 provide some protection. However, to be completely safe, you should isolate the thermistors from any external voltage potential. With no thermistor connected, the temperature reading assumes the zero-voltage temperature, which is -40° C.

 IC_1 also has a manual reset that provides direct user control for external triggering. If you depress the momentary switch, S_1 , and select the "Trig" button on the user form, then the circuit performs a temperature measurement. The hardware turns off when the user form clos-



This PC-based thermometer derives its power from the parallel port and uses thermistors to sense four temperature zones.



es. The program control resides in Excel (running under Office 2000) macros that perform I/O through the LPT1 port of the PC. The program uses a free file "Input32.dll" to bit-wise-control the parallel port's digital I/O. The author of the .dll file is Jonathan Titus, editorial director of Test and Measurement World. You load Ouad-Zone.xls with its macros, connect the circuit of Figure 1 to the parallel port, and then run the ControlPanel macro. A user form (Figure 2) pops up, overlaying the spreadsheet, and connects temperature-measurement actions with

the electronics. Your possible options using the user form are single-temperature measurement, multiple-temperature measurements separated by user-defined time intervals, linked measurements that append the data to an Excel spreadsheet, and externally triggered single-temperature measurements. You can download the spreadsheet and the .dll file from the Web version of this Design Idea at www.ednmag.com.

The user form displays a single quad-





zone temperature measurement when you press the Update button on the user form. Measurement data links to the cells from columns A to G (named "data") in the spreadsheet when you press the Linked button. When you press the Loop button, the circuit samples measurement data in user-defined intervals. S₁ externally triggers measurement data if you press the Trig button. By using macros within Excel, all the graphing, analysis, and data-storage utilities common to Excel are available for familiar usage. The macros in the .xls listing contain the basic interface features for capturing the signal-conditioned thermistor-sensor signals. Within Module 1, the declaration of Input32.dll needs to include its directory path. The code for input/output of temperature data is within the userform module.

The macros also include a software-calibration routine that steps users through a temperature-calibration sequence. With the thermistor inside a calibrated oven, you right-click on the user form to initiate calibration. The "cal" spreadsheet

of **Figure 2** stores the raw calibration data. The "FitChart" chart plots this raw data and displays a fifth-order-polynomial trend-line equation. The user-form code uses the equation's coefficients to scale and display the temperatures in the user form.

Is this the best Design Idea in this issue? Select at www.ednmag.com.