design ideas

Edited by Bill Travis

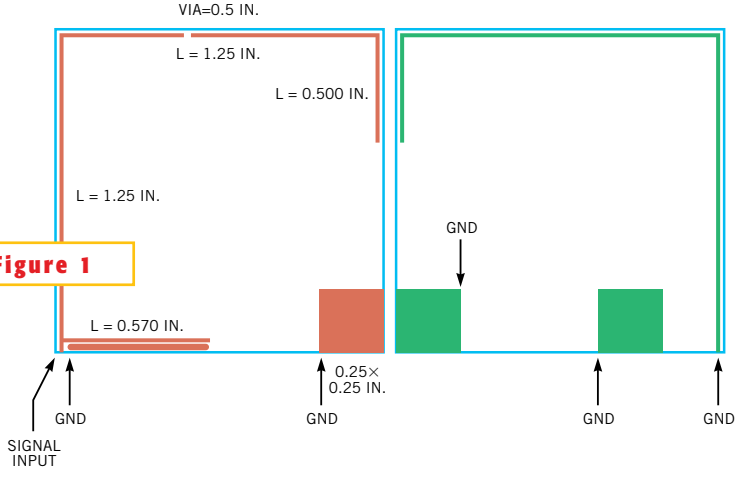
Small, 915-MHz antenna beats monopole

Dave Cuthbert and Bob Casiano, Micron Technology, Boise, ID

A 915-MHz data-acquisition project required a small antenna, but the available antennas lacked the necessary characteristics: efficiency, compactness—that is, smaller than a standard 3-in. monopole—with adequate bandwidth, and with amenability to modeling by inexpensive NEC-2 antenna software. (To learn more about NEC antenna software, go to www.nittany-scientific.com/nec.) The result of this design effort, called the "Tab" antenna for its square shape has the following characteristics:

- a square shape, 1.25 in. per side (0.1 wavelengths);
- the ability to be constructed in FR-4 pc board;
- linear polarization;
- a 2-to-1 VSWR (voltage-standing-wave-ratio) bandwidth of 46 MHz (5% bandwidth);
- the ability to be mounted parallel or perpendicular to a pc board;
- enhanced suppression of second- and third-harmonic radiation; and
- the ability to be mechanically trimmable to resonance.

Figure 1



This 915-MHz antenna measures only 1.25 in. sq yet outperforms a standard 3-in. monopole.

The Tab antenna is a folded monopole that you miniaturize by forming it into an inverted L with a downward bend at the end (**Figure 1**). You can solder it perpendicular to a pc board or build it as part of a pc board and place it at a corner. The folded section transforms the 12.5Ω radiation resistance to 50Ω and provides second-harmonic suppression. Third-harmonic suppression comes from an open stub near the base of the antenna. Detailed NEC-2 modeling explores the sensitivity to changes in the dimensions and optimized harmonic suppression. Because NEC models wire antennas in a vacuum and the Tab antenna is built on FR-4, you must incorporate the dielectric properties of the dielectric between the antenna elements into the model.

To incorporate the dielectric properties, you add periodic RC loads between the transmission-line elements. The loads are the small boxes in **Figure 2,** and each load comprises a 30Ω resistor in series with a 78-fF capacitor. The capacitance of each RC load is equal to the difference between the transmission-line capacitances calculated with FR-4 as the dielectric and with vacuum as the dielectric. You calculate the resistance of each RC load using the published FR-4 loss tangent of 0.02. The following formulas determine the approximate RC values for the transmission-line loads:

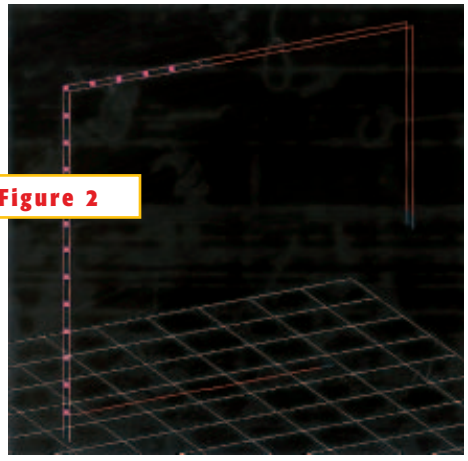
$$Z_0 = \frac{276}{\sqrt{Er}} \log_{10}\left(\frac{2D}{d}\right),$$

where D is the conductor spacing and d is the conductor diameter.

$$C = \frac{t_{PROP\_VACUUM}\sqrt{Er}}{Z_0}.$$

$$R = \frac{LOSS\ TANGENT}{2\pi fC}.$$

Figure 2



The square grids represent loads of 30Ω in series with 78-fF capacitors.

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You calculate the RC load parameters for 915 MHz and place them every 0.1 in. (approximately 5°) along the line. You use the following parameters in the calculations:

- D=62 mils,
- d=20 mils,
- effective Er (dielectric constant) of FR-4=3,
- loss tangent=0.02, and
- t_{PROP_VACUUM}=85 psec/in.

Table 1 shows the effective parameters in air and in the FR-4 medium. You use iterative modeling to determine the antenna dimensions with the following design parameters: The first vertical section and the horizontal section must be of equal lengths, the feedpoint impedance target is 50Ω, and the resonant frequency is 915 MHz. You meet these design criteria with a simulated antenna height of 1.3 in. and a total element length of 3.3 in. The actual element length of 3 in. stems from dielectric loading. You also shorten the actual antenna height to 1.25 in. to compensate for the impedance increase that the dielectric loss causes. Note that the modified NEC model accounts only for the dielectric between the antenna elements.

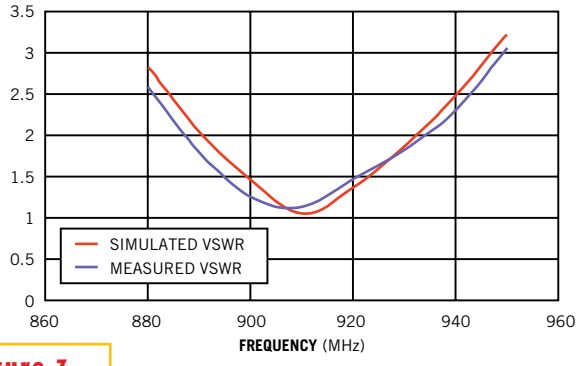


Figure 3

The simulated VSWR figures of the Tab antenna agree closely with the measured results.

The folded section, functioning as a shorted 180° transmission line at 1830 MHz, provides second-harmonic suppression. And, although the optimum point for the short circuit is 1.75 in. from the feedpoint, you can achieve second-harmonic suppression of 25 dB by placing the short within 10% of this point. The location of the short has little effect at 915 MHz. An open transmission line at the feedpoint that is 90° at 2745 MHz provides third-harmonic suppression. This line creates a near-short circuit at 2745 MHz and provides harmonic suppression of 15 dB when you trim it to within 5% of the optimum length. **Table 2** compares the simulated harmonic suppression of the Tab antenna with that of a quarter-wavelength monopole with a 50Ω source driving both antennas.

The Tab antenna has 20-mil-wide traces on opposite sides of 62-mil FR-4 and mounting pads at three locations to allow soldering the antenna securely to a larger board. You tune the antenna by trimming the open transmission line to provide an impedance minimum at 2745 MHz and then trimming the antenna elements to resonance at 915 MHz. **Figure 3** shows that the simulated 2-to-1 VSWR bandwidth is 41 MHz, whereas the measured bandwidth is 46 MHz. Note that the required operating band is only 902 to 928 MHz. The increased measured bandwidth arises from dielectric losses and indicates that the radiation efficiency is approximately 90%. The large bandwidth of the Tab antenna results in low sensitivity to environmental detuning. This design effort yields an antenna only 40% as tall as a standard quarter-wavelength monopole, yet having excellent radiation efficiency, extended bandwidth, and superior harmonic suppression.□

TABLE 1–ANTENNA PARAMETERS IN AIR AND IN FR-4 PC-BOARD MATERIAL

Dielectric	Er	Z_0 (Ω)	C (fF)	R
Air	1	219	39/0.1 in.	Infinite
FR-4	3	126	117/0.1 in.	30Ω
RC load			78	30Ω

TABLE 2–HARMONIC SUPPRESSION OF QUARTER-WAVELENGTH MONOPOLE AND TAB ANTENNA

Frequency (MHz)	Quarter-wavelength monopole (dB)	Tab antenna (dB)
1830	7	25
2745	1	15

Digital signal controls sine generator

Simon Bramble, Maxim Integrated Products, UK

THE CIRCUIT of **Figure 1** produces an accurate, variable-frequency sine wave for use as a general-purpose reference signal. It includes an eighth-order elliptic, switched-capacitor lowpass filter, IC_3, which uses a 100-kHz square-wave clock signal that microcontroller IC_2 generates. (Any other convenient square-wave source is also acceptable.) The microcontroller receives its clock signal from a 10-MHz oscillator module. A voltage supervisor,

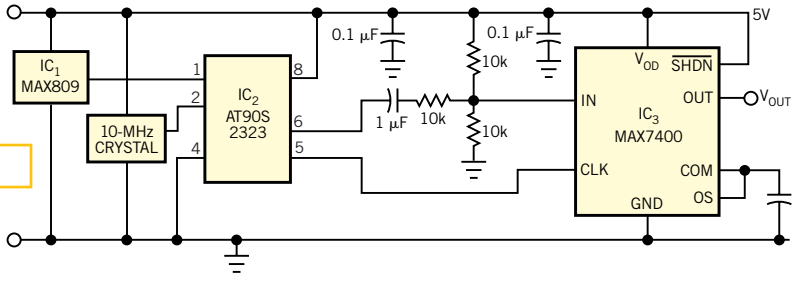


Figure 1

By removing harmonics from a square wave, this circuit generates an accurate and adjustable sine-wave output.

LISTING 1—ASSEMBLY CODE FOR SINE GENERATOR

```
;*****************************************************************************
; PORT DEFINITIONS
;*****************************************************************************

.equ   SREG   =$3f
.equ   SPL    =$3d
.equ   GIMSK  =$3b
.equ   GIFR   =$3a
.equ   TIMSK  =$39
.equ   TIFR   =$38
.equ   MCUCR  =$35
.equ   MCUSR  =$34
.equ   TCCR0  =$33
.equ   TCNT0  =$32
.equ   WDTCR  =$21
.equ   EEAR   =$1e
.equ   EEARL  =$1e
.equ   EEDR   =$1d
.equ   EECR   =$1c
.equ   PORTB  =$18
.equ   DDRB   =$17
.equ   PINB   =$16

.equ    RAMEND  =$DF    ;Last On-Chip SRAM Location
.equ   XRAMEND =$DF
.equ   E2END  =$7F
.equ   FLASHEND=$1FF

;*****************************************************************************
; REGISTER DEFINITIONS
;*****************************************************************************

.def   junk        =r16              ; junk register
.def   junk1       =r17              ; another junk reg (!)
.def   count       =r18

;*****************************************************************************
; MAIN CODE

;*********************************************************************
.cseg
.org   0
       rjmp   reset                  ; executed on RESET
.org   2
       rjmp   Int_T0                       ; executed on Timer 0 overflow
start:
       ldi    junk, 0xD8             ; preload counter with 216d
       out    TCNT0, junk            ; to give overflow after 5us

count_loop:
       cpi    count, 0x64            ; count to 100
       brne   count_loop

       ldi    junk1, 0b00000001
       in     junk, PORTB            ; read in Port B
       eor    junk, junk1
       out    PORTB, junk            ; flip bit 0 (CLK2 output)

       clr    count
       rjmp   start
```

```
;*****************************************************************************
; SUBROUTINES
;*****************************************************************************

;********************** MICRO INITIALISATION ROUTINE *************************
reset:                               ; port definitions and reset
; Initialise Stack:
       ldi    junk, low(RAMEND)      ;
       out    SPL, junk              ; define top of Stack

; Initialise Timer 0
       ldi    junk, 0b00000000       ; stop counter
       out    TCCR0, junk

; Initialise ports:
       ser    junk
       out    DDRB,junk              ; set all ports to outputs
       clr    junk
       out    PORTB, junk            ; clear outputs

; Initialise Interrupts:
       ldi    junk, 0b10000000       ; enable Timer 0
       out    GIMSK, junk            ; set Global Interrupt bit
       ldi    junk, 0b00000010
       out    TIMSK, junk            ; overflow Interrupt

       clr    count

       ldi    junk, 0b00000001       ; Start Counter, Prescaler = 1
       out    TCCR0, junk

       rjmp   start

;*************** TIMER/COUNTER OVERFLOW INTERRUPT ROUTINE *********************



Int_T0:                                     ; service here on interrupt

       ldi    junk, 0xD8             ; reset clock
       out    TCNT0, junk            ; to give overflow after 5us

       ldi    junk1, 0b00000010
       in     junk, PORTB            ; read in Port B
       eor    junk, junk1
       out    PORTB, junk            ; flip bit 1 (CLK1 output)

       inc    count
       reti

;*****************************************************************************

end:
       rjmp   end

;*****************************************************************************
; END OF FILE
;*****************************************************************************
```

IC_1, ensures correct operation in the event of a power failure. IC_3 sets the filter's cutoff frequency at one-hundredth the clock frequency.

The eighth-order elliptic filter's sharp roll-off sharply reduces the harmonic amplitudes in a 1-kHz square-wave input, thereby producing a nearly perfect 1-kHz sine wave at its output. Using divider-chain logic or a processor, you can then create a digitally adjustable sine-wave source by adjusting the clock and input frequencies and maintain a ratio of 100-to-1 between them. To prevent clipping at the positive and negative peaks, attenuate the input signal and superimpose it on a dc level of $V_{CC}/2$. The result for a 5V input is a 2.25V peak-to-peak output. **Listing 1** shows the assembly code for the microcontroller this application uses. You can download the code from the Web version of this Design Idea at www.edn.com.□

Transmitter accurately transfers voltage input

Clayton Grantham, National Semiconductor, Tucson, AZ

When you connect remote sensors to a central process controller, a simple, robust, and commonly used interface is the 4- to 20-mA loop. The advantages of this current loop include the simplicity of just two twisted wires that share both power and signal, the loop's high noise immunity in harsh environments, and the de facto loop standard within the process-control industry. Within this interface scheme, a typical 24V battery

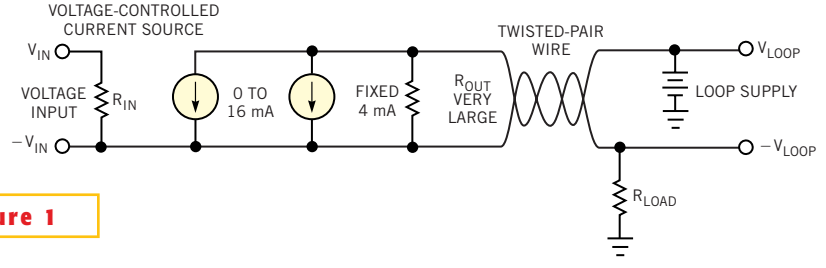
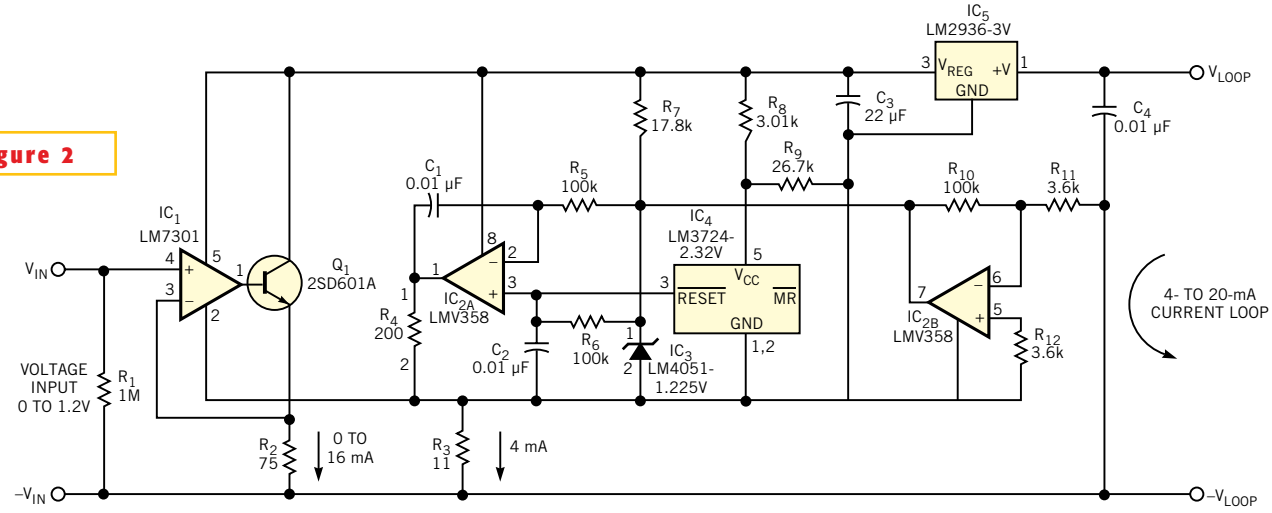


Figure 1

This ideal 4- to 20-mA current transmitter has one voltage-controlled current source and one fixed current source.

Figure 2



This circuit transforms a 0 to 1.2V input voltage to a 4- to 20-mA output range.

(loop power source) connects through a twisted-wire pair to a transconductance amplifier (voltage-to-current converter) that converts a sensor's—for example, a pressure transducer's—output voltage into a current that then gets transmitted back through the twisted-wire pair to a receiver (load resistor) at the process-control computer. An important criterion in this interface is that the current transfer of sensor information must be accurate. **Figure 1** shows the transmitter with one voltage-controlled current source and one fixed-current source.

The fixed-current source is 4 mA, a current that constitutes the power source for the transmitter and the sensor electronics. This fixed current source must have an output impedance greater than 20 MΩ to keep the loop current independent of loop-supply variations. Similarly, current needs to be independent of temperature—that is, greater than 100 ppm/°C—because the transmitter and the sensor can be in harsh environments. The voltage-controlled current source has the same requirements as the fixed-current source and needs to convert the input voltage signal linearly into a 0- to 16-mA current. Thus, it produces an ideal transconductance as the two-port network representation of a voltage-controlled current source. The total loop-current equation is: Loop current=4 mA+(gm)V_{IN} (for V_{IN}=1.2V, gm=13.3 mmho).

The transconductance circuit in **Figure 2** allows you to transmit current (4- to 20-mA loop) with less than 1% total error from −40 to +85°C and over a 3.2 to 40V loop-voltage range. Many IC realizations of a current transmitter have existed for years, but none operates at the loop voltage of 3.2V. Also, these ICs are becoming sensor-specific, whereas you can modify and optimize the circuit in **Figure 2** for any sensor electronics or loop-current variation (for example, a 1 to 5A loop) at low loop voltage. The total loop current is as follows: Loop current=$1.225V(R_{11}/R_{10})/R_3+V_{IN}/R_2$. The circuit discussion starts with the realization of the fixed current source, I_S. The fixed 4-mA current all flows through R_3. The servo circuitry, including IC_2 and IC_3, senses the 44-mV voltage drop across R_3 and keeps it fixed. Note that the ground current of all ICs also flows through R_3; thus, the 4-mA fixed-current setting includes ground-current errors. The dual op amp, IC_2, is both an inverting gain stage and an integrator stage. R_{10} and R_{11} set the inverting gain to −27.8V/V. The noninverting-integrator components C_1, C_2, R_5, and R_6 provide a comparison of the −44 mV across R_3 (gained up to 1.225V) to the shunt-reference voltage of IC_3. The output of IC_{2A} adjusts the sum of the current though R_4 and any ground current from IC_2, IC_3, and IC_4 to a value of 4 mA. IC_4 acts as an analog power-on-reset circuit that holds off the start-up of servo action until all the ICs have sufficient supply voltage. With the divider ratio of R_8 and R_9 and the 2.32V option of IC_4, the start-up voltage equates to: $V_{START-UP}=2.32V(R_8+R_9)/R_9=2.7V$.

This start-up value is higher than the rated supplies of IC_1 and IC_2 and lower than IC_5's regulated output of 3V. R_4 level-shifts the output of IC_{2A} up from zero. R_7 biases IC_3 into its specification range to guarantee 0.1% tolerance and 50-ppm/°C temperature coefficient over the −40 to +85°C range. The circuit discussion continues with the realization of the voltage-controlled current-source. IC_1, Q_1, and R_2 are configured as a voltage-to-current converter. Thus, for a full-scale range of 20 mA, 16 mA comes from the voltage-to-current converter. With the maximum V_{IN} at 1.2V, R_2 must be 75Ω to produce 16 mA. IC_1 must have a common- mode input range that goes beyond its negative supply (less than −44 mV). R_1 is optional and prevents an open circuit on IC_1's input. You can remove R_1, depending on the output impedance of any input-sensor electronics. Note that R_1 directly introduces an error in the full-scale loop-current.

At the heart of the circuit discussion is the realization of an output impedance, R_{OUT}, greater than 20 MΩ in **Figure 1**. The low-dropout regulator, IC_5, accomplishes this task by subregulating the supply to IC_1 and IC_2. The good line regulation of IC_5 keeps the 3V output within 30 mV over the input range of 3.2 to 40V. Additionally, IC_5 requires as little as 200 mV of overhead to properly regulate, and it

can withstand more than 40V. This current-transmitter circuit is useful for both low-loop-voltage designs, and it's backward-compatible with higher loop-voltage implementations. Furthermore, IC_5 has reverse-supply and surge protection. Therefore, this circuit does not require an additional diode within the loop, a common need with other ICs to prevent accidental reverse-wiring damage. The TO-252-package option simplifies the thermal-design considerations. With a 1-in.-sq-area pad for heat sinking, the worst-case power dissipation calculation would keep the junction temperature within its rated 150°C: $T_J = 85°C + (20\ mA)(40V) \times 50°C/W = 125°C$.

You could increase the V_{IN} range of the current-transmitter by scaling R_2, as long as you don't violate the common-mode input range of IC_1. IC_1's V_{CM} includes its positive rail. So, to obtain a higher V_{CM}, you can increase the voltage option of IC_5. For example, use the LM2936-5V and R_2 equal to 312.5Ω for a 0 to 5V input range. This configuration would also require that the loop supply be at least 5.2V. Note that any sensor and other electronics can and should use the 3V subrails that IC_5 creates as long as the current they demand does not exceed 3 mA. The 4-mA fixed-current circuitry adjusts for the current demand. **Figure 3** shows the total error on prototype units over temperature.

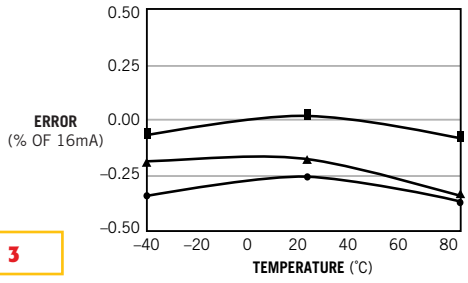


Figure 3

On three prototype circuits of Figure 2, the total error is well below 1% over temperature at 3.2V loop voltage.

The total error includes the offset (4-mA) and full-scale (20-mA) effects on the ideal loop current. The tolerances of R_2, R_3, R_7, and R_8 should be within 0.1% with 50-ppm/°C temperature coefficients. With IC_5 subregulating the rails of IC_1, IC_2, and IC_3, the power-supply-rejection-ratio error of these ICs does not generate a significant error. In like manner, IC_2's CMRR (common-mode-rejection-ratio) error does not generate a significant error. IC_3's CMRR error and Q_1's base-current error both influence the best nonlinearity attainable: less than 0.01%. IC_2's offset error is in series with the 44-mV voltage across R_3, producing an offset error of 4 mA. Adjust R_3 if you need to null this error. Adjust R_2 to fine-tune the full-scale range of 20 mA. The op amp's offset-temperature-coefficient error is small compared with the Δ1% temperature-range budget.□

Absolute-value circuit delivers high bandwidth

Ron Mancini, Texas Instruments, Bushnell, FL

Most absolute-value circuits have limited bandwidth and high component count, and they require several matched resistors. The circuit in **Figure 1** uses three fewer components than most absolute-value circuits require, and only two of the resistors must have 1% tolerance to obtain 1% accuracy. This circuit's output voltage is an accurate representation of the absolute value of the input signal, and it is accurate for input signals containing frequencies as high as 10 MHz. Another advantage of this circuit is that it has a positive-voltage output, thus saving an analog inverter in most applications. When the input voltage is positive, the negative output voltage of IC_1 cuts off the diode, thereby preventing signal propagation through IC_1. Virtually no signal propagates through R_2, because the resistor connects to ac ground through the output of IC_2. The only signal path is through R_3 to buffer IC_2, and the output of the buffer is a positive voltage. When the input voltage is negative, the positive output voltage of IC_1 forward-biases the diode, thus providing an ac short circuit for R_3 to ground. IC_2 is within IC_1's feedback loop, so the output voltage is positive because of IC_1's configuration as an inverting op amp.

This design uses a dual op amp to minimize parts count. Two op amps in a feedback loop tend to be unstable. Select an op amp that has sufficient phase margin to prevent oscillation when the input voltage is negative. The circuit's dynamic range is from the op amp's input offset voltage to the maximum output voltage. This dynamic range is from 1 mV to 4.1V for the TLC072 with ±5V power supplies. The excellent bandwidth performance results from combining the high-frequency TLC072 op amp with a fast Schottky-barrier diode. You can use higher frequency op amps to obtain better bandwidth results, but you must take care in the op-amp selection to avoid oscillation or reduced dynamic range.□

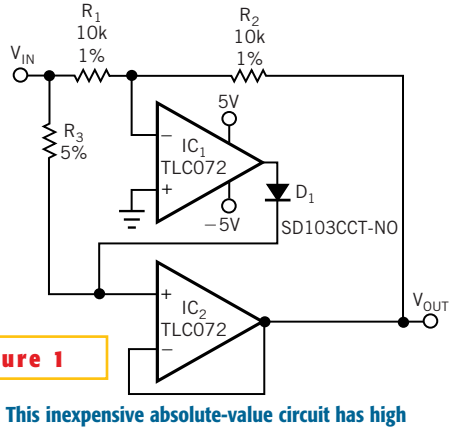


Figure 1

This inexpensive absolute-value circuit has high bandwidth.