Edited by Bill Travis

Microcontroller directs supply sequencing and control

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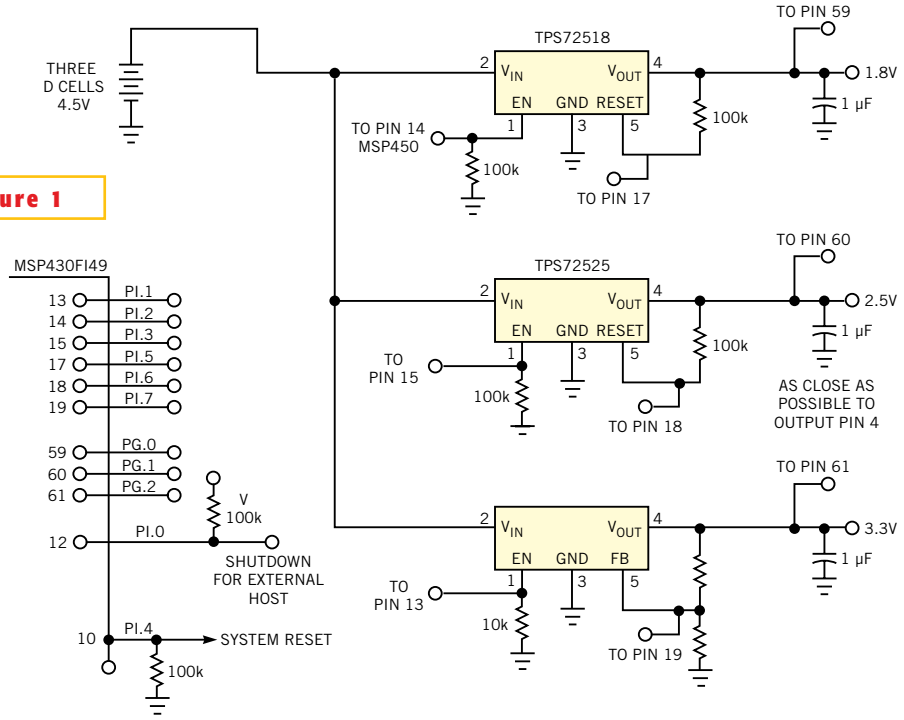
With the proliferation of dual-voltage architectures and multiprocessor boards, even simple applications can require several processor voltage rails. With each processor having its own power-up and -down requirements, power-rail sequencing and control can become a complex task. The challenge for power-supply designers is to consider each processor's timing and voltage requirements and assimilate these into a total system, ensuring that the final design meets the requirements of all processors.

Failure to properly power processors can lead to problems that range from the fairly benign, such as a reduction in MTBF, to the catastrophic, such as latch-up. Given the variety of available processors and the application challenges you expect when developing a power-sequencing and -control scheme, use of a microcontroller is desirable because of its programmability. The MSP430 is a good fit for such an application (**Figure 1**). The high-performance, low-cost 16-bit RISC processor has several high-quality analog peripherals and a JTAG interface.

Figure 1



An ultra-low-power microcontroller controls a system's power-supply sequencing.

Controlling power supplies that have enable pins, such as those on most "brick" dc/dc converters and low-dropout regulators, is simply a matter of using a GPIO (general-purpose I/O) line. If the power supply has no enable function, an inline switch, normally a MOSFET, can control the power supply, either with a GPIO or PWM signal. The circuit in **Figure 1** uses the TPS725xx family of low-dropout regulators to provide 3.3, 2.5, and 1.8V from an input dc source. These regulators have an enable pin and a reset function. You can easily expand this circuit to any number of voltage rails. The MSP430 monitors a control variable to determine when to activate each rail. For power-sequencing applications, the two most commonly controlled variables are time and voltage. When time is the control variable, the controller enables the first rail. At a specific time thereafter, it enables the next rail. Some time after that, it enables the next rail, and so on until it has enabled all rails.

The MSP430 provides the timing-sequence and the -control signals to turn on the power supplies. If voltage is the control variable, then the controller activates the first voltage rail and monitors its rise via an ADC. When the first voltage rail reaches a specific voltage level, the controller enables the next voltage rail and monitors its rise until it reaches

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a specified voltage level. At this point, the controller enables the next voltage rail and monitors it. This process continues until the controller has enabled all voltage rails. When using voltage as the control variable, the controller can use either a GPIO or a PWM signal as the enable signal, depending on whether the design requires rail tracking. You can also use a combination of voltage and timing control.

In **Figure 1**, each low-dropout regulator connects to two MSP430 lines—one for enabling and the other for monitoring. When time is the control variable, the monitoring takes place via Port 1 (GPIO); when voltage is the control variable the monitoring occurs via Port 6 (ADC). The MSP430 also provides a system reset and has an input for power-down. The code is fairly simple and does not require much programming experience. When time is the control variable, the first thing to do is initialize the MSP430 and setup the port and timer; this operation takes five lines of code (see **Listing 1**, which is available with the Web version of this Design Idea at www.edn.com). The next operation is to load the capture-and-compare register zero (CCR0) with the first timing interval and start the timer. When CCR0's value is equal to the timer's value, the first voltage rail becomes enabled. CCR0 is then loaded with the next time interval, and the timer resets and restarts. When CCR0 is equal to the timer value, the second voltage rail becomes enabled. This operation repeats until all rails become enabled.

Once all rails are enabled, a delay loop enters the picture to ensure that the reset pins on the low-dropout regulators have time to come up. The TPS725xx family has an open-drain, 100-msec reset function. Once the delay is complete, the MSP430 checks each regulator's reset line to ensure that all rails are up. If all rails are up, the MSP430 issues a system reset. When voltage is the control variable, only five lines of code are necessary to initialize the MSP430 (**Listing 2**, which is available with the Web version of this Design Idea at www.edn.com). The next operation is to load registers R9, R10, and R11 with values that represent 3.3, 2.5, and 1.8V, based on a 3V ADC reference. The first rail becomes enabled, and its output voltage undergoes monitoring until it is within specification, at which point the next rail is enabled and monitored. This operation repeats until all three rails become enabled. Once all the rails are enabled, the delay loop for regulator reset activates, and the system reset occurs.

Once the MSP430 turns on all the voltage rails and applies the system reset, it enters the monitor mode. It continually checks the low-dropout regulator's output voltage, via the reset or output pins, depending on whether time or voltage is the control variable. If a fault occurs, the MSP430 enters an error routine. The most obvious fault would be the loss of a voltage rail, but other faults, such as overvoltage and undervoltage, are also amenable to monitoring. The actions that the error routine takes depend on the application. The simplest actions would be to power down all rails, but programmability gives you complete control. One final function is the powering down of the voltage rails. An external signal, likely from the main processor, signals the MSP430 to power down the processor rails. In this example the power-down sequencing is just the opposite of the power-up sequence, but you can define any sequence. One addition to the power-down sequence could be to turn on dummy loads to discharge the output filter capacitors. This design uses the TPS-725xx low-dropout regulators because they offer fast transient response and stability with any output capacitor. However, some applications may require large output capacitors to maintain stability and transient response. In these cases, the ability to discharge these filter capacitors improves MTBF. □

Circuit provides leading-edge blanking

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In isolated switch-mode power supplies using peak-current-mode control, generally the current-sense resistor senses the current on the primary side of the power converter. **Figure 1** shows a typical circuit, in which R_2 is the current-sense resistor that monitors the current. The current-sense signal goes to the input of the PWM comparator—in this case, the PWM comparator's input (I_{SENSE}) of the controller IC. R_3 and C_1 provide an RC delay in an attempt to remove some of the leading-edge spikes on the current-sense signal. Sometimes, the RC delay circuit is insufficient for removing the false noise signals at the input of the PWM comparator. This Design Idea shows how to suppress the false triggering signals caused by parasitic LC (inductance and capacitance), causing LC tanking and false-peak current triggering to the peak-current-limit comparator.

The RC delay circuit in **Figure 1** works for most applications in suppressing voltage spikes that may falsely trip the peak-limit-current comparator. However, some applications require a leading-edge blanking circuit to suppress false triggering. **Figure 2** shows the typical current-sense signal that appears across R_2. The leading-edge spike at time T_1 occurs

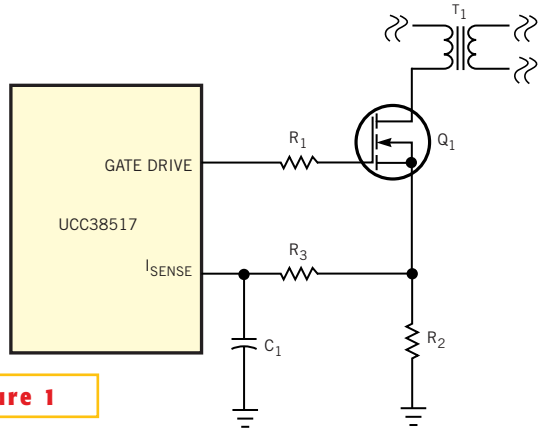

Figure 1

In this classic PWM-controller configuration, R_2 is the sending resistor for the output current.

when the gate drive switches from low to high and the parasitic capacitance from the gate to the source of Q_1 is charging. Depending on the values of R_1 and R_2, a large-enough leading-edge voltage spike could falsely trigger the PWM comparator at the I_{SENSE} pin. This problem is common in isolated dc/dc power converters. To remove false triggering from the PWM comparator, it is desirable to blank out the leading-edge spikes that appear on the current-sense signal. You can suppress these leading-edge spikes by adding four additional components to the circuit in **Figure 1**. **Figure 3** shows the extra circuitry necessary to provide leading-edge blanking. The gate drive from the PWM circuit activates the leading-edge blanking circuit. Transistor Q_2 suppresses the leading-edge current-signal spike. Components R_4, C_2, and R_5 set up the amount of time the leading edge of the current-sense signal is suppressed from the PWM comparator.

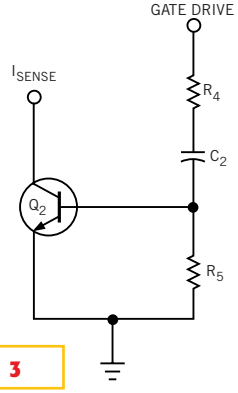

Figure 3

Transistor Q_2 suppresses (blanks) leading-edge spikes that could falsely trigger a PWM comparator.

Selecting the components for the leading-edge blanking circuit is simple. You select Q_2 with sufficiently low saturation voltage, V_{SAT}, to suppress the leading edge of the current-sense signal. You select R_4 and R_5 to drive transistor Q_2 into saturation. You then select C_2 to set up the timing for the circuit. To select transistor Q_2, the maximum collector-to-emitter voltage, V_{CE}, must be less than the gate-drive voltage. The transistor saturation voltage, V_{SAT}, must be low enough to suppress the voltage spike at the PWM comparator's input. For most applications, you can get away with using a 2N2222 transistor. You must select R_3 to provide some current-limiting protection for transistor Q_2. R_4 must supply sufficient base drive, I_B, current to Q_2. You select R_5 such that its current is 10% of the base-drive current. You choose the value of C_2 to keep transistor Q_2 saturated for two RC time constants. You can use the following equations to calculate the resistor and capacitor sizes:

$$R_4 = \frac{V_{GATE} - V_{BE}}{I_B},$$

$$R_5 = \frac{V_{GATE} - V_{BE}}{I_B/10}$$

and

$$C_2 = \frac{T_{BLANK}}{2(R_4 + R_5)},$$

where V_{GATE} is the maximum gate-drive voltage of the PWM comparator, and T_{BLANK} is the amount of leading-edge blanking time required.

Another power-supply design has current-sense spikes so large that the module will not regulate. This design requires the implementation of the leading-edge blanking circuit in **Figure 2**. The design, a 200-kHz flyback converter, requires a leading-edge blanking time, T_{BLANK}, time of 200 nsec. The leading-edge blanking circuit requires a maximum base current, I_B, of 42 mA. The I_B specifications require R_4 to be 275Ω and R_5 to be 200Ω. To attain the 200-nsec delay, C_2 needs to be approximately 390 pF. Q_2, a 2N2222 current-suppression transistor, requires a current-limiting resistor, R_3, of roughly 1 kΩ. The PWM comparator's input, I_{SENSE}, has a peak threshold of 1.5V. **Figure 4** shows the current-sense signal of the flyback converter before the addition of the suppression circuit. The waveform shows that leading-edge spikes turn off switch Q_1.

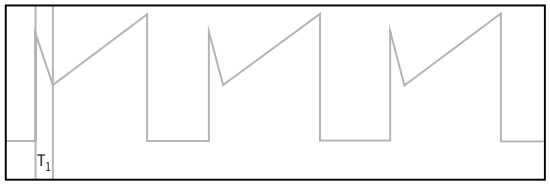

Figure 2

The leading-edge spike in this waveform could falsely trigger the PWM comparator in Figure 1.

After you add the leading-edge blanking circuit to the power module, it clamps the leading-edge voltage spikes and allows the converter to operate correctly. **Figure 5** shows the current-sense waveform. Leading-edge noise spikes on the current-sense signal can cause instabilities in peak-current-mode-control power-supply designs. Usually, you can resolve these issues with an RC filter at the input of the peak-current-limit comparator. In some instances, the noise disturbance caused by parasitic capacitance and gate-drive current can cause the PWM comparator to trip falsely. In these instances, the supply requires a leading-edge blanking circuit similar to this one.□

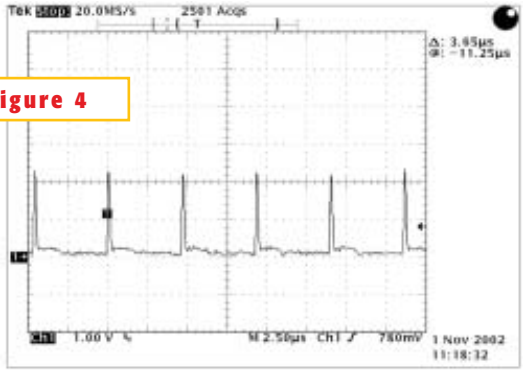

Figure 4

Without leading-edge suppression, the spikes turn off Q_1 in Figure 1.

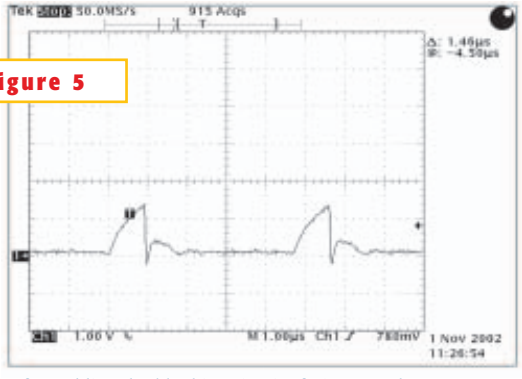

Figure 5

After adding the blanking circuit of Figure 3, the converter works normally.

MOSFETs reduce crosstalk effects on analog switches

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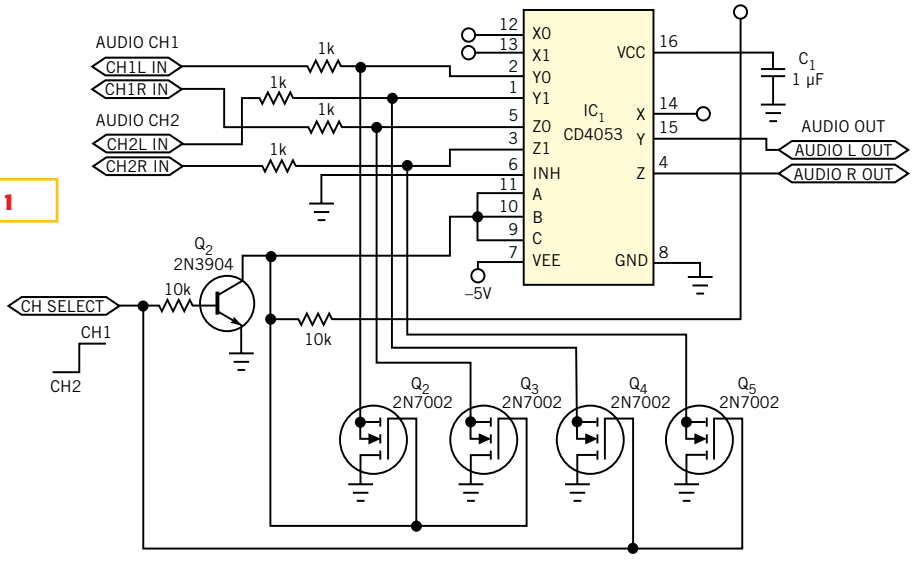
Some cost-effective analog multiplexer/demultiplexer ICs, such as the CD4053 and CD4066, find frequent use as signal distributors. These digitally controlled analog switches have low on-resistance. However, with all channels in the same package, crosstalk can be annoying and unavoidable.

Figure 1



By using a few low-cost MOSFETs, you can drastically reduce crosstalk effects in an analog multiplexer.

Figure 1 provides a cost-effective and viable method of solving this problem. By simply adding some n-channel MOSFETs, such as the 2N7002 or 2N7000, the crosstalk effect becomes negligible. When the Channel Select signal is high, the CD4053's input pins A, B, and C assume a level of nearly 0V. This operation selects Channel 1. Therefore, the Y output connects to Y0 and Z to Z0. Meanwhile, the Channel Select signal turns on Q_4 and Q_5, thereby drastically attenuating the Channel 2 signal at Y1 and Z1. The crosstalk effect simultaneously decreases. When the Channel Select signal is set low, Y=Y1 and Z=Z1, and Q_2 and Q_3 turn on to attenuate the crosstalk effect. For the 2N7002, the $R_{DS(ON)}$ resistance is several ohms; therefore, the crosstalk decreases by more than 40 dB. Add to that the analog switch's internal rejection ratio, and the total crosstalk rejection could be as high as 80 dB.□

Grounded resistor tunes oscillator

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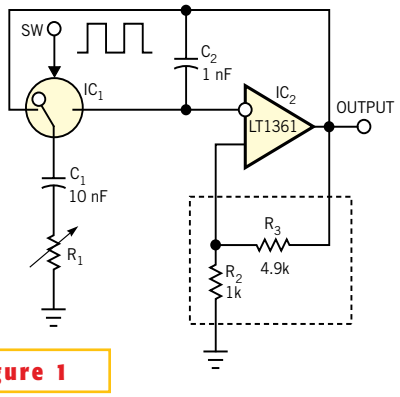
To vary the frequency of any sine-wave oscillator, you should use a pair of ganged variable resistors, and you should thoroughly match their characteristics over the entire variation range to satisfy the oscillator's balancing conditions. This restriction leads to problems in the tuning range and high cost, thereby limiting the range of applications. The sine-wave oscillator in **Figure 1** is free of the cited disadvantage. You can tune it over a wide frequency range using only variable resistor R_1. The oscillator requires no balancing, so no matching problems arise. The variable resistor connects to ground, an advantageous fact in many applications. Like most classic sine-wave RC oscillators, the implementation comprises an operational amplifier, IC_2, with two feedback loops. One loop is a frequency-independent, positive-feedback loop using two fixed resistors, R_2 and R_3, in this example. The other loop is frequency-dependent. This loop uses capacitors C_1 and C_2; variable resistor R_1; and a single-pole, double-throw analog switch, IC_1, driven by a periodic sequence of square-wave pulses applied to the SW input.

Figure 1



In this sine-wave oscillator, the output frequency is dependent only on the value of the grounded resistor R_1.

Assuming a switching frequency, $F_S=1/T$, much higher than the oscillation frequency and assuming that the pulse width, τ, is half the switching period ($\tau=0.5T$), the approximate voltage trans-

fer function of the frequency-dependent feedback loop is:

$$H(s)=\frac{s^2+s\omega_0 d_1+\omega_0^2}{s^2+s\omega_0 d_0+\omega_0^2},$$

where $\omega_0=1/2R\sqrt{C_1C_2}$ is the oscillation frequency, $d_0=\sqrt{C_1/C_2}+2\sqrt{C_2/C_1}$, and $d_1=2\sqrt{C_2/C_1}$. Using this function and assuming the transfer coefficient of the positive-feedback circuit to be $\gamma=R_2/(R_2+R_3)$, you obtain the oscillation condition in the form $\gamma>d_1/d_2=2\sqrt{C_2/C_1}/(2\sqrt{C_2/C_1}+\sqrt{C_1/C_2})$. The oscillation condition does not depend on R_1. It thus becomes obvious that controlling grounded resistor R_1 results only in the variation of the oscillation frequency and does not affect the condition for oscillation. This situation means that you can tune this oscillator over a wide range of frequencies, preserving the output waveform.

PSpice simulations prove the possibility of tuning the oscillation frequency over three decades (20 Hz to 20 kHz) by varying R_1 from 1.2 MΩ to 1.2 kΩ. This design uses an LT1361 (www.linear.com) for IC$_2$, $R_2=1$ kΩ, $R_3=4.9$ kΩ, $C_1=10$ nF, $C_2=1$ nF, and $F_S=500$ kHz. The output-voltage amplitude is 3.2 to 3.3V. The total harmonic distortion in the 0- to 100-kHz band does not exceed 3%. It's useful to note that, because the oscillation frequency is proportional to the conductance of the variable resistor ($G_1=1/R_1$), you can use the oscillator as a linear, wide-band conductance-to-frequency or resistance-to-period converter.□

Obtain higher voltage from a buck regulator

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Several semiconductor vendors' current-mode buck controllers have input-voltage ranges of 30 to 36V but have output-voltage ranges from the reference voltage to approximately 6V. This output-voltage constraint arises from the common-mode-voltage limitation of the current-sense amplifier. In real-world applications, the power-supply designer must be able to generate high output voltage for printers, servers, routers, networking, and test equipment. Using a conventional buck regulator to generate higher voltages is a challenge. The circuit in **Figure 1** meets

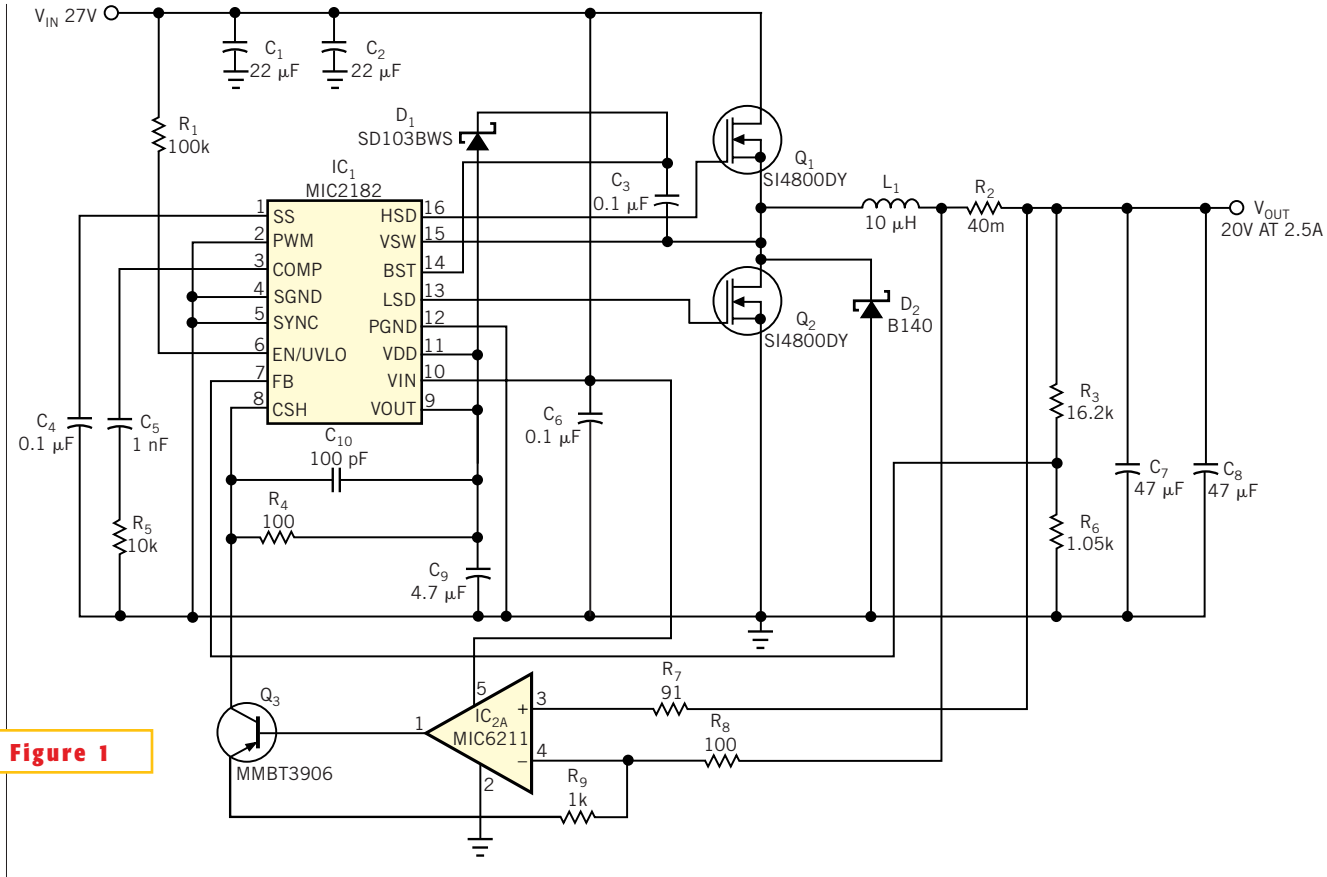

Figure 1

You can generate 20V output using a standard, current-mode buck regulator.

the challenge by using an external op amp, a small-signal pnp transistor, and a low-output-voltage buck regulator to deliver 20V output voltage from a 27V input supply for load currents as high as 2.5A. You can easily program the circuit to provide higher load currents by merely lowering the sense resistor, R_2. IC_1, the controller in **Figure 1** is the MIC2182, and IC_2, the operational amplifier, is the MIC6211. Resistors R_3 and R_6 program the output voltage as follows: $V_{OUT}=20V=V_{FB}(1+R_3/R_6)$.

CSH (Pin 8) and VOUT (Pin 9) of the buck controller normally connect across the sense resistor, R_2, for output voltages as high as 6V. The controller asserts current limit when it senses approximately 100 mV across these two pins. In the case of $V_{OUT}=20V$, the operational amplifier and Q_3 level-shift the voltage drop across R_2 from 20V down to 5V, which is within the input common-mode range of the internal current-sense amplifier of the buck regulator. You can readily understand the circuit operation by assuming a voltage drop of 40 mV across R_2 for a load current of 1A. The current through R_8 is 400 µA ((20.04−20)/100), which is also the current through R_9 and R_4 (via Q_3). This current generates a voltage drop of 40 mV across R_4 (400 µA×100Ω). The controller's VOUT pin connects to the internal 5V regulator (VDD) and R_4; the other side of R_4 connects to the CSH pin. The voltage on the VOUT pin is 5V, and the voltage on the CSH pin is 5.04V. The voltage difference between these two pins is exactly the voltage drop across R_2. The simple circuit in **Figure 1** allows you to achieve greater than 95% efficiency for load currents as high as 2.5A with $V_{OUT}=20V$, using a conventional low-output-voltage, current-mode buck regulator. **Figure 2** shows the efficiency of the regulator.□

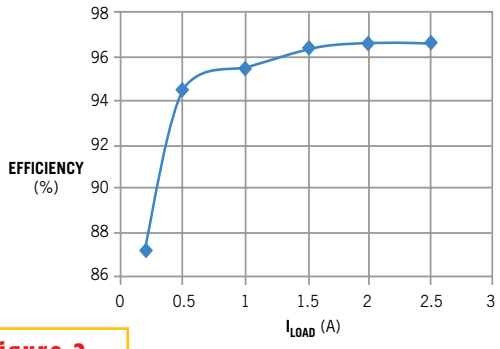

Figure 2

This curve shows the efficiency of the regulator in Figure 1.