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A dry-cooled AC quantum voltmeter

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Abstract

The paper describes a dry-cooled AC quantum voltmeter system operated up to kilohertz frequencies and 7 V rms. A 10 V programmable Josephson voltage standard (PJVS) array was installed on a pulse tube cooler (PTC) driven with a 4 kW air-cooled compressor. The operating margins at 70 GHz frequencies were investigated in detail and found to exceed 1 mA Shapiro step width. A key factor for the successful chip operation was the low on-chip power consumption of 65 mW in total. A thermal interface between PJVS chip and PTC cold stage was used to avoid a significant chip overheating. By installing the cryocooled PJVS array into an AC quantum voltmeter setup, several calibration measurements of dc standards and calibrator ac voltages up to 2 kHz frequencies were carried out to demonstrate the full functionality. The results are discussed and compared to systems with standard liquid helium cooling. For dc voltages, a direct comparison measurement between the dry-cooled AC quantum voltmeter and a liquid-helium based 10 V PJVS shows an agreement better than 1 part in 10^{10} .

Keywords: Josephson voltage standard, Josephson junction, cryocooler, AC quantum voltmeter, ac voltage, programmable Josephson voltage standard, PJVS

(Some figures may appear in colour only in the online journal)

1. Introduction

Josephson voltage standards usually require liquid helium for the operation of the superconducting circuits. Dry cooling of Josephson arrays would be highly advantageous, since liquid helium access might be limited and the safety precautions for the operation with cryogenic liquids could be omitted. Also, for industrial usage in calibration laboratories the permanent availability of a system cooled by electricity is advantageous. Furthermore, the use of cryocoolers allows the setup of fully automated turn-key systems.

Conventional Josephson voltage standards based on drycooled hysteretic Josephson junctions (JJs) are in use for many years [1, 2] and there were efforts to apply such cooling also for programmable Josephson voltage standards (PJVS) [3]. These arrays are very attractive for ac calibrations due to the programmable output voltage. By means of sampling techniques [4–7] and locked synthesiser methods [8] the effect of transients in the waveform can be eliminated [9, 10]. The main challenge of dry cooling is the handling of the chip overheating, which is especially critical for 10 V PJVS arrays with an on-chip heat dissipation typically above 100 mW. First successful cryocooler operation of 1 V PJVS arrays (dissipating only one-tenth of the power) was presented more than ten years ago [11–13], followed recently by standards at the 10 V level [14, 15].

In this paper we present an AC quantum voltmeter [4, 16] with a 10 V PJVS array that operates on a pulse tube cooler (PTC) [17]. In comparison to other cryocooled AC Josephson voltage standards [18–20] the focus of our work was to setup a system for calibration of ac voltages up to 7 V rms and kilohertz frequencies. The general functionality of PTC in Josephson voltage standard applications was already demonstrated by direct comparison measurements [2, 13]. For an effective chip cooling a special thermal interface was tested and characterised experimentally. The presented dry-



Figure 1. Available cooling power of the pulse tube cooler with the PJVS setup installed.

cooled AC quantum voltmeter is fully automated and the functionality is demonstrated by calibrating dc and ac voltages into the kHz range. The operating margins are discussed in detail and the results are compared to systems cooled with liquid helium.

2. Dry cooling of a 10 V PJVS array

2.1. Cryocooler setup

The PJVS array is cooled by a closed-cycle, two-stage pulse tube refrigerator from the TransMIT GmbH [21]. Such a cooler has a long lifetime due to the absence of moving parts at low temperatures. For the presented experiments, the PTC was driven by a 4 kW air-cooled compressor from Sumitomo, with a 3-phase 400 V ac wall power connection. The available cooling power is almost 400 mW at 4.2 K, and 250 mW at 3.7 K (figure 1), the operating temperature of the PJVS array. The temperature of the first stage is about 44 K and the second stage achieves an end temperature of 2.2 K. The cold stage temperature increases slightly after installation the required wiring for PJVS operation. Except the 70 GHz dielectric waveguide, all wiring is thermally anchored at the first stage of the PTC to reduce the heat flow to the cold stage. The coldfinger with the installed PJVS array is magnetically shielded by a cup of cryoperm, a soft magnetic alloy.

A dry cooling is associated with a variation of the cold stage temperature in the cycle period of the operating frequency of the cryocooler. This temperature oscillation (about 200 mK peak–peak with 1.2 Hz) would decrease the operating margins. By means of a reservoir of liquefied helium (50 ml liquid) mounted on the cold stage, the temperature is stabilized to 10 mK peak–peak. Due to the large specific heat of helium the temperature oscillations are damped significantly without a reduction of the effective cooling power [15, 22]. This is in contrast to the setup in DC Josephson voltage standard systems [2], where a plate of stainless steel with a low thermal conductivity is used to stabilise the temperature.

A capillary feeds the helium gas from a tank (31 volume, 12 bar pressure at room temperature) to the 44 K stage and

70 GHz Synthesizer Rotary valve Connection **PJVS** box Wiring Hetank 1st stage (44K) He-pot at 1st stage **Dielectric waveguide** Mylar foil 2nd stage with 100 ml He-reservior Cold finger without mag. shield Thermal Interface with PJVS array

Figure 2. Open pulse tube cooler with Josephson voltage standard setup.

next to a 100 ml reservoir at the cold stage (figure 2), where the helium gas condenses at temperatures below 5 K. The Hepot at the 1st stage is a heat exchanger. It is used for precooling the helium gas in order to increase the rate of liquefaction. A set of Mylar foils protects the first and second stage from the thermal radiation.

2.2. Chip heat transfer

One of the most crucial parameters for a successful dry cooling of PJVS arrays is the heat transfer from the chip to the cold stage of the cryocooler. It is needed to avoid a significant chip overheating due to the dissipated power. In contrast to hysteretic Josephson circuits [2], PJVS arrays produce considerably more heating power which typically exceeds 100 mW. To improve the heat flow between the PJVS chip and the cryocooler cold stage a special thermal interface was successfully tested. Not only the backside of the PJVS array is cooled, also the top side of the chip is thermally connected to a cooled copper plate via a film of vacuum grease Apiezon-N [23]. The backside of the array is connected to a sapphire substrate via a film of indium [14]. For better thermal contact, AuPd is deposited on the silicon backside of the PJVS chip [24]. Finally, this sandwich is mounted on the PTC cold stage. A photograph of the chip mounted on the thermal interface is shown in figure 3.



Figure 3. Photograph of the 10 V PJVS package.



Figure 4. Temperature dependency of the critical current of the last significant bit (LSB) of the PJVS array, a single Josephson junction.

The heat flow of the thermal interface was determined experimentally. The last significant bit (LSB) of the PJVS array, a single JJ, was used as on-chip temperature sensor for this purpose. First the temperature dependence of the critical current $(I_{\rm C})$ of the LSB was measured (figure 4) by means of an integrated heater mounted on the cold stage. In this case the temperature of the PTC was equal to the chip temperature, as the power dissipation of a single JJ is negligible with less than 1 μ W. In a next step, the full PJVS array except the LSB is biased with a current above $I_{\rm C}$ to produce an on-chip heat. The generated heating power, about 45 mW, was determined according to the measured PJVS voltage and the current selected. The temperatures of the chip (T_{Chip}) as well as the PTC (T_{PTC}) were rising and determined after reaching the thermal equilibrium. The chip temperature was detected by a measurement of the critical current of the LSB. From the temperature difference $(T_{\text{Chip}} - T_{\text{PTC}})$ the thermal conductance k was estimated to be about $k = 0.2 \text{ W K}^{-1}$ at $T_{\rm PTC} = 3.7$ K, and 0.3 W K⁻¹ at 4.2 K, respectively. As the thermal conduction at low temperatures is decreasing in general, this behaviour is also observed in the measurement.

The measured *k*-values represent a lower limit, since the chip temperature may be overestimated. In fact the critical current of the LSB is not only affected by temperature but also by microwave radiation generated by intrinsic



Figure 5. Current voltage characteristic of a 10 V PJVS array with altogether 69632 JJs under 69.6 GHz radiation at a temperature of $T_{\text{PTC}} = 3.7$ K. The insets have 20 μ V div⁻¹ vertical resolution.

Current (mA)

oscillations [25], when the JJ-array is biased to the voltage state. For different chip installations the measured *k*-factors vary in the range from 0.2 to 0.5 W K⁻¹ at 4.2 K, which is an adequate reproducibility for this purpose.

2.3. Operating margins of the dry-cooled PJVS array

The current-voltage characteristic under microwave radiation of a complete 10 V PJVS array installed on the described thermal interface is presented in figure 5 at a cold stage temperature of 3.7 K. Shapiro steps with a width of 1.2 mA are seen centred at a bias current of 3 mA. The operating margins reach a maximum at a microwave frequency of 69.6 GHz, although also other frequencies show similar performance. The microwave power was adjusted to generate equal widths of the 0th- and 1st-order Shapiro steps. The on-chip microwave power is 35 mW as determined by a measurement of the temperature increase when the microwave is switched on. For this purpose the PTC cooling power dependence on temperature is taken into account (figure 1). It is in good agreement with the microwave power of about 60 mW applied at the WR12 input flange by taking into account the 1 dB attenuation of the dielectric waveguide used and a reflection of 28% at the finline antenna [26]. Altogether, the total on-chip power dissipation is just 65 mW, consisting of 30 mW dc ($I_{\rm B} = 3$ mA at 10 V), and 35 mW microwave power. The low power consumption was a key factor for a successful chip operation.

The most important feature of the PJVS array is the *intrinsic* Shapiro step width, shown in figure 6. For minimising noise and drift effects just two low-noise current sources are used for biasing, instead of the 17 high-speed channels from the AC quantum voltmeter [16]. One source is biasing the full PJVS array denoted with I_1 at the centre of the positive Shapiro step (I_B) and the second source biases the half array at the negative Shapiro step (-5 V) with a current of $I_2 = -2 \times I_B$. In this state the total voltage is zero and the voltage is read out with high resolution. By tuning I_1 with an additional trim current I_{Trim} through the full array the real



Figure 6. Intrinsic 1st order Shapiro step measurement of a 10 V PJVS array mounted on a cryocooler ($T_{\text{PTC}} = 3.7 \text{ K}$) and in liquid helium for comparison.



Figure 7. Temperature dependency of the current I_{144} , that generates a voltage of 144 μ V for a single JJ (the LSB of the PJVS array), measured without microwave radiation. The insets show schematic *I*–*V*-curves of a JJ and illustrate the I_{144} value.

operating margins of $\Delta I = 1.2$ mA become visible. A Keithley 2182A nanovoltmeter (NPLC 1, filters off) was used to read out the PJVS voltage and 20 readings were acquired for each trim current. The measured standard deviation error bars are about 10 nV, and they are not increased by the cryocooler operation, as seen in comparison to the measurement in liquid helium.

For the two measurements shown in figure 6 the same array was investigated. The Shapiro step centres were $I_{\rm B} = 3.0$ mA for the PTC cooling and $I_{\rm B} = 3.1$ mA in liquid helium, illustrated by the shift of the step. Furthermore, the operating margins are slightly larger in liquid helium. Both effects are related to the differences in the heat transfer and the operating temperatures, discussed in the next section.

2.3.1. Temperature dependencies. A crucial parameter of the cryocooled PJVS array is the temperature dependence of the current (I_{144}) that makes a voltage of 144 μ V for a single JJ without microwave. This voltage agrees with the 1st-order Shapiro step at our driving frequency of 69.6 GHz (see inset

of figure 7). Because I_{144} is close to the centre of the Shapiro step $I_{\rm B}$ when microwave is applied, the I_{144} (T) dependence is a measure for parasitic shifts of $I_{\rm B}$ due to temperature changes. The I_{144} (T) slope should be as small as possible to minimise shift effects, especially if temperature gradients within the PJVS array exist. Such gradients would produce different $I_{\rm B}$ for the individual JJs and for the series connection of the array a decrease in the operating margins results.

Several factors can produce a non-homogeneous on-chip temperature distribution. Firstly, the bias states of the PJVS segments (0 and $\pm I_{\rm B}$) depend on the output voltage and produce a location-dependent heat. This can be especially critical for ac voltage generation with alternating heating powers for the segments. Secondly, the dissipated microwave power is also location-dependent due to microstrip losses and the position of the wave sink, where the microwave is absorbed. Thirdly, the heat transfer could depend on the chip position as well due to an inhomogeneous wetting with Apiezon and indium. As the heat transfer of the thermal interface was measured only for the whole array, no conclusion can be drawn concerning the homogeneity. In [27] a simulation model is presented to estimate the on-chip temperature distribution for PJVS circuits operated on 10 K cryocoolers.

In summary, these effects are responsible for the slightly lower Shapiro step width in a cryocooler compared to liquid helium (figure 6). Their influences become less important when the absolute dissipated on-chip power is small as well as the I_{144} (T)-slope. Therefore the JJ parameters were adapted for cryocooled PJVS arrays by optimising the fabrication technology [28]. The resulting $I_{144}(T)$ dependence is shown in figure 7. The slope is relatively small for temperatures below 4 K, and the rising characteristic is mainly the result of a decreasing normal resistance R_N with temperature for this type of JJs. The critical current density of the JJ was reduced from 4 to 2 kA cm^{-2} while maintaining the characteristic voltage of about $I_{\rm C}R_{\rm N} = 140 \,\mu {\rm V}$. The smaller critical current (about $I_{\rm C} = 2.5 \,\text{mA}$ at $4.2 \,\text{K}$) is accompanied by a reduced centre bias current $I_{\rm B}$ of the Shapiro step with less dc power generation. At the same time, the required microwave power is reduced as well, since the microwave current needed to generate Shapiro steps is nearly proportional to the critical current. Even a microwave power of 35 mW is sufficient to establish Shapiro steps with widths exceeding 1 mA. Therefore, many existing microwave Gunn oscillators between 70 and 75 GHz used for conventional DC Josephson voltage standards can be used also to drive PJVS.

The Shapiro step of the whole array was investigated in the temperature range between 2.7 and 6 K (figure 8). For this measurement just one current source is used for biasing the complete PJVS array. The observed characteristics of $I_{\rm B}$ and ΔI are the result of the Nb/Si-junction [29, 30] dependencies on the critical current $I_{\rm C}$ and the normal resistance $R_{\rm N}$. At temperatures below 3.7 K a retrapping current $I_{\rm R}$ [31] is observed (open circles in figures 4 and 8), which results in a hysteretic *I*–*V*-curve. Therefore the Shapiro step width decreases at lower temperatures as well, since the step becomes partly ambiguous. The open circles in figure 8 represent down-sweep currents, the full circles up-sweep. In



Figure 8. Dependence of the PJVS operating margins ΔI and the overall bias current position $I_{\rm B}$ for the entire PJVS array versus temperature.

general, hysteretic quantised voltage states are not desirable for PJVS operation.

The optimal cold stage temperature is $T_{\text{PTC}} = 3.7$ K with a maximum step width of 1.2 mA. The limited thermal conductance results in a chip temperature approximately 0.3 K higher ($T_{\text{Chip}} = 4.0$ K) when the PJVS is operated. Taking into account the effective chip surface of 2 times 1 cm × 1.5 cm (Front and back side) the associated heat transfer is about 0.02 W cm⁻² ($P_{\text{Chip}} = 65$ mW). In comparison, the situation in liquid helium is more relaxed. For the same heat transfer the temperature difference is below 0.1 K, according to the characteristic curve of helium pool boiling [32].

The Shapiro step centre $I_{\rm B}$ increases with temperature, as expected from the $I_{144}(T)$ dependence (figure 7). For example, if a temperature change of 0.3 K occurs at the operating temperature of 3.7 K, a shift in the bias current of just $\Delta I_{\rm B} = 0.1$ mA is expected.

As intended, the low bias current of $I_{\rm B} = 3$ mA results in a small on-chip heat loss. This is not only advantageous for cryocooler operation, but also for liquid cooling since it reduces the helium consumption. Another significant criterion of PJVS arrays is the ratio of Shapiro step width and its centre bias, which is $\Delta I/I_{\rm B} = 0.39$ in the optimal case $(T_{\rm PTC} = 3.7 \text{ K})$. A high ratio is advantageous, since relative drifts of the current bias sources became less influential.

In the temperature range between 3 and 4.2 K the operating margins are above our target value of 1 mA. By using just a 2 kW compressor the end temperature of the PTC is expected to be around 4 K including the 65 mW heat load in the PJVS operation. This results in a 1.1 mA step width, which would be also sufficient for stable operation.

3. AC quantum voltmeter measurements

3.1. AC calibrations

The ac measurements of Fluke 5700A calibrators reported in this section were performed with the AC quantum voltmeter



Figure 9. Operating margins for ac calibrations of a Fluke 5700 A calibrator at nominal 7 V rms and 1 kHz frequency.

setup reported in detail in [33]. A fast sampler (NI 5922) digitises the difference between the ac voltage and the synchronised stepwise waveform of the PJVS (20 Josephson steps per period). For the calibrations, a list of ac voltages that will be measured fully automatically can be loaded from a file. The measurements were carried out at a cryocooler temperature of $T_{\text{PTC}} = 3.7$ K. An additional stabilisation of the temperature was not required due to the large operating margins and their low temperature dependence (figure 8).

A trim current experiment was performed to investigate the operating margins for ac calibrations. An example is shown in figure 9 for a nominal calibrator voltage of $V_{\text{NOM}} = 7 \text{ V}$ rms at 1 kHz frequency. The vertical axis shows the relative difference from the nominal value of the calibrator. The error bars represent the standard deviation. A data point is the mean of ten measurements, each with an integration time of 1 s. The time required for averaging and reconstruction the voltage is negligible, because the signal post-processing is done simultaneously while the sampler digitises the next waveform.

PJVS arrays with large operating margins in liquid helium can exhibit just marginal Shapiro steps in a PTC when the thermal interface is insufficient. Often this behaviour is not detectable for low output voltages (small on-chip heat). Therefore, in order to cover the worst possible scenario regarding chip overheating the highest rms voltage was investigated.

For the measurements each segment of the PJVS was biased on its centre of its Shapiro steps, and an additional trim current was swept through the full array. The trim current ranges from -0.6 to +0.6 mA in steps of 50μ A and this sweep was repeated four times. A flat step of about 0.8 mA can be seen, however the various data points for a constant trim current are not always within the individual standard deviations. This behaviour was already observed in former experiments [7, 16] and clearly demonstrates that the calibrator ac voltage has a significant drift exceeding the white noise level. This was confirmed by Allan deviations is in



Figure 10. AC measurements of a Fluke 5700 A calibrator at 7 V rms in the frequency range between 30 Hz and 2.5 kHz. The calibrations were done with liquid helium (red) and with a dry-cooled AC quantum voltmeter (blue).

the range of 10^{-8} , as shown in [34] for a liquid helium cooled AC quantum voltmeter.

The measured ac operating margins of 0.8 mA are sufficient for calibrations, but a reduction is noticed compared to the intrinsic Shapiro step width of 1.2 mA according to figure 6. This can be caused by several factors.

Firstly, the noise level is lower in the intrinsic Shapiro step setup. Here only two current sources with a bandwidth of 100 Hz bias the PJVS array, whereas in the AC quantum voltmeter setup a total of 17 bias sources are used, each with hundred megahertz bandwidth. The higher bandwidth is required to change steps as quickly as possible. This seems to be the dominant source of the step width reduction, since a similar result was found also in the dc comparison measurements reported in the last section.

Secondly, the connected device under test (calibrator Fluke 5700 A) has some internal noise level, which reduces the margins as well.

Thirdly, another reason is related to the PTC cooling. As already mentioned, ac voltage operation of the PJVS generates a location depended heat, resulting in on-chip temperature gradients which reduce the margins. Furthermore, between the states U = 0, and 10 V there is a change in the on-chip power of 30 mW ($I_{\rm B} = 3$ mA). This results in a temperature modulation of the chip of about $\Delta T = 0.15$ K (thermal conductance 0.2 W K⁻¹) with the frequency of the ac voltage. In consequence, the Shapiro step width (ΔI) and the centre currents ($I_{\rm B}$) of the segments are changing as well, and a decrease in the operating margins results.

Demonstrating the performance of the setup, the 7 V rms voltage was calibrated for various frequencies in the range from 30 Hz up to 2.5 kHz. In order to minimise the mentioned drift effects of the calibrator, the ac voltage was measured with 10 s integration time for the shown set of frequencies (figure 10), and this procedure was repeated 10 times. The data points in figure 10 are the mean of the 10 measurements, and the error bars represent the standard deviation, which are



Figure 11. 10 V dc calibration of a Fluke 732 A standard with a liquid helium- and a dry-cooled AC quantum voltmeter.

about $1 \,\mu V/V$. The results are in good agreement with the measurements using a liquid helium cooled AC quantum voltmeter the following day.

In conclusion, the ac calibrations performed demonstrate the full functionality and reproducibility of the dry cooling setup.

3.2. DC calibrations

As a further example, dc standards were investigated as well. A time sequence of a 10 V calibration of a Fluke 732 A voltage standard is presented in figure 11. The setup described in [33] was used, in which a Keithley 2182 A nanovoltmeter (NPLC 1, filters off) reads out the voltage difference and a multiplexer reverses the polarity of the 732 A to eliminate thermal EMFs. Altogether 20 readings are acquired for each polarity. The measurements were performed with the dry-cooled quantum voltmeter, and the following day with a liquid helium system. The results of the averages coincide within their standard deviation of about 100 nV. The measured operating margins were about 0.9 mA.

3.3. Direct Josephson comparison

The intrinsic accuracy of the dry-cooled AC quantum voltmeter was investigated by a direct comparison to a second Josephson voltage standard, which is cooled with liquid helium. The same measurement setup as for the dc calibration of Fluke 732 A standards was used, but with the difference that the polarity is reversed not by the multiplexer [33] but by the Josephson standards themselves. Again a trim current sweep of the dry-cooled PJVS was performed (figure 12(b)) and a time sequence is presented in figure 12(a) at zero trim current. The operating margins are about 0.8 mA and similar to the previous ac calibrations. The data points in figure 12(a)combine twenty readings each in positive- and negative polarity to eliminate the thermal EMF The error bars represent the standard deviation of about 15 nV, which is slightly larger as the 10 nV seen in the intrinsic Shapiro step measurement (figure 6). The difference between the Josephson voltages is on average 0.5 nV (dotted magenta line in figure 12(a)). The



Figure 12. Direct comparison measurement at 10 V of a dry-cooled and a liquid helium based AC quantum voltmeter, (a): time sequence, (b): operating margins.

Table 1. Uncertainty budget for the 10 V dc comparison.

Component	Uncertainty (nV)
Type A	
6 min integration time	0.50
Type B	
Frequency offset	0.04
Null detector, gain	0.01
Leakage current	0.17
Total uncertainty $(k = 1)$	0.53

standard deviation of the 16 data points is 2 nV, resulting in a Type A uncertainty of 0.5 nV.

The Type B uncertainty contributions are listed in table 1. The gain of the null detector was determined before and after the measurement to $g = 0.999\,984$ and 0.999 989, respectively. By taking into account the maximum difference voltage of 0.6 μ V, the relative error due to the null detector gain is less than 1×10^{-12} . The AC quantum voltmeter bias sources are supplied from isolation transformers and the measured isolation resistances to ground were about $R_{\rm ISO} = 100 \,\rm G\Omega$. The lead resistance of the measurement loop is about $R_{\rm LEAD} = 3 \,\Omega$, and the associated systematic error caused by leakage currents can be estimated according to the resistance divider of $R_{\rm LEAD}$ and $R_{\rm ISO}$ to 1.7×10^{-11} (rectangular distribution assumed). Both 70 GHz synthesisers are phase looked to the same 10 MHz reference, and the relative frequency offset between them is less than 4×10^{-12} [16]. Altogether the relative agreement is better than 1×10^{-10} at 10 V.

4. Conclusion

A dry-cooled AC quantum voltmeter was presented. Special attention was paid to the cooling of the 10 V PJVS array because the chip heat transfer was found to be a crucial factor for successful operation. By optimising the thermal interface and by reducing the on-chip power dissipation we were able to attain Shapiro step widths above our initial target value of 1 mA. This is comparable to the operating margins achieved with standard cooling in liquid helium. In order to investigate the performance of a dry cooled PJVS the pulse tube cryocooler was integrated in an AC quantum voltmeter setup and several calibration measurements of calibrator ac voltages up to kilohertz frequencies were performed. The operating margins for the different calibration modes were found to be 0.8 mA and are adequate for calibrations. The reproducibility of the system was proven by comparing the results with a liquid helium cooling setup. A direct dc-voltage comparison of the dry-cooled AC quantum voltmeter with a second PJVS shows an agreement of better than 1×10^{-10} , thus demonstrates the full functionality of such a dry-cooled system.

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