ACTA IMEKO
July 2012, Volume 1, Number 1, 59-64
www.imeko.org

Low distortion signal generator based on direct digital synthesis for ADC characterization

Walter F. Adad, Ricardo J. Iuzzolino

Instituto Nacional de Tecnología Industrial, Av. General Paz 5445, Buenos Aires, Argentina

This paper presents a low distortion signal generator with a frequency range from 0 to 10 kHz using the direct digital synthesis (DDS) method for ADC characterization. The results show that the maximum distortion in the whole frequency range is -80.37 dB, the frequency resolution is 1.421 nHz (with a 48-bits DDS chip), the stability in frequency is 25 µHz/Hz and the amplitude stability is 13 µV/V.

Keywords: Direct digital synthesizer, frequency synthesizers, direct digital synthesis, ADC characterization.

Citation: Walter F. Adad, Ricardo J. Iuzzolino, Low distortion signal generator based on direct digital synthesis for ADC characterization, Acta IMEKO, vol. 1, no. 1, article 12, July 2012, identifier: IMEKO-ACTA-01(2012)-01-12

Editor: Pedro Ramos, Instituto de Telecomunicações and Instituto Superior Técnico/Universidade Técnica de Lisboa, Portugal

Received January 10th, 2012; **In final form** July 10th, 2012; **Published** July 2012

Funding: This work was supported by Instituto Nacional de Tecnología Industrial

Corresponding author: Walter F. Adad, e-mail: adad@inti.gob.ar

1. INTRODUCTION

Analog-to-digital converters (ADC) and digital-to-analog converters (DAC) have to be characterized in static and dynamic regime [1].

Static characterization can be made using a solid state DC voltage standard or a Josephson system. While, for dynamic characterization, it is necessary to excite the ADC with different types of signals waveforms, amplitudes and frequencies. To attack these problems we have designed an arbitrary function generator based on direct digital synthesis (DDS).

This technique has some advantages in comparison with others techniques, such as phase-locked loop (PLL). The DDS technique has higher frequency resolution, usually generators based on PLL have a limited frequency resolution in the order of $1{:}10^6$, although some advanced PLL achieve much higher resolutions, while DDS technique can achieve values of frequency resolution in the order of $1{:}10^{14}$. Additionally, the total harmonic distortion (THD) of PLL generators typically has values of -40 dB in comparison with a THD better than -70 dB achievable by DDS devices.

Moreover, in DDS devices the stability in frequency depends on the reference external oscillator, multiple devices can be synchronized, facility of great importance in multi-tone applications. Finally, the DDS devices are software programmable and easy to use.

This function generator can be used in other applications such as impedance measurements (as described in [2]) and any measurement schemes which require alternating signals as stimulus.

2. THEORY OF OPERATIONS OF DIRECT DIGITAL SYNTHESIS

DDS technique consists in digital processing to generate signals at different frequencies and phases selectable by software, from a reference clock.

As the DDS technique consists in dividing the reference clock frequency from a tuning word selectable by software, the relationship between the tuning word, the clock reference, the number of bits of the DDS and the desired output signal frequency is given by [3]

$$f_o = \frac{\delta\varphi}{\delta t} = M\frac{f_{clock}}{2^N}, \tag{1}$$

where δt is the duration of a DDS time step ($1/f_{clock}$) and $\delta\varphi$ is the phase angle changing in one time interval δt. Considering that the tuning word (M) is the amount by which the phase accumulator increments on each DDS time step and that 2^N is the capacity of the phase accumulator, then $\delta\varphi = M / 2^N$ (with N equal to the number of bits of the phase accumulator). Combining these results gives the frequency of the output sine wave (f_o).

Replacing $M = 1$ in equation (1) gives the frequency resolution of the DDS devices as

$$f_r = \frac{f_{clock}}{2^N}. \tag{2}$$

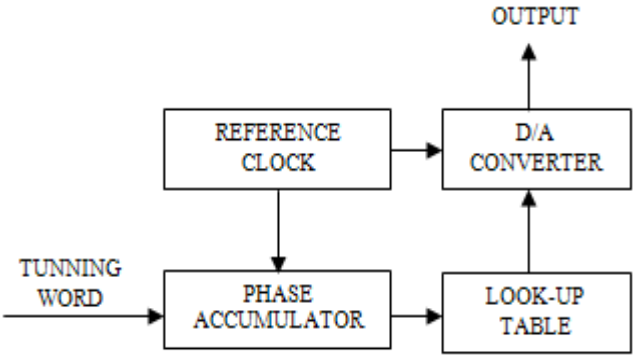

Figure 1. Simplified block diagram of a DDS device.

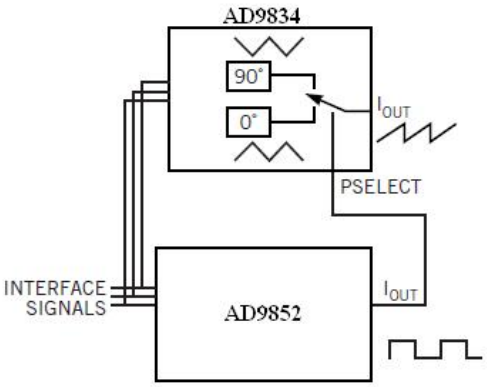

Figure 3. Simplified block diagram of the sawtooth waveform generation.

For example, with 48 bits DDS and a reference clock of 400 kHz it is possible to obtain a frequency resolution of 32.52 nHz.

A simplified block diagram of DDS device is depicted in Figure 1. The block diagram consists of four blocks: a reference clock, a phase accumulator, a look-up table and a D/A converter.

The phase accumulator sums at each clock pulse the tuning word. Thus, its output is a digital ramp (binary code), as shown in Figure 1.

The look-up table converts the phase accumulator output to a digital sinusoidal waveform.

Because of limitations in the number of bits of the look-up table, the high resolution output of the phase accumulator (32 or 48 bits) is truncated. This truncation introduces spurious components in the output signal spectrum that must be filtered in order to obtain low distortion.

As is explained in [3], the main spurious component due to phase accumulator truncation is situated at

$$f_{spur} = \mathrm{mod}\left(M, 2^{(N-W)}\right)\frac{f_{clock}}{2^{(N-W)}} \tag{3}$$

where f_{spur} is the frequency of the main spurious component due to truncation in the phase accumulator, mod(·) is the modulus operator, N is the resolution of the phase accumulator and W is the number of bits entering the look-up table.

Finally, the D/A converter transforms the digital sinusoidal waveform into an analogue signal. The nonlinearities of the D/A converter are the major source of harmonic distortion.

3. SYSTEM DESCRIPTION

Figure 2 shows a simplified block diagram of the developed generator.

Internal clock and external clock blocks in the diagram represent the reference clock. The clock selector allows choosing between the internal clock (a quartz crystal) and an external clock. This clock selector is controlled by a microcontroller. Since the DDS technique does not introduce frequency instability to the system, the stability in frequency is dominated by the internal or external clock.

The clock provider block delivers the clock signal to the system and also provides an external output for synchronization with other systems.

The system generates single-tone, multi-tone, triangular, saw-tooth and square waveform signals. To generate dual tone signals, two AD9852 devices are used, while to generate single-tone signals, one of them can be used.

Since the AD9852 are only capable of generating sinusoidal and square waveforms, a third DDS was added, the AD9834, to generate triangular and saw-tooth waveforms.

To generate the triangular waveform, the AD9834 internally bypasses the look-up table and directly connects the phase accumulator output to the DAC.

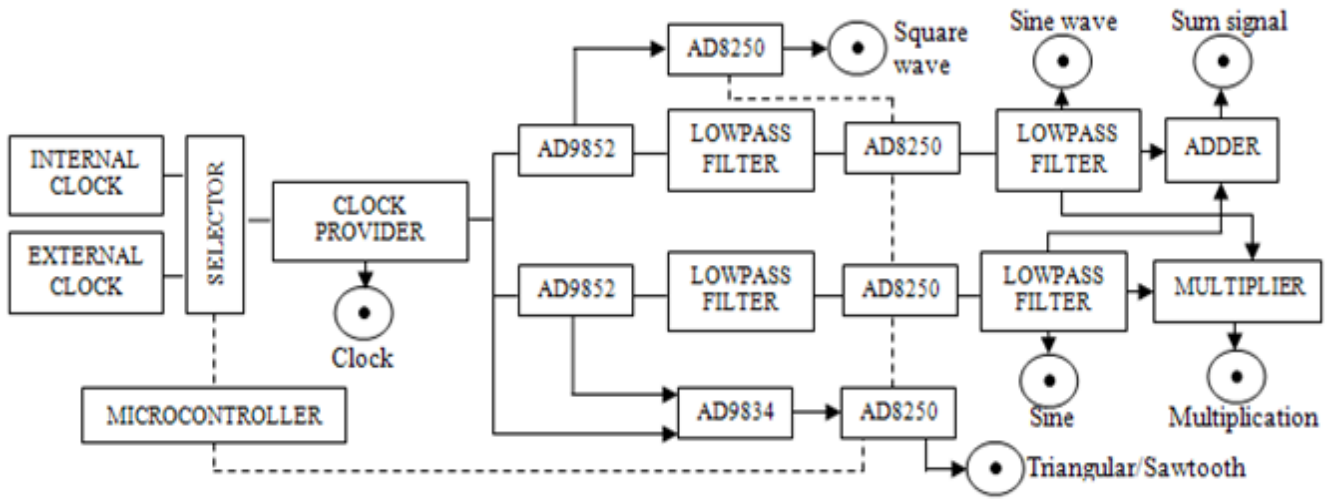

Figure 2. Simplified block diagram of the developed generator.

On the other hand, to generate the saw-tooth waveform, as suggested in [4], pulses generated by the AD9852 switch between the phase of the two triangular waveforms produced by the AD9834. Figure 3 illustrates this situation.

As it has been described in last section the digital output signal must be filtered.

Therefore, Butterworth low pass passive filters of third order with a cut-off frequency of 20 kHz were placed at the output of the AD9852. As in [5], they were implemented with passive components so that the only noise source is the thermal noise introduced by resistors. The Butterworth topology was used because of the flatness in the passband.

To generate different amplitudes of the output signals, low distortions Programmable Gain Amplifier (PGA) were employed, the AD8250. The gain can be set to 1, 2, 5 or 10.

Next to the low distortion amplifiers, lowpass filters were placed (in the case of sinusoidal signal) to remove spurious frequencies generated by the PGA. They have the same topologies of the first one, but with a cut-off frequency of 100 kHz.

Finally there are an adder and a multiplier circuit to generate the dual tone signals. AD734AN is used as multiplier because of its low distortion.

4. SOURCES OF DISTORTION

In order to evaluate the DDS behaviour the main distortion sources were analyzed, which are:

- Phase accumulator truncation.
- Internal D/A converter.
- Interference between tracks in the PCB design.

To study the capabilities of the system a simulation program was developed. Simulation results have shown that the spurious frequency due to phase accumulator truncation were over the bandwidth of the system (10 kHz), and can be filtered properly with the filters mentioned in the previous section. These reconstruction filters, also reduce the harmonic distortion caused by the D/A converter.

To reduce the quantization noise effects introduced by the D/A converter, different measurements were performed in the system. Some of these measurements are showed in section 5.1 and they consist of varying the relationship between the DDS output frequency and the reference clock frequency.

The PCB was designed to reduce interference between tracks, as suggested in [6] and [7]. The following issues were taken into account:

- Ground plane inclusion. A two layers PCB was designed. The bottom layer as a ground plane. With its inclusion the THD has been reduced in 10 dB.
- Capacitive crosstalk reduction. To reduce the interference between tracks, parallel tracks were avoided, keeping them as short as possible.
- DDS's AD9852 synchronization. The generation of dual-tone signals employs two AD9852 devices synchronized. To accomplish that, the tracks from the reference clock to these devices were routed keeping both the same length.
- Reference clock low impedance return path. Tracks crosses behind the track of the reference clock (bottom layer) were avoided in other to prevent the spread of the return current throughout the circuit.

Figure 4 shows the PCB design of the two-tone sinusoidal generator.

5. RESULTS

To verify the system performance, different tests were carried out. Most of these tests were realised in order to achieve the target THD.

5.1. Spectral analysis without reconstruction filters

In order to evaluate the THD of the system, a simulation program was developed. It implements the four blocks shown in Figure 1.

Figure 5, shows the DDS spectrum obtained by simulation

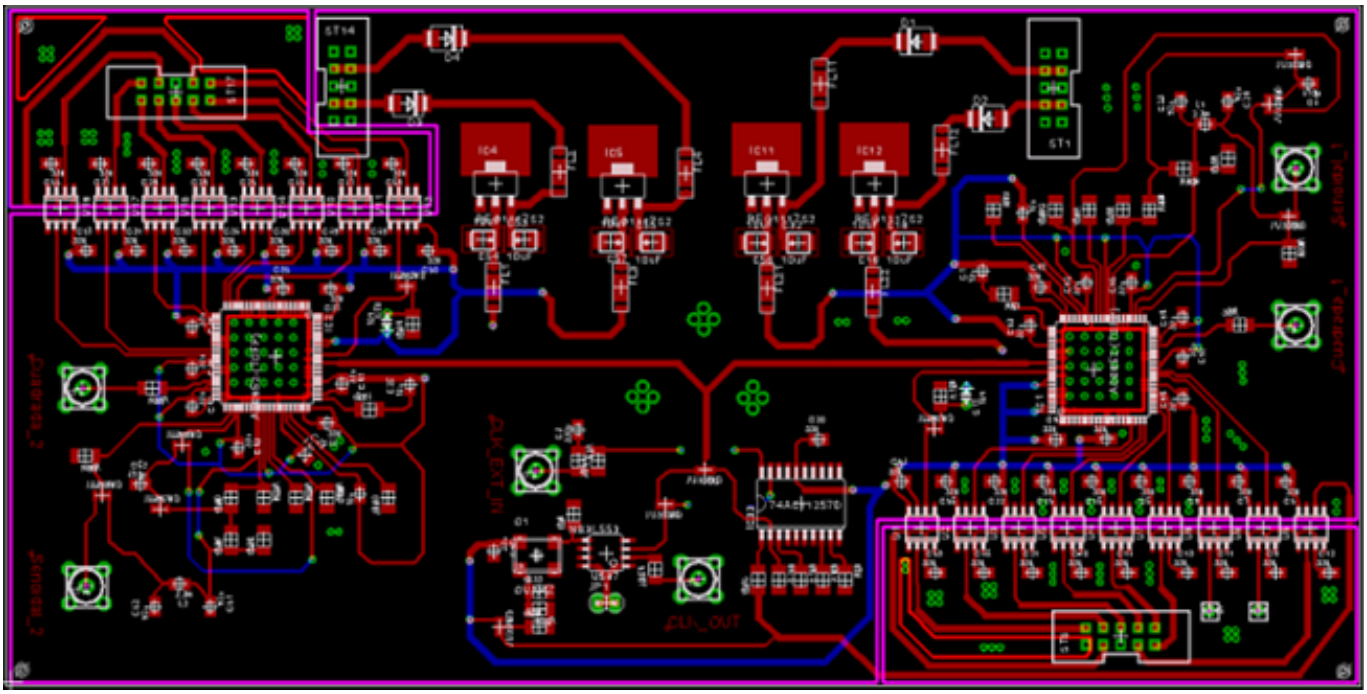

Figure 4. PCB design.

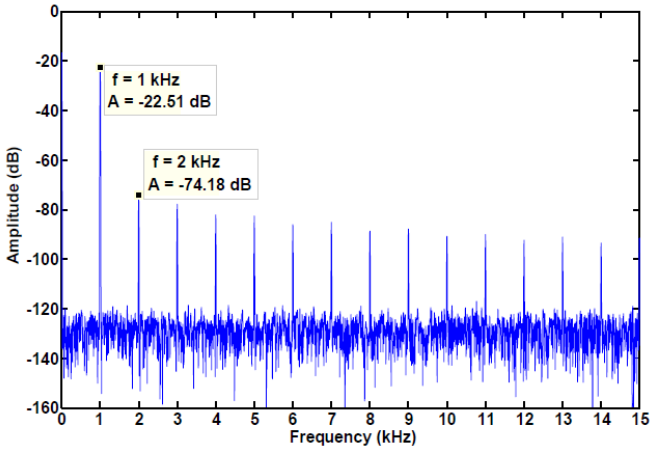

Figure 5. DDS Output spectrum obtained by simulation.

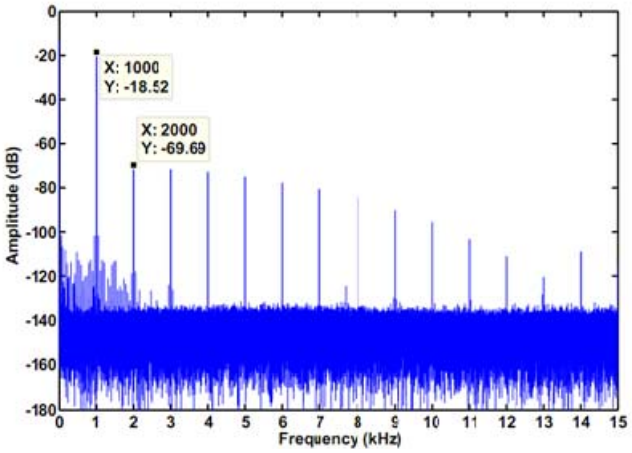

Figure 7. DDS Output spectrum obtained by measurement.

at the output of the D/A converter. A Spurious free dynamic range, SFDR = -51.67 dBc was achieved.

Then, the output of the system without the reconstruction filter was measured using the setup showed in Figure 6. In this scheme, the DDS was programmed through a microcontroller connected to a PC to generate a frequency of 1 kHz. The output signal of the DDS was acquired with an acquisition system developed in the laboratory which has a THD = -100 dB.

The measured output spectrum is depicted in Figure 7, where a SFDR = -57.17 dBc can be observed. These results illustrate the necessity of including reconstruction filters to obtain a low distorted signal.

It is important to point out that the SFDR achieved is due to a reconstruction filter was not applied in order to evaluate the DDS performance.

5.2. Spectral analysis after the application of the reconstruction filter

Using the measurement setup showed in Figure 6, but adding the reconstruction filter described in previous section at the output of the DDS, a THD of -80.37 dB was obtained by measurement while a THD of -80.62 dB was obtained by simulation. It is important to mention that in this case the SFDR is equal to the THD because the amplitudes of the harmonics three to six is depreciable with respect to the strongest spurious frequency (situated in the second harmonic).

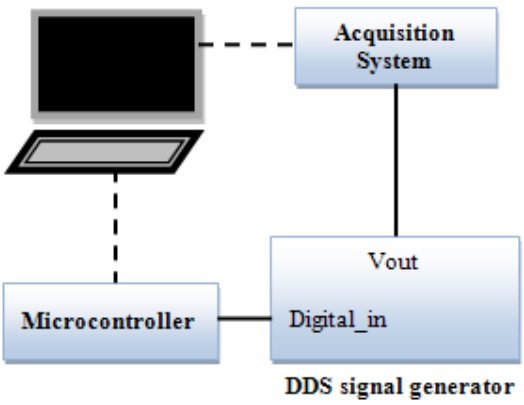

Figure 6. Measurement setup employed to evaluate the output spectrum of the system without the reconstruction filters.

The results are summarized in Table 1 and showed in Figure 8.

As a conclusion, the introduction of the reconstruction filter reduced considerably the THD, eliminating harmonics above 7 kHz and reducing the amplitude of the first five.

5.3. Influence of reference clock frequency on the output signal spectrum

To study the behaviour of the system, the THD of the DDS was calculated at different frequencies of the reference clock using the measurement setup showed in Figure 9.

As in Figure 6, the DDS was programmed through the microcontroller connected to a PC to generate a determinate frequency (1 kHz and 0.227 V). Using a programmable signal generator, the reference clock frequency of the DDS was varied in order to select the best frequency for it. The filtered output signal of the DDS was acquired with the same acquisition system as in the previous test.

Table 2 and Figure 10 show the THD obtained by measurement at different relationships between the frequencies of the reference clock and the DDS output signal.

These results also confirmed the DAC SFDR specification of the AD9852 device increasing the SFDR as the reference clock frequency and output frequency ratio change [8]. As a conclusion, a THD of -80 dB (objective of this work) was achieved when the relationship between frequencies of the reference clock and the DDS output signal was set to 80 and 100.

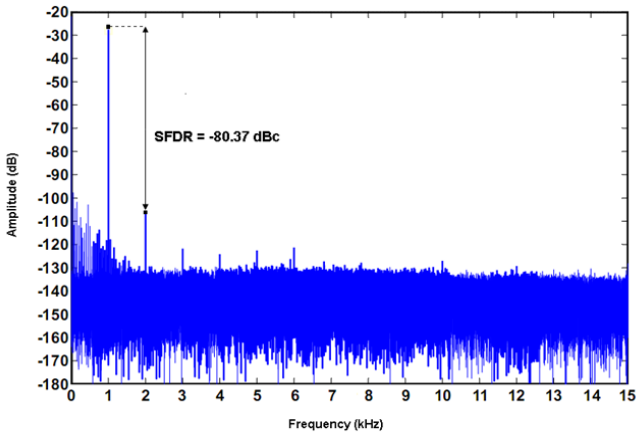

Figure 8. DDS Output spectrum obtained by measurement after the application of the reconstruction filter.

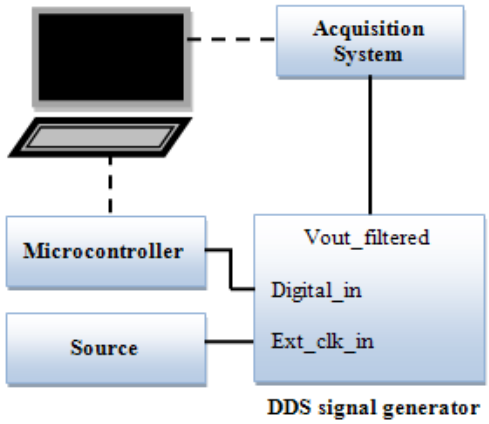

Figure 9. Measurement setup.

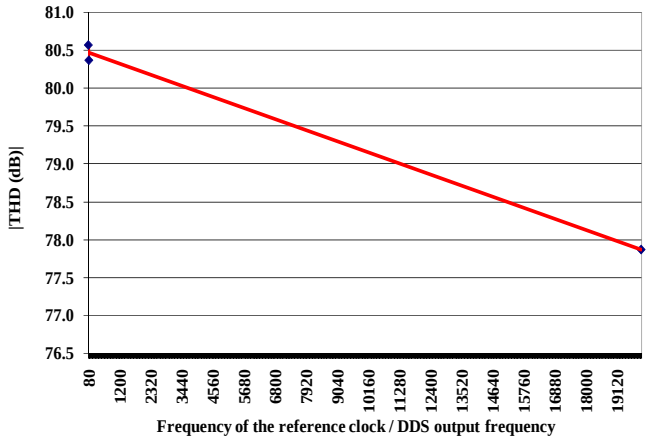

Figure 10. THD as a function of the frequency of the reference clock.

This behaviour is taken into account when selecting the clock frequency, and for that reason we use as upper limit to select the clock frequency 400 kHz. As indicated previously with this range is possible to filter the output signal of the DDS by a 3rd order low pass filter.

5.4. Influence of set the DDS output frequency to an exact submultiple of the reference clock frequency

Using the measurement setup shown in Figure 9, the DDS was programmed to generate an output frequency which is multiple of the reference clock. After that, the DDS was programmed to generate an output frequency which is not multiple of the reference clock.

The results are shown in Table 3. They show a difference of 0.2 dB in the THD when the output signal frequency was not an integer multiple of the reference clock frequency.

Table 1. Maximum Total Harmonic Distortion of the system.

THD simulated	THD measured
-80.62 dB	-80.37 dB

Table 2. THD at different f_{REFCLK}, f_0 ratios.

DDS output frequency	Clock reference frequency	$\frac{f_{REFCLK}}{f_0}$	THD
1 kHz	20 MHz	20000	-77.87 dB
1 kHz	100 kHz	100	-80.37 dB
1 kHz	80 kHz	80	-80.57 dB

Table 3. THD as function of DDS output frequency.

DDS output frequency	Clock reference output frequency	THD
1000 Hz	80 kHz	-80.57 dB
1001.457 Hz	80 kHz	-80.77 dB

Table 4. Influence of multiplier in the THD.

DDS output frequency	Clock reference frequency	Multiplier	THD
1 kHz	80 kHz	x5	-80.16 dB
1 kHz	100 kHz	x4	-80.16 dB

Table 5. Frequency and amplitude stability of the DDS output.

Frequency stability	Amplitude stability
25 µHz/Hz	13 µV/V

5.5. Internal frequency multiplier

The AD9852 has an internal frequency multiplier with which is possible to increase the frequency of the device internal clock.

To evaluate the influence of this frequency multiplier on the THD, from the measurement setup showed in Figure 9, the DDS was programmed to generate the same output frequency using different multiplier settings. Then the THD was obtained.

The results are depicted in Table 4.

It is important to point out that the DDS internal frequency was the same at both cases (400 kHz). As can be seen in Table 4, no changes were observed in the THD at different values of the DDS internal multiplier, therefore there is not variation of the THD as a function of the DDS internal multiplier.

5.6. Frequency and amplitude stability

In order to measure the frequency and amplitude stability of the signal generator designed, the DDS was programmed through a microcontroller to generate 62.5 Hz sinusoidal wave (0.227 V) using the internal clock of the system.

To analyse the frequency stability, the output signal of the generator was connected to a time interval counter, which was programmed to collect data through a PC during ten hours.

To measure the amplitude stability, the output of the generator was measured employing a high accuracy multimeter.

The measurement results of the frequency and amplitude stability are shown in Table 5.

Figure 11 depicts the Allan deviation, $\sigma_y(\tau)$, of the DDS output signal frequency when the internal clock was used.

The standard deviation is a statistic tool employed to quantify the dispersion of a number of samples. The variance is a numeric measure of the deviation of these samples with respect to the mean value. However, the classic variance only can be calculated from stationary data. It implies that the data is independent of time. When data is not stationary (such as in frequency and amplitude measurement), classic variance does not converge and another tool is required. So, the Allan

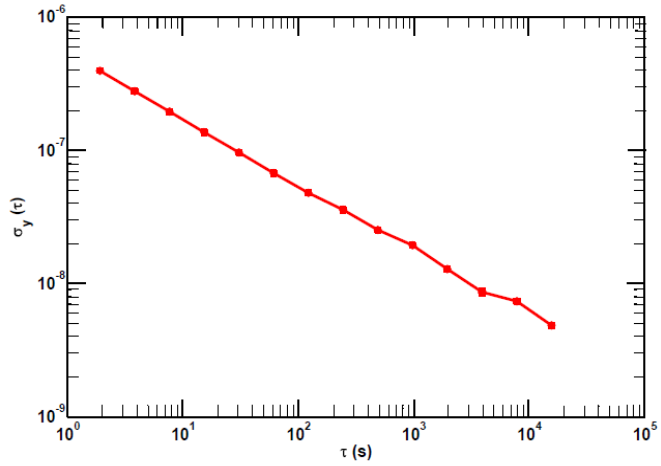

Figure 11. Allan deviation of the DDS frequency output signal.

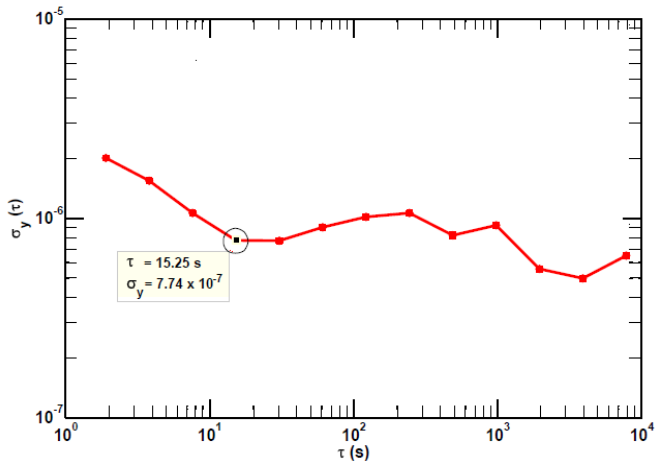

Figure 12. Allan deviation of the DDS amplitude output signal.

variance was used because it converges for different types of noise present in electronic circuit [9].

Figure 11 shows that an averaging time in the range of 20 to 16000 s can be employed because of the predominant noise in the whole range is white noise.

It is important to note that the DDS technique does not introduce frequency instability to the system, so it is the frequency stability of the reference clock.

Figure 12 shows the Allan deviation of the output signal amplitude. In this case, to achieve the optimal $\sigma_y(\tau)$, an averaging time (τ) of 15.25 s has to be used because this τ is the minimum $\sigma_y(\tau)$ in the range of white noise.

6. CONCLUSION

We designed a low distortion (-80.37 dB) arbitrary function generator of a resolution equal to 1.41 nHz and frequency stability of 25 μHz/Hz.

The total harmonic distortion reached by the proposed design is suitable for the application, but one possible modification can be performed in order to improve this feature. It consists in the use of an external digital to analogue converter (DAC) with more bits and low distortion at the output of AD9852. It is important to note that this device can be programmed to employ an external or internal DAC.

The proposed signal generator was designed to generate multi-tone signals in a relatively simple way. For example, to generate four tones, as the device can be synchronized to an external clock, adding a second board and connecting an external clock to both PCBs, the system will be capable of generating four tones. In comparison with commercial signal generators most of them can generate two tone signals.

During these research other DDS commercial chip was analyzed, the AD9959. This device has four DDS cores. The advantage of employing it is that four tone signals can be generated with one PCB (in comparison with the system presented in this paper). Despite this, the design with this device was discarded because it was analysed that while a good PCB design could ensure a feature of – 100 dB SFDR, the limitation is given by the isolation between channels of the device specified as better than 65 dB [10]. Other disadvantages are lower frequency resolution (32 bits in comparison with 48 bits of the AD9852) and internal DAC of 10-bits instead of 12-bits converters of the implemented design.

Other important conclusion obtained from the results is that as the direct digital synthesis technique is based on digital signal processing it does not introduce instability to the frequency. Therefore, the only contribution to the frequency uncertainty is the relative uncertainty of the reference crystal. As the system has the possibility to use an external reference clock, the achieved stability can be improved.

This function generator may be used in electrical metrology and in schemes of measurements that require AC signals as a stimulus, for example, in Time and Frequency domain, where a Cesium clock can be used to synchronize the system proposed (so the frequency stability of the system is the frequency stability of the Cesium) and the DDS can be programmed to generate different frequencies to test frequency meters.

REFERENCES

[1] IEEE, Tech. Rep., "IEEE Std 1241.2001, IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters," 2001.

[2] Fu, Y.; Li, Z.; Zhang, Z.; Sun, J.; Chen, L.; , "DDS sources for precise measurement", Precision Electromagnetic Measurements (CPEM), 2010 Conference on , vol., no., pp.402-403, 13-18 June 2010.

[3] Analog Devices, "A Technical Tutorial on Digital Signal Synthesis", 1999.

[4] Collins, N. & Limerick, "DDS devices produces sawtooth waveform", 2003.

[5] Lacanette, K., Application Note, AN-779, "A basic introduction to Filters – Active, Passive, and Switched Capacitor NI", 1991.

[6] Montrose, M. I. "Printed Circuit Board Design Techniques for EMC Compliance", 2000.

[7] Brandon, D. "Synchronizing Multiple AD9852 DDS-Based Synthesizers", 2003.

[8] Analog Devices, "CMOS 300 MSPS Complete DDS AD9852", 2002-2007.

[9] López, J. M., "La varianza de Allan en la metrología del tiempo y la frecuencia", 2005.

[10] Analog Devices, "4-Channel, 500 MSPS DDS with 10-Bit DACs AD9959", 2005-2008.