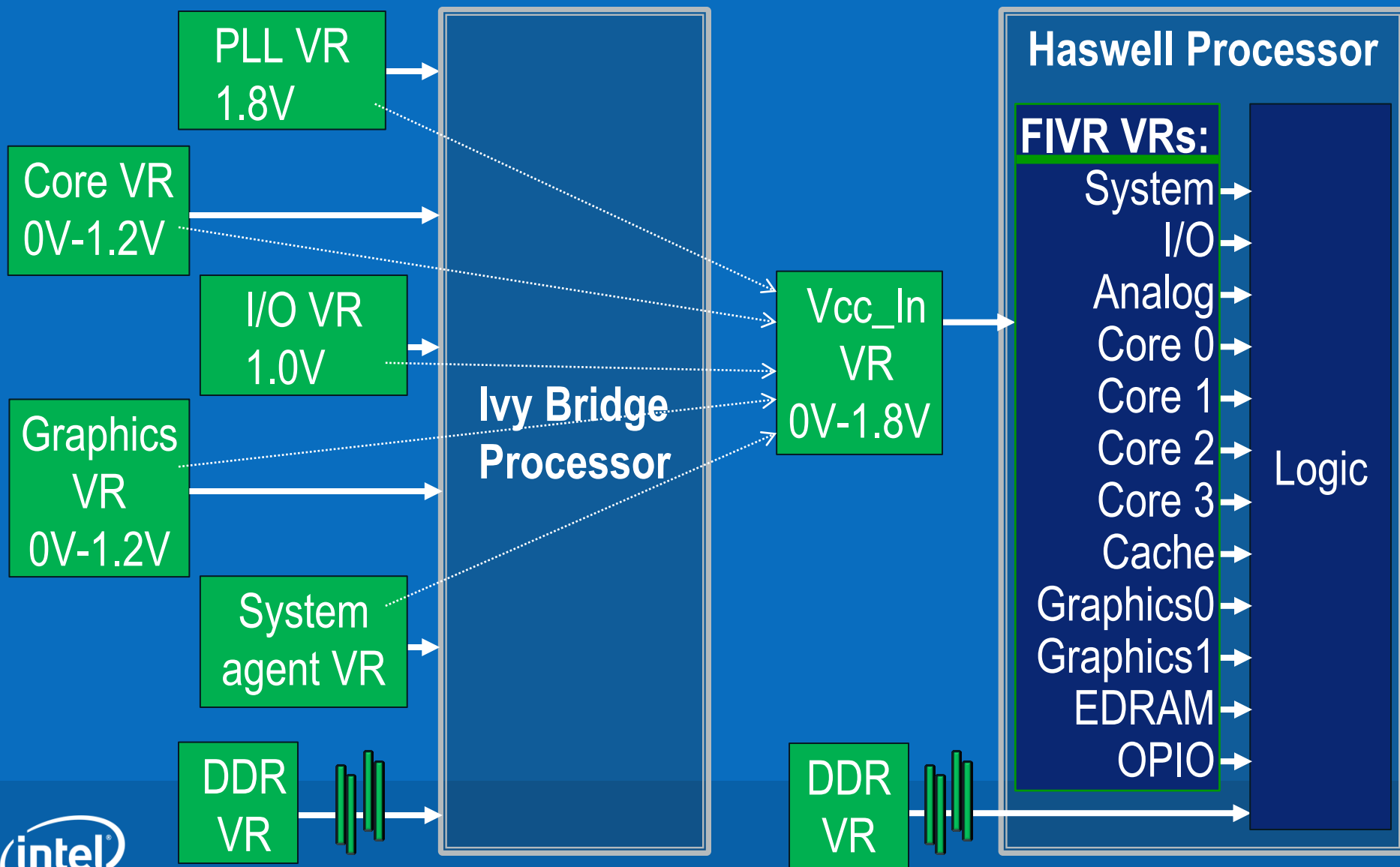


# PACKAGE AND PLATFORM VIEW OF INTEL'S FULLY INTEGRATED VOLTAGE REGULATORS (FIVR)

Edward (Ted) Burton



# Ivy Bridge Platform      Haswell Platform



# FIVR At a Glance

- 140MHz switching frequency
- Up to 16 phases per VR
- Up to 80MHz unity gain
- Non-magnetic package trace inductors
- MIM caps
- Silicon current density of 31 Amps/mm<sup>2</sup>
- Typical efficiency of 90% in turbo



# FIVR Value Proposition

- Platform footprint, cost & thickness reduction
  - Smaller XYZ → more features, thinner handhelds
- Platform power component cost reduction, while doubling graphics, adding EDRAM, doubling vector hardware...
- Battery life improvement
  - Reports of over 50% increase vs prior generation
- Graphics power-perf improvement
  - Tens of % improvement in constrained form-factors

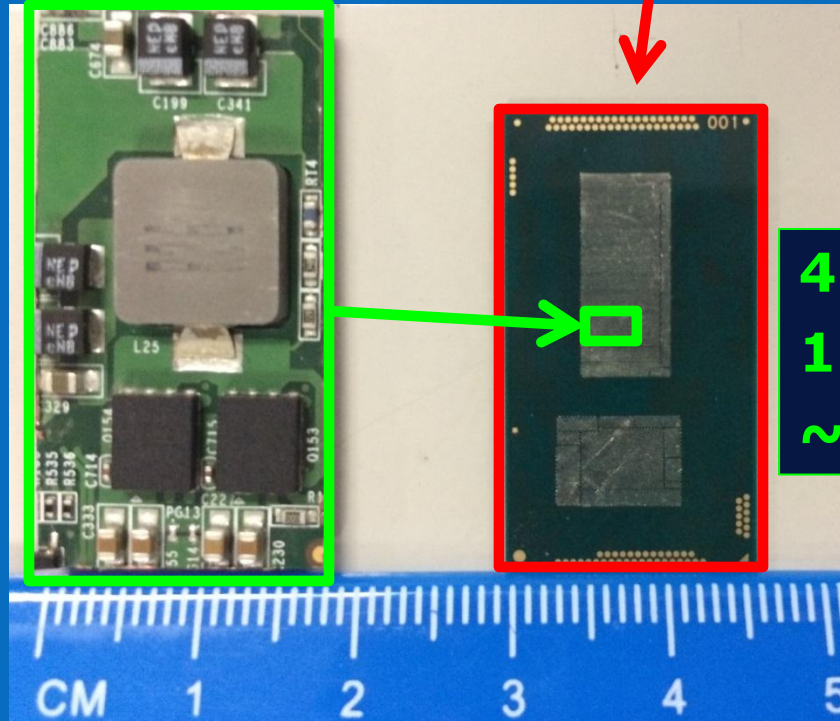
Today's Focus



# Volume Scales $\sim 1/\text{Frequency}$

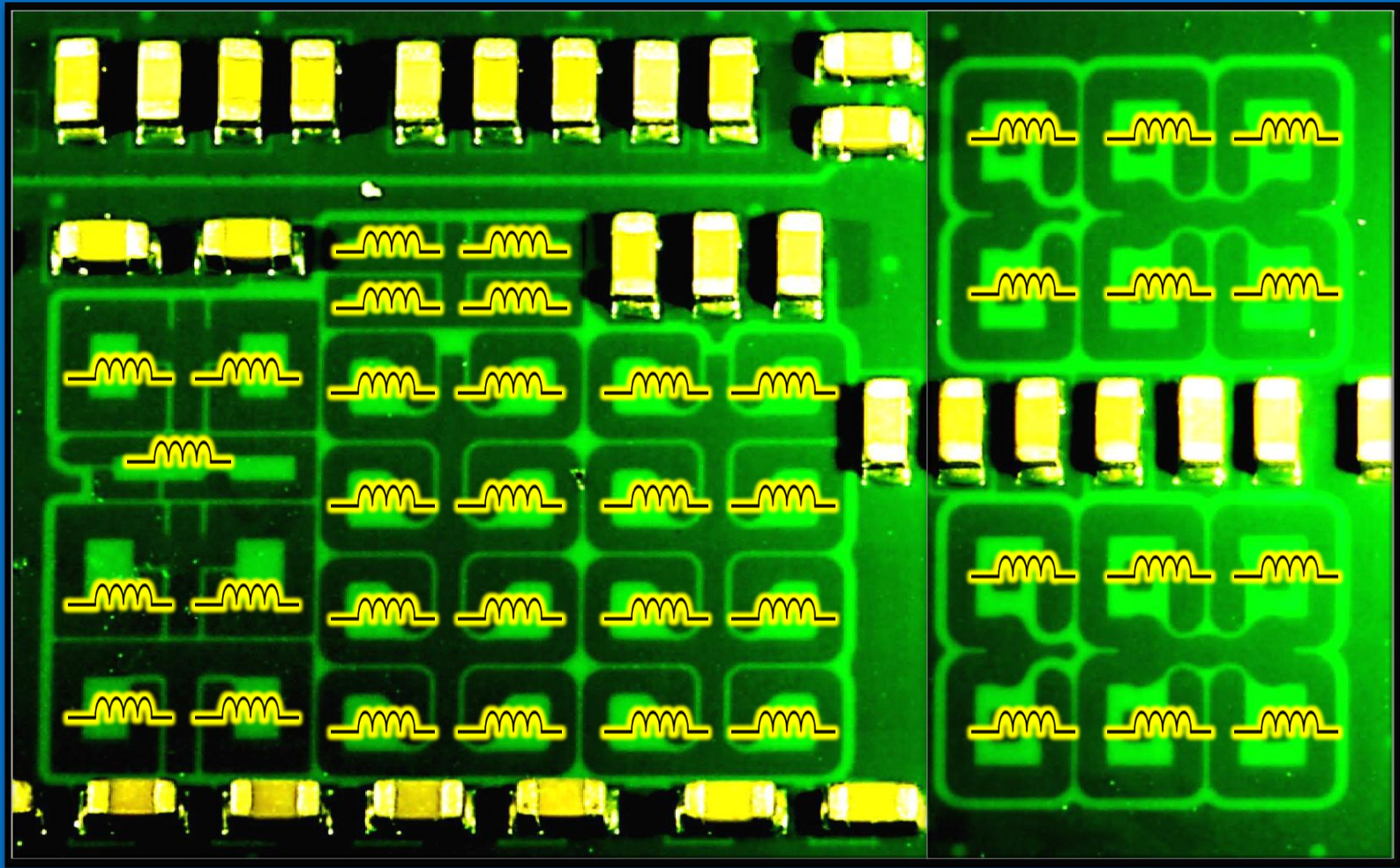
One 30A VR phase,  
prior generation  
Ultrabook  
300kHz Switcher  
800mm<sup>2</sup>

CPU and PCH chips plus  
7 multi-phase FIVRs  
140MHz Switchers  
495mm<sup>2</sup>

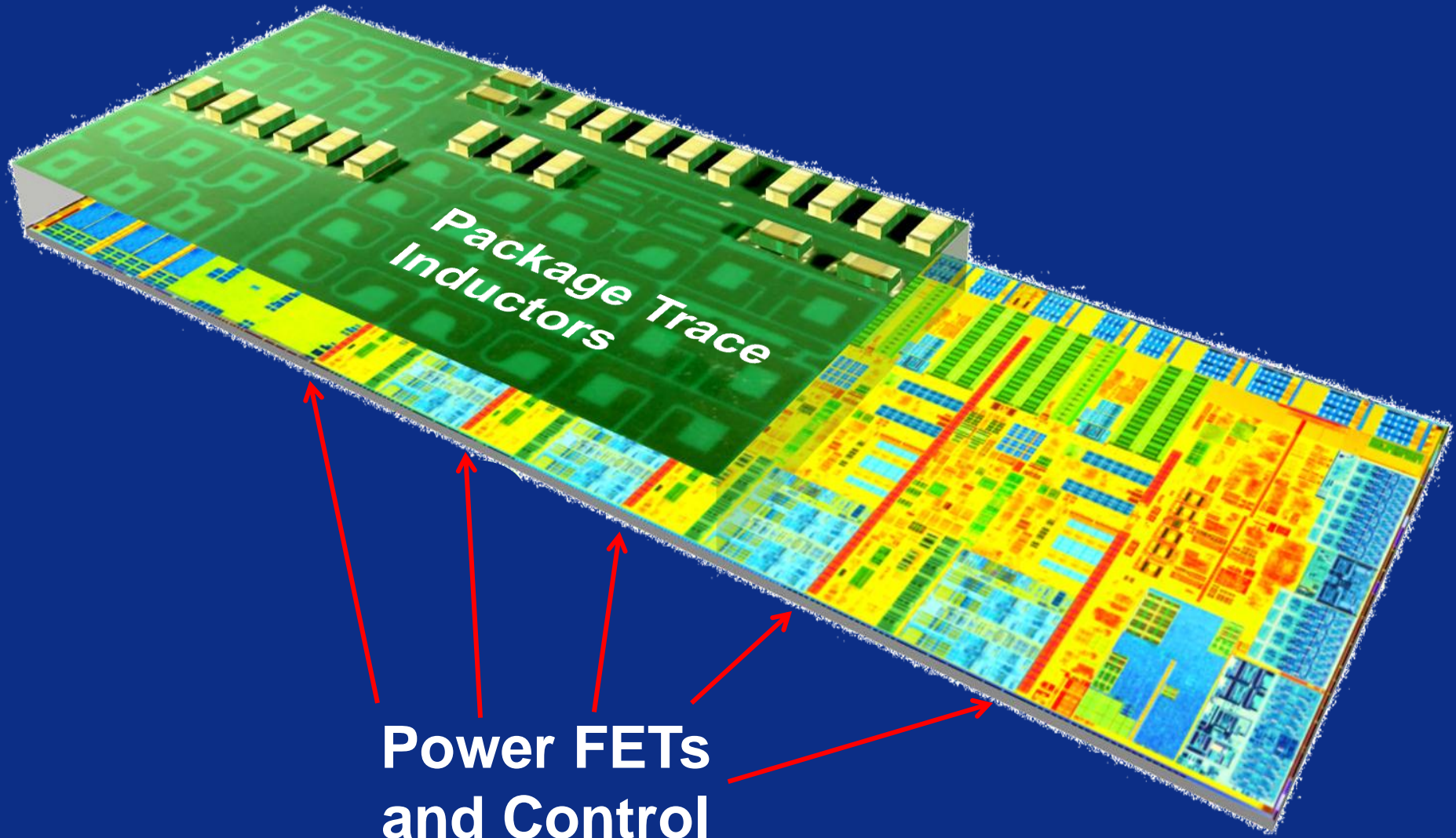


**466x Frequency**  
**111x area shrink**  
 **$\sim 4x$  thickness shrink**

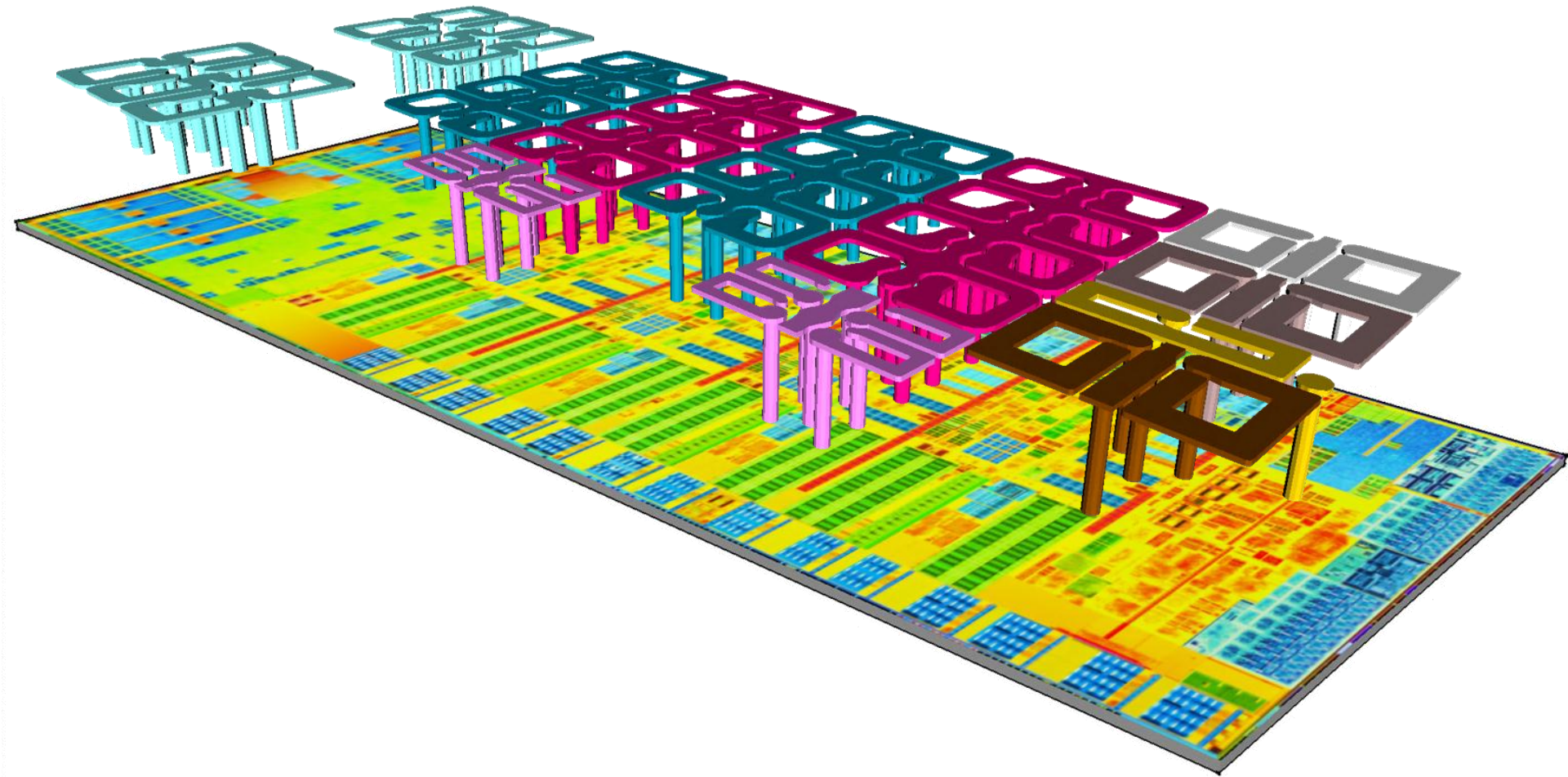
# FIVR Photo - Package Underside



# FIVR Cutaway View

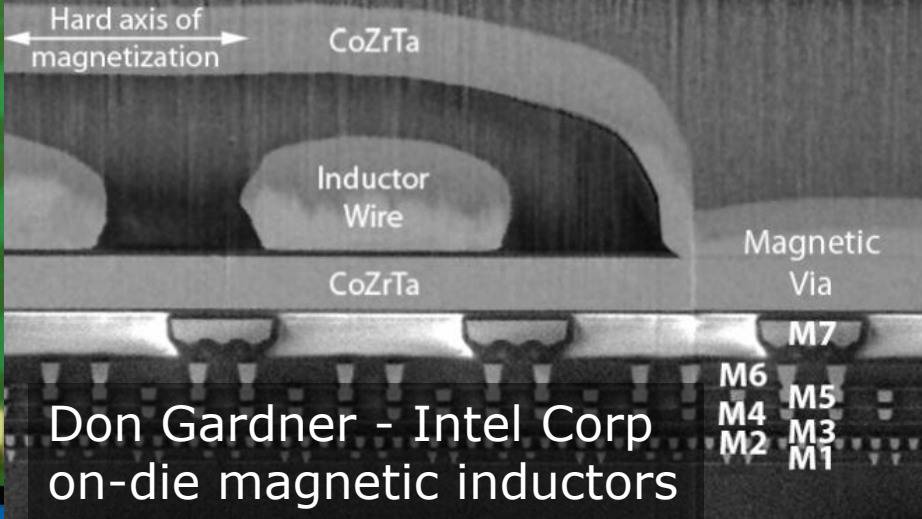
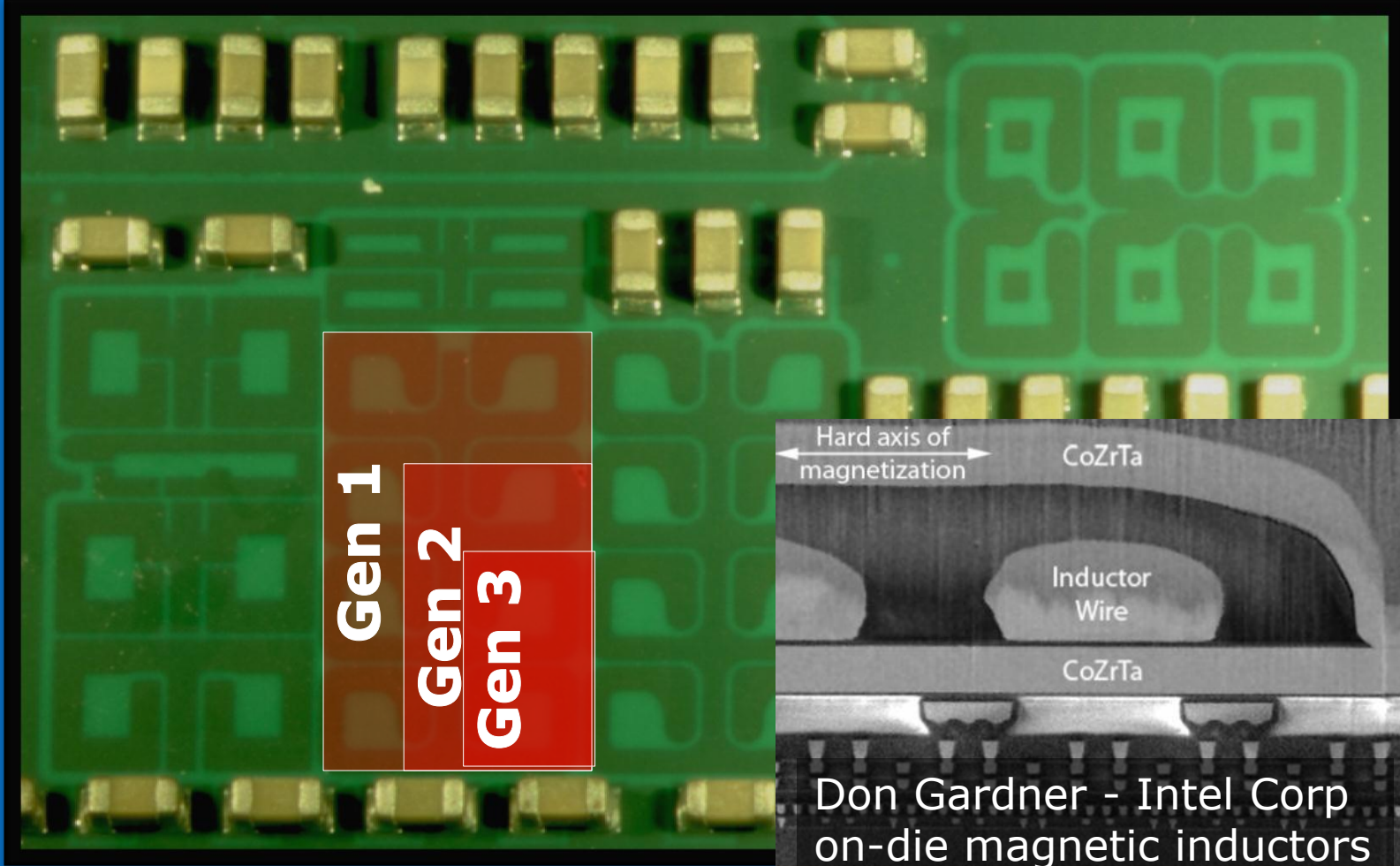


# XRAY View – FIVR Inductors





# Future Scaling Issue & Solution

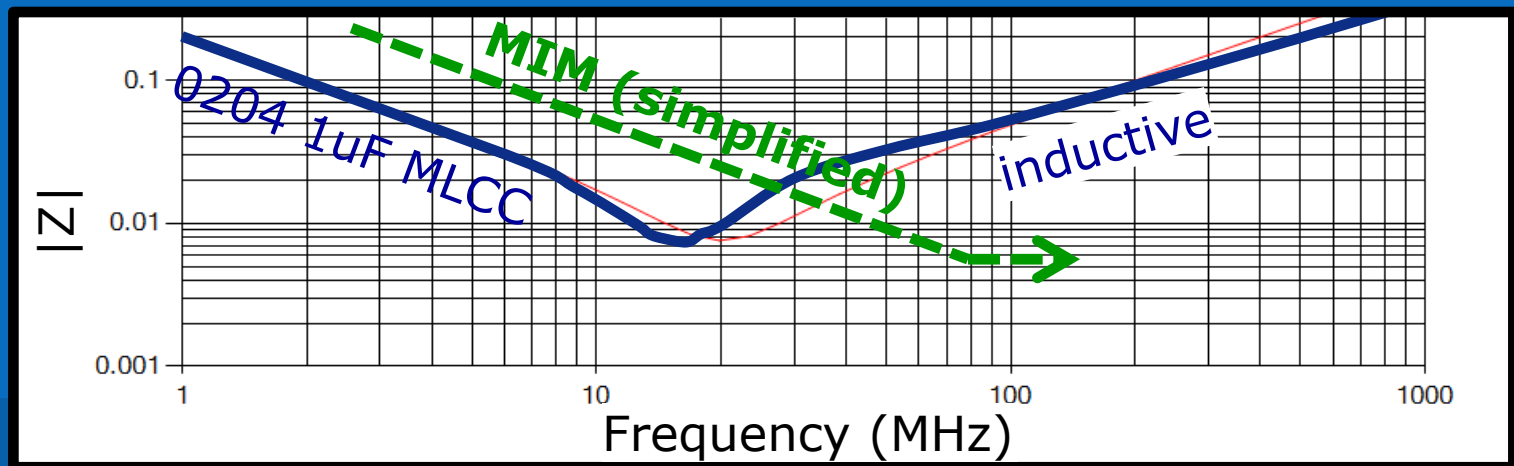


Don Gardner - Intel Corp  
on-die magnetic inductors

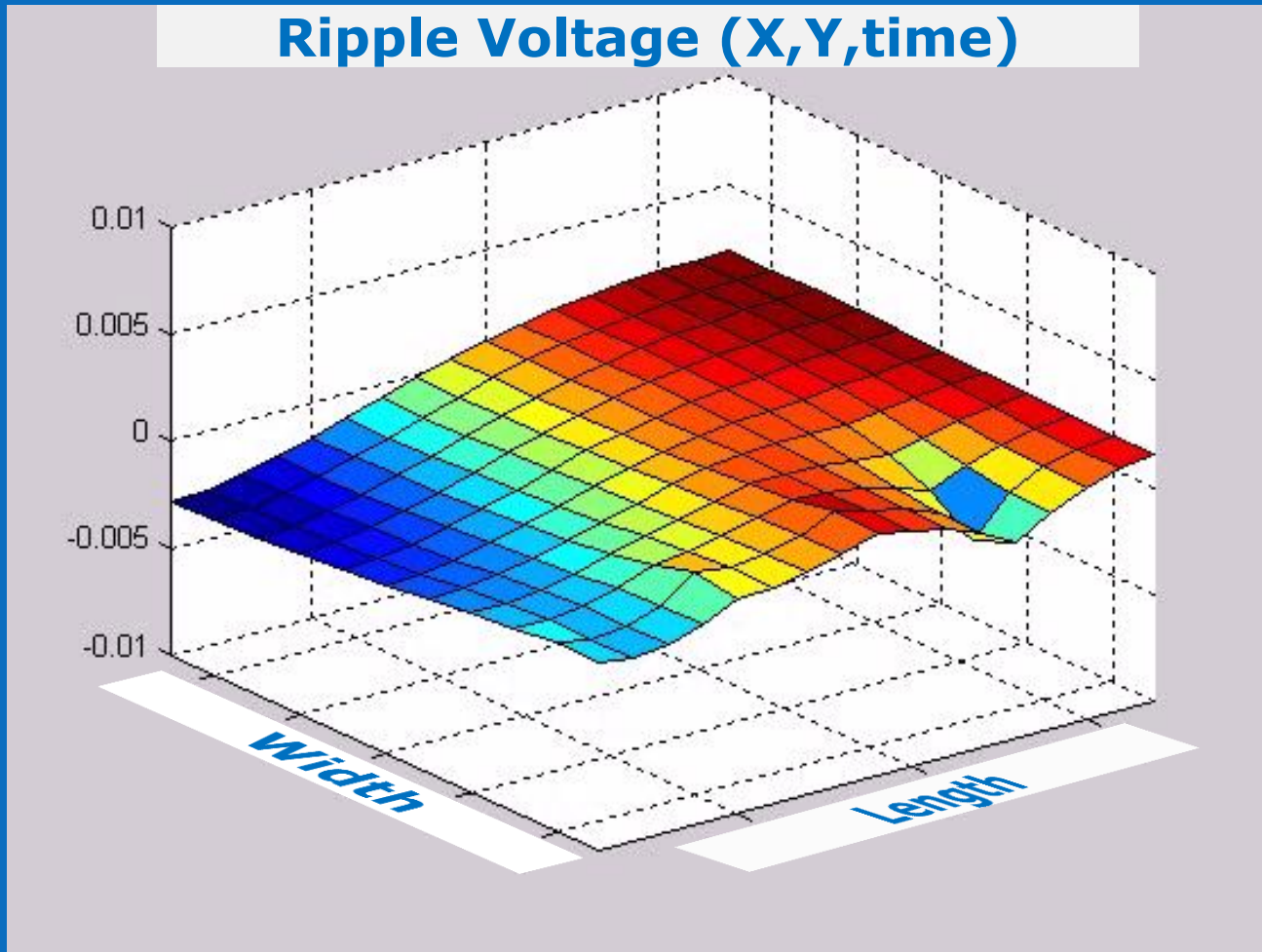


# Typical Package Cap vs MIM

- Reverse geometry 0204 1uF cap impedance curve
- Package cap inductance raises HF Z (70 milliohm @140MHz)
- Needs high frequency parallel die capacitance
- No inductance for uniformly distributed MIM capacitor & uniformly distributed load, so no high frequency increase in Z
- Nonuniform loads get “complicated”
- Real loads and real phases are nonuniform



# Real Behavior “Complicated”

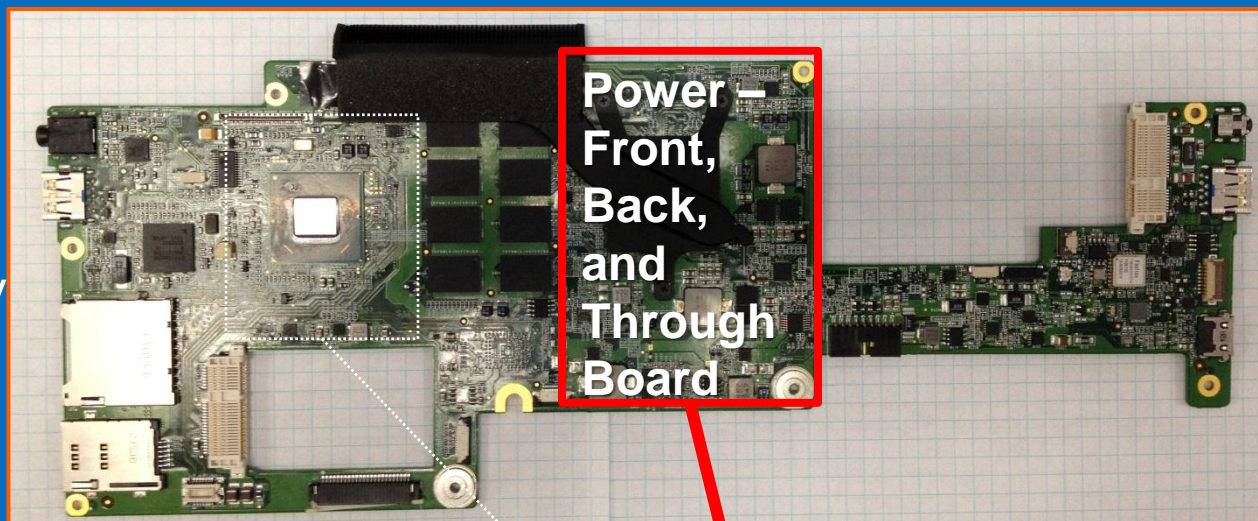


# FIVR → Thinner Handhelds

Ivy Bridge

Backside all power

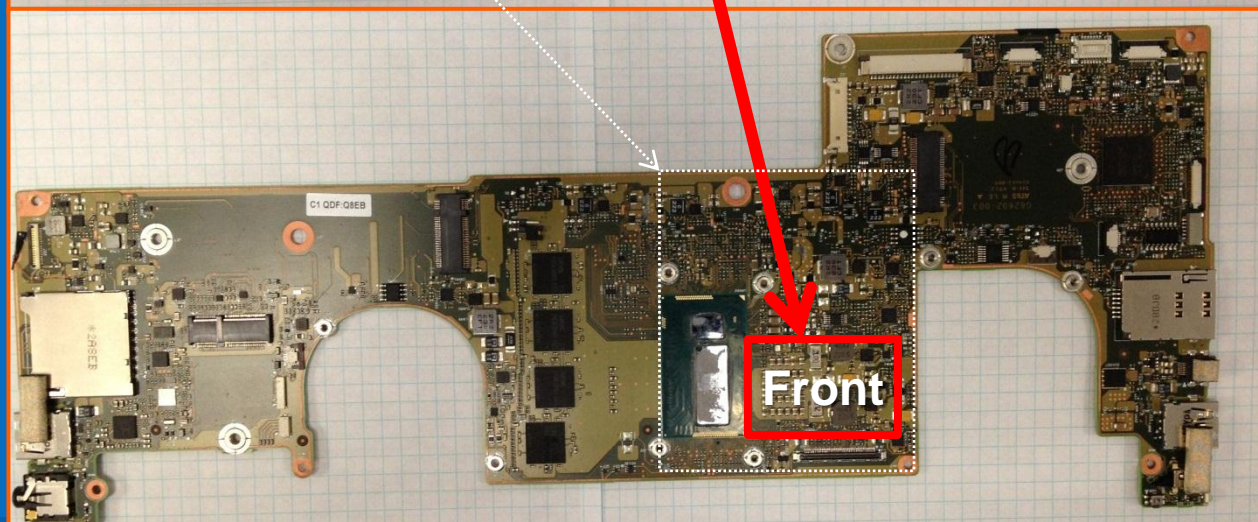
Big inductors, butterfly mounted through board



Haswell

Backside bare

Small inductors & caps & 75% fewer



**2mm thinner – cheaper - 10% larger battery**



# FIVR → More Platform Features

## Ivy Bridge

- × SATA
- × ~~Analog audio~~
- × ~~IR remote~~
- One USB3.0
- two USB2.0
- LAN or Thunderbolt



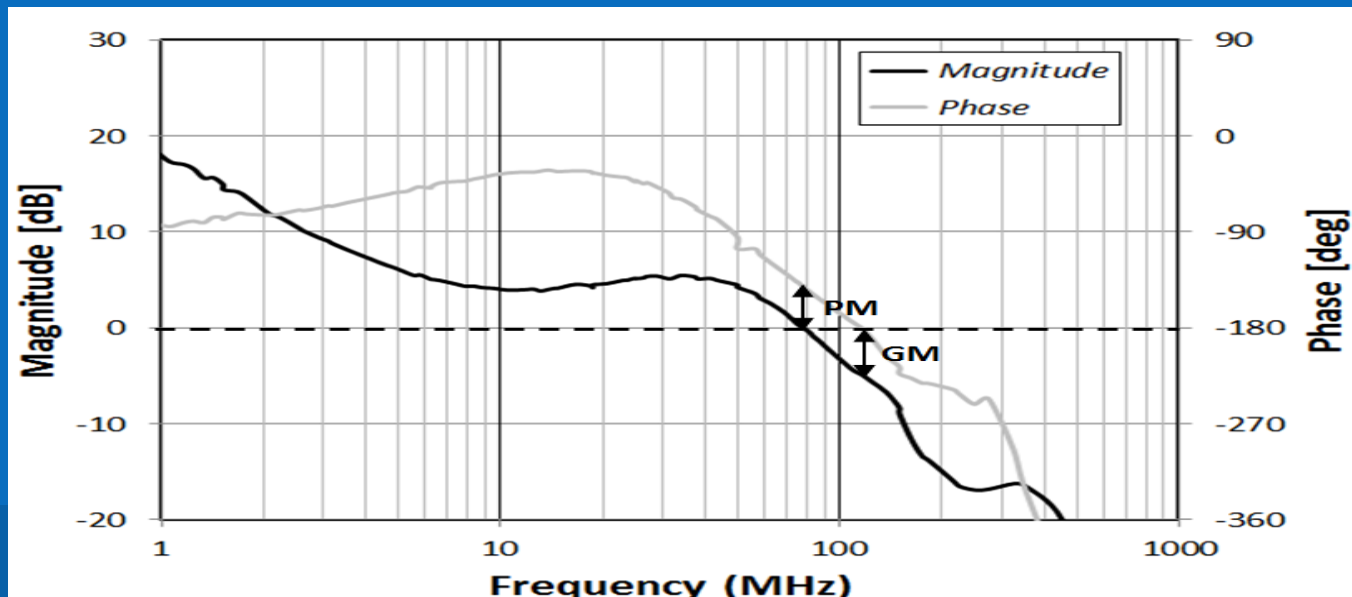
## Haswell

- ✓ SATA
- ✓ Analog audio
- ✓ IR remote
- Four USB3.0
- LAN and Thunderbolt
- 2x graphics
- Free space to add more features
- ~\$5 Saved in power BOM

# High UGB, Fast Transitions

## A Fringe benefit of miniaturization

	Typical prior generation VR	FIVR
Unity Gain Bandwidth	$\leq 80\text{kHz}$	$\leq 80\text{MHz}$
Core and Graphics voltage max transition times	100's of microseconds	100's of nanoseconds



# Power States – 2.6-122x Lower

Package State	Actions taken in various Package States	Ivy Bridge CPU power (W)	Haswell CPU power (W)
C0	Cores, Graphics active	17 W (TDP)	15 W (TDP)
C6	Core's and Graphics FIVRs off DDR in self refresh	2.3	0.9 <b>1/2.6</b>
C7	System agent & DDR IO gated off. CPU critical arrays on Sustain Rail.	2.2	0.85 <b>1/2.6</b>
C8	Display & IO FIVRs off. LLC flushed System Agent gated off. Vin = 1.2V.	N/A	0.077 <b>1/29</b>
C9	Vin set to 0V	N/A	0.018 <b>1/122</b>
C10	Platform power target of 100mW or better.		N/A



# 2x-3x Turbo Power Headroom

## Small platform example:

- Old platform rails 1phase each:
  - Graphics: 30A inductor @  $\sim 1V \rightarrow \sim 30W$  max
  - Cores: 30A inductor @  $\sim 1.1V \rightarrow \sim 33W$  max
- FIVR platform's input rail:
  - 2 30A inductors @ 1.7V  $\rightarrow$  102W max (shared dynamically)
  - Core-only workloads: Triple the available turbo power
  - Graphics workloads: Double the available turbo power for graphics

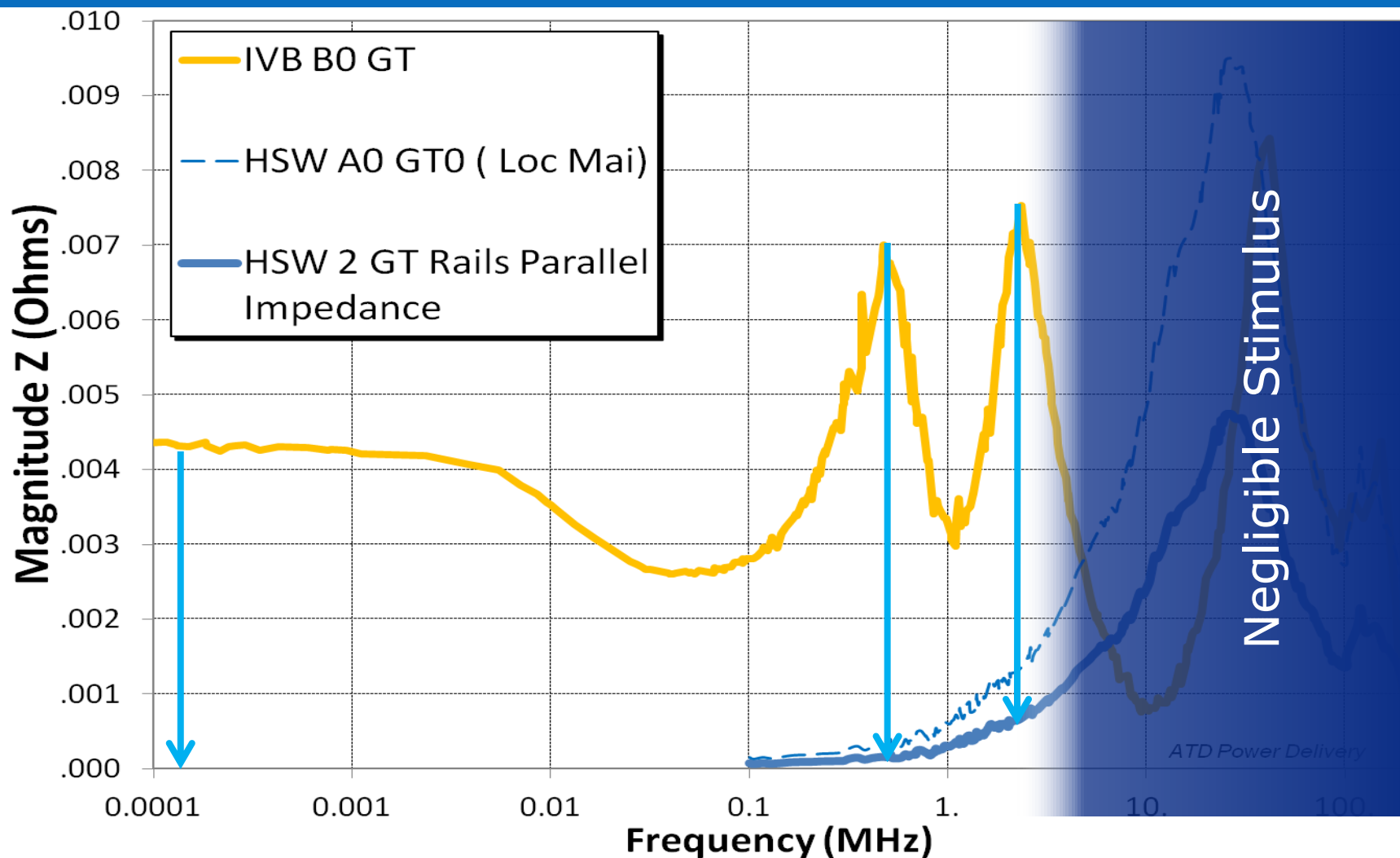
## More Turbo Power Headroom $\rightarrow$ More Performance

- Higher burst frequency
- Larger graphics
- More cores

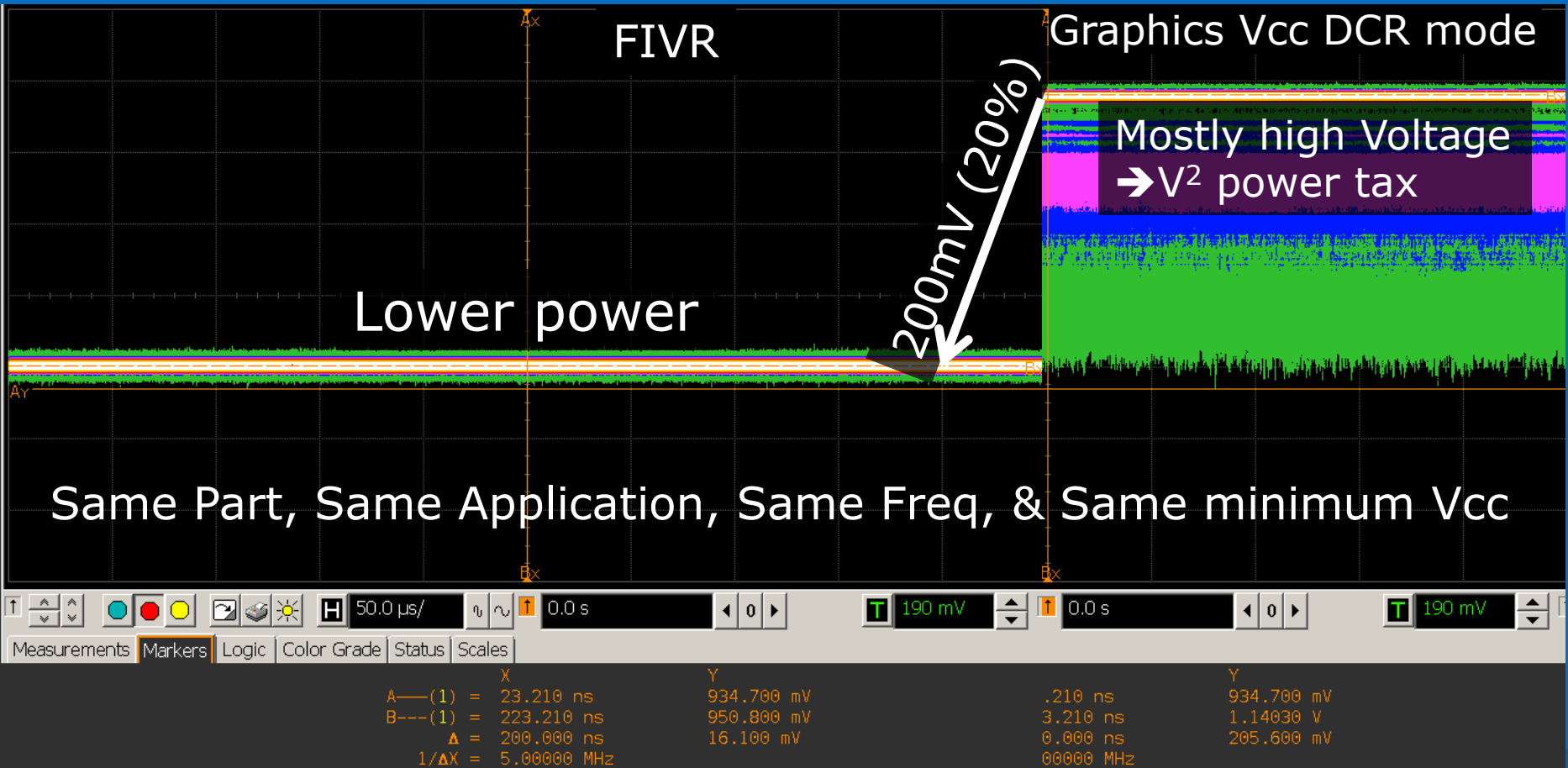




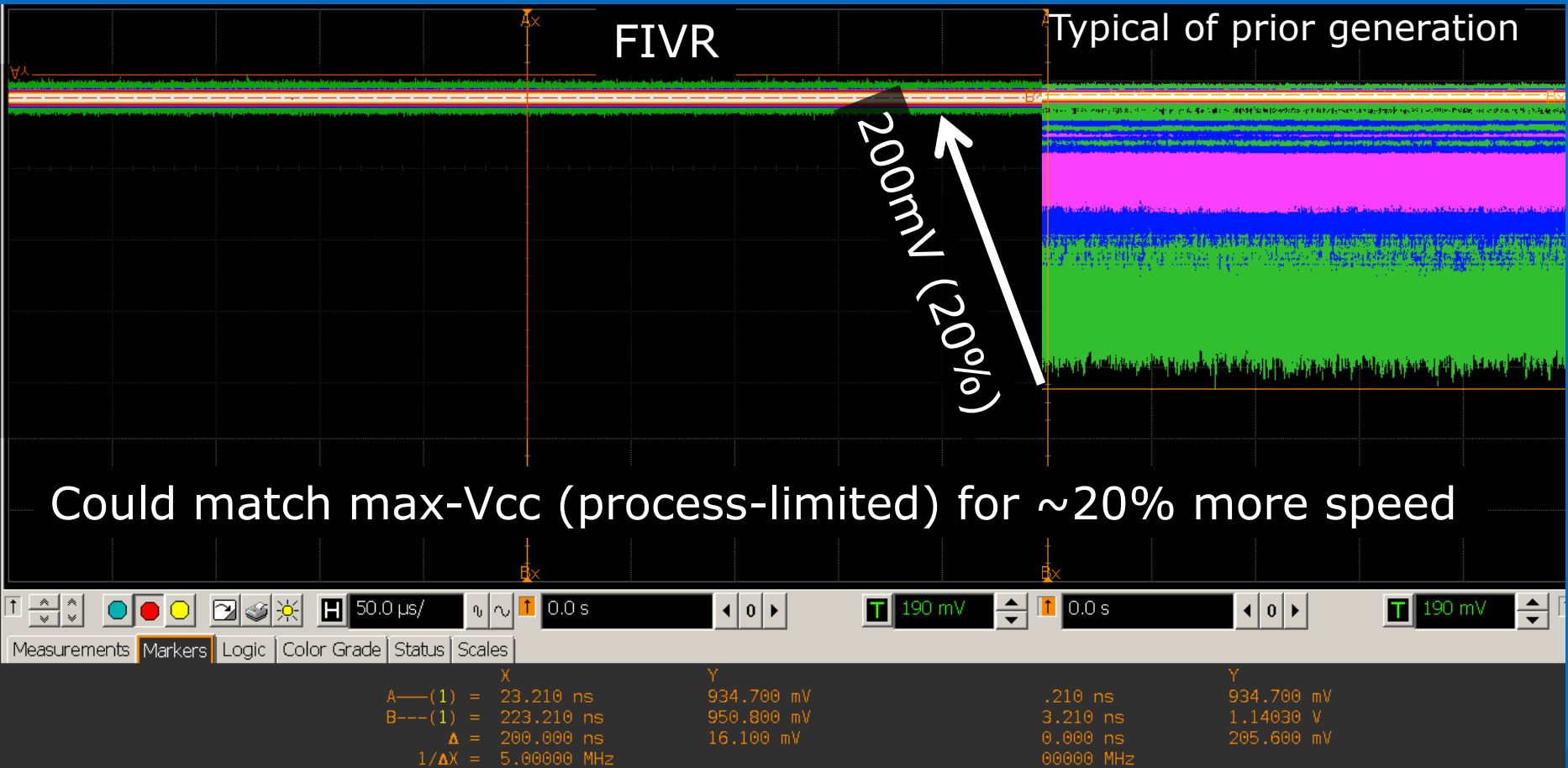
# Graphics - 95% Lower Effective Z



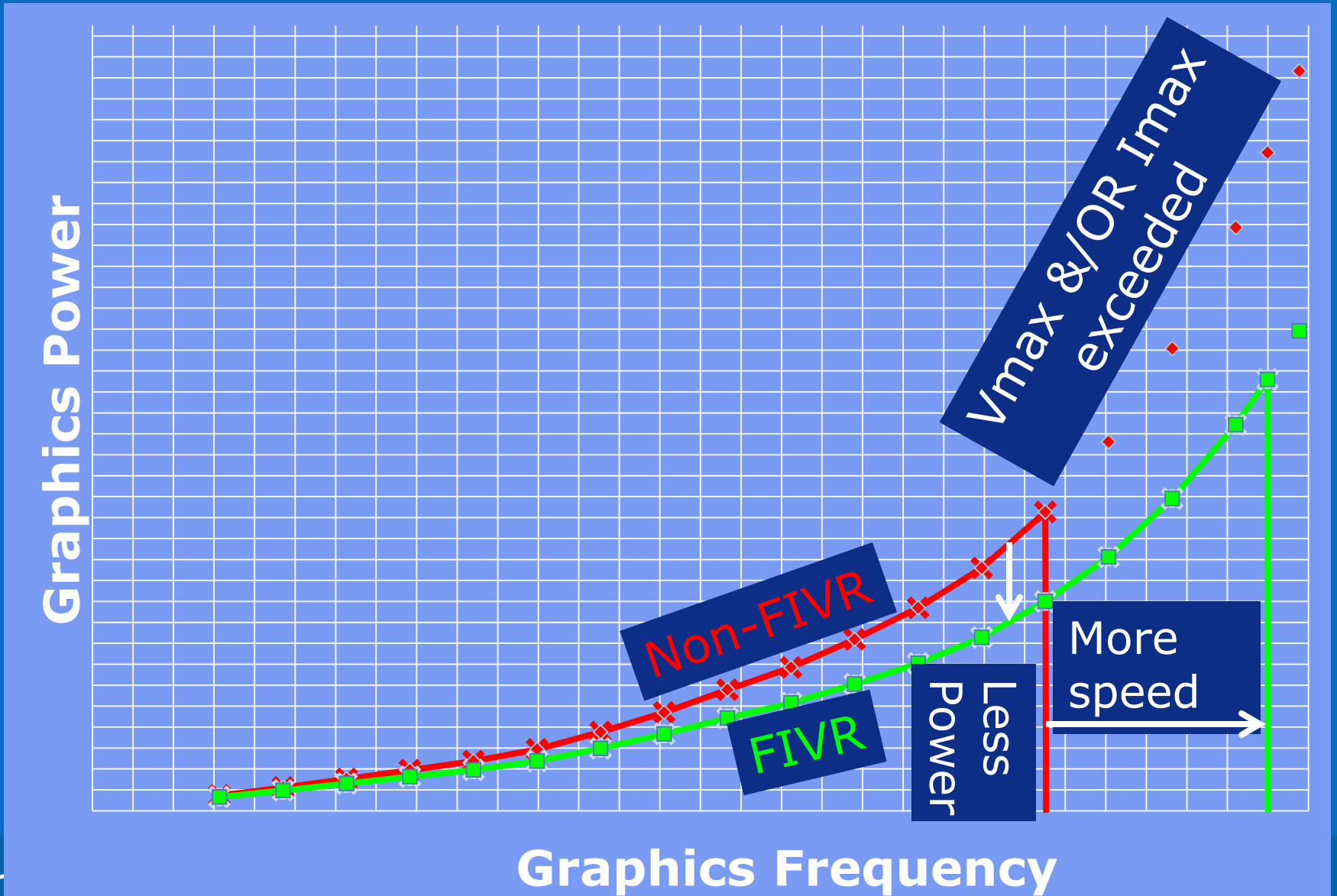
# Graphics Power Reduction (Typical Example)



# Graphics Speedup (Cut/Pasted Prior Example)



# Lower Power, Higher Speed



# Summary

- 140MHz switching enables integrated output filters
  - On-die MIM capacitors; package trace inductors
  - Thinner platforms, with more features
  - Reduced power component cost, while doubling graphics and core vector hardware and adding EDRAM
- Battery Increased life by upwards of 50% on many platforms
  - Quickly ramped input and output rails to support new sleep states
  - Set every rail to its optimal voltage
- Improved graphics power-perf 10's of %



# Supporting Slides



# 90% Efficiency at Full Vout

